4-17-1997

Telemetric Torque Measurement System

Jason Joseph
Western Michigan University, jason@thejosephfamily.org

Francisco Sinta
Western Michigan University

Jeff Williams
Western Michigan University

THE CARL AND WINIFRED LEE HONORS COLLEGE

CERTIFICATE OF ORAL EXAMINATION

Jason Joseph, having been admitted to the Carl and Winifred Lee Honors College in 1993, successfully presented the Lee Honors College Thesis on April 17, 1997.

The title of the paper is:

"Telemetric Torque Measurement System"

Dr. John Gesink
Electrical and Computer Engineering

"Telemetric Torque Measurement System"

By Jason Joseph, Francisco Sinta, Jeff Williams

Advisor: Dr. John Gesink

Electrical and Computer Engineering 482

April 15, 1997

Abstract

The Telemetric Torque Measurement System (TTMS) was designed to measure the torque produced by a snowmobile engine. The design of the TTMS was refined and modified in stages, leading to the final design. The TTMS consists of two basic sections: the transmitter section and the frequency demodulator section. The transmitter section effectively measures the torque on a snowmobile jack-shaft. The torque signal is converted into a voltage which is then fed into a voltage to frequency converter and converted into an audio tone. This tone is broadcast in the FM broadcast band via an FM transmitter. An FM receiver then receives the audio tone. The frequency demodulator section receives the encoded signal from the FM receiver through a headphone jack and converts the signal into a voltage that is proportional to torque applied to the snowmobile jack-shaft.

Several tests were completed to verify the operation of the TTMS and its ability to meet the design specifications. Some specifications were not verified because of lack of test equipment. The TTMS project was tested and calibrated using known torque values. The test results showed that the TTMS is capable of producing a linear output voltage that is proportional to torque. The TTMS is capable of running for at least 3 hours on one set of batteries, and is capable of spinning at a speed of at least 2000 RPM. The dimensions of the TTMS meet specifications, and the range of transmission is at least 10 feet. Some minor changes to the TTMS design were made consisting of only component value changes. Overall, the TTMS project was successful.

Disclaimer

This report was generated by a group of engineering seniors at Western Michigan University. It is primarily a record of a project conducted by these students as part of curriculum requirements for being awarded an engineering degree. Western Michigan University makes no representation that the material contained in this report is error free or complete in all respects. Therefore, Western Michigan University, its faculty, its administration or the students make no recommendation for use of said material and take no responsibility for such usage. Thus persons or organizations who choose to use said material for such usage do so at their own risk.

WESTERN MICHIGAN UNIVERSITY
COLLEGE OF ENGINEERING AND APPLIED SCIENCES
DEPARTMENT OF ELECTRICAL ENGINEERING
KALAMAZOO, MICHIGAN 49008

SENIOR DESIGN PROJECT REPORT RELEASE FORM

In accordance with the "Policy on Patents and Release of Reports Resulting from Senior Design Projects" as adopted by the Executive Committee Of the College of Engineering and Applied Sciences on Feb. 9, 1989, permission is hereby granted by the individuals listed below to release copies of the final report written for the Senior Design Project entitled:

PROJECT TITLE: Telemetric Torque Measurement System

PROJECT SPONSOR: Smiths Industries

TEAM MEMBERS NAMES:

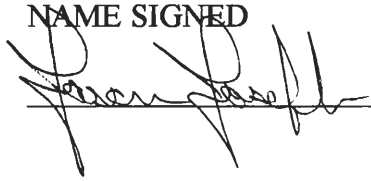
NAME PRINTED	NAME SIGNED	DATE
Jason Joseph		4-14-97
Francisco Sinta		
Jeff Williams		

Table of Contents

Acknowledgments

The design team would like to thank our sponsor, Smiths Industries, for their support and assistance with this project. We would like to thank our advisor, Dr. John Gesink, for his help in all aspects of this project. We would also like to thank James Vandepolder, the Mechanical Engineering Department, and the Automotive Engineering Department for their continued support in testing and development of the project.

Summary

The Telemetric Torque Measurement System (TTMS) was designed to measure torque applied to a rotating shaft at speeds up to 9000 RPM. Several approaches were considered for the design, leading to the final TTMS design concept. The final design uses a strain gage bridge to sense torque in a rotating shaft. This torque signal is transmitted to a stationary receiver that outputs a voltage proportional to the torque applied to the shaft.

The main design constraint was the overall physical size of the TTMS. The specifications require the TTMS to have a radial clearance of .75" and an axial length of 1.5" not including the strain gage array. The TTMS was designed by researching components and using a syntheses design methodology.

The basic structure of the TTMS begins with a strain gage array to gather torque data in the form of a voltage proportional to strain measured. An instrumentation amplifier is then used to amplify the strain gage signal. A voltage to frequency converter is used to modulate the voltage signal for FM transmission. This signal is then fed into an FM transmitter to transmit the torque data. An FM receiver demodulates the transmitted signal. Finally, a frequency demodulator circuit is used to convert the signal from the FM transmitter into a voltage proportional to the torque applied.

The transmitter section of the TTMS is powered by two 3.5V lithium batteries connected in series. The 7V supply is regulated to 5V by a voltage regulator. The

receiver section is powered by a ±9V supply in the form of two 9V batteries connected in series with the mid-point connected to ground.

The transmitter section of the TTMS is built on a printed circuit board, and secured in a nylon housing that also houses the FM transmitter and lithium ion batteries. The phase locked loop section of the TTMS is built on a breadboard.

The TTMS was tested using five different tests. The first test was designed as a preliminary test to verify the operation of the TTMS. This test was completed qualitatively, and was used to judge the overall operation of the circuit. This test showed that the TTMS was capable of producing an output voltage that was proportional to the differential voltage applied to the input of the TTMS. The second test was designed to measure ability of the TTMS to measure torque under static conditions, without rotation. This test showed that the TTMS produces a linear output voltage that is proportional to torque applied to the shaft under test. The third test was designed to measure the battery life of the TTMS system. Test results showed that the battery life of the TTMS is greater than three hours, and exceeds the requirements outlined by the design specifications. The fourth test was designed to measure the ability of the TTMS to rotate at high speeds without physical damage. This test was completed at a rotational speed of 2000 RPM and no physical damage was incurred. The final test was used to test the transmission range of the TTMS. The test results showed that the TTMS is capable of transmitting a distance greater than 10 feet.

Overall, the TTMS system operates as expected. Design modifications were minimal, and the test results showed that the voltage output of the frequency demodulator circuit is proportional to the torque applied to the shaft under test.

Introduction

The Telemetric Torque Measurement System (TTMS) was designed to measure torque in the rotating jack-shaft of a snowmobile. The TTMS project was introduced because of a desire to maximize snowmobile performance for racing applications. For racing, it is necessary to maximize the torque output of a snowmobile to improve acceleration. In order to adjust engine settings, a dynamic torque measurement system that is capable of measuring the torque output of a snowmobile engine is required. This project is also designed to test and improve the design skills of the design team.

The success of the project is dependant on satisfying several questions. Is it feasible to have electrical components rotating at speeds in excess of 8000 RPM? Is it feasible to transmit signals in the radio frequency band at these high speeds and receive a clean signal? If so, should these delicate components be protected and how will they be protected? The purpose of this project was to answer these questions and analyze the performance characteristics of the TTMS through engineering design, development, and testing. The performance characteristics include the ability of the TTMS to effectively measure torque on a rotating snowmobile jack-shaft. To effectively measure torque, the TTMS must meet the required design specifications.

The scope of this project was to design, build, test, and analyze a working prototype of the Telemetric Torque Measurement System. Learning, developing, and testing the engineering concepts involved in the TTMS using true engineering design methodology were also included in the scope of the project. The final aspect of the scope was to show the relationship between theoretical design and practical application, and

illustrate the types of problems that arise and solutions that can be obtained only by fully analyzing all aspects of the design. The TTMS project illustrates some typical problems and solutions that occur when dealing with signal processing systems and electronic measurement of mechanical variables.

Discussion

TYPICAL TORQUE MEASUREMENT SYSTEM

All torque measurement systems have a similar structure. A typical torque measurement system is shown below in figure 1.

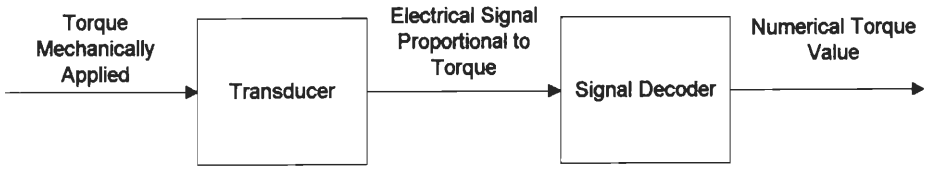


Figure 1 – Torque Measurement System

The input to the torque measurement system is a torque mechanically applied to a given object. This torque is sensed by a transducer. A transducer converts this mechanical input into an electrical output. This electrical output is proportional to the torque applied to the object. This electrical output is then converted into a numerical torque value by a signal decoder. A signal decoder is a device that takes an electrical input and produces a readable output. Examples of signal decoders include multi-meters and oscilloscopes.

TORQUE MEASUREMENT SYSTEM FOR A ROTATING SHAFT

This system changes depending on the application for which it is designed. Consider torque produced by any motor, such as and automobile engines and snowmobile engines. An engine's power is delivered to these vehicles through a drive-train, which

includes a drive shaft. The power delivered by the engine creates a torque in the drive shaft, which must rotate to propel the vehicle. Therefore, one application of a torque measurement system involves measuring torque on a rotating shaft.

The system shown in figure 1 is used to measure torque on a rotating shaft. Torque is input to a transducer, which converts the torque signal into an electrical signal. The method in which the transducer output is delivered to a decoder must be changed for a rotating system. This change occurs because wires cannot be connected directly from the transducer to the decoder unless the decoder is located on the shaft. Logically, fastening a decoder directly to a shaft is not desirable. For this reason, the decoder is located away from the shaft.

There are two basic methods for delivering the torque signal from a transducer to a decoder circuit. The first method involves using slip-rings, and the second method involves using wireless communication. In certain applications, slip-rings are desirable because of the ability to directly connect the transducer to the decoder. Because of this simplicity, the system shown in figure 1 will not change. However, slip rings are usually large and cannot be conveniently located in small engine compartments. Using wireless transmission, a torque measurement system can be constructed using only additional electronic components. Using the wireless technology that is available today, the size of the system can be minimized.

A signal flow diagram of a wireless torque measurement system is shown in figure 2.

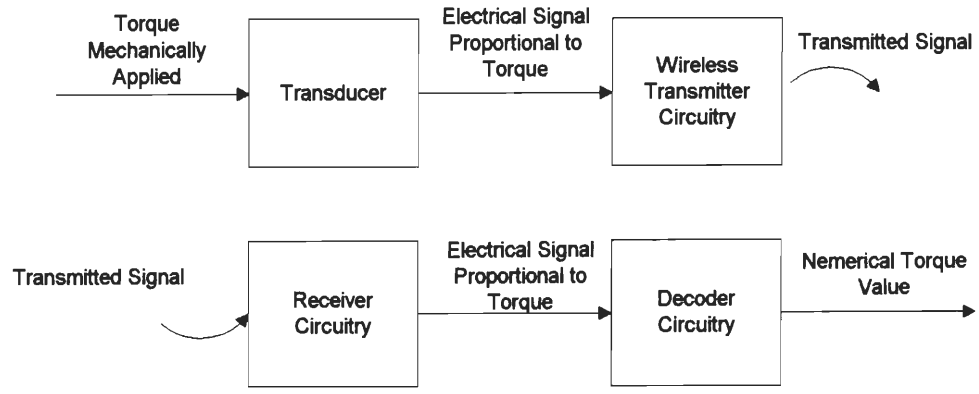


Figure 2 – Wireless Torque Measurement System

TELEMETRIC TORQUE MEASUREMENT SYSTEM

Specifications were developed with Smiths Industries for the Telemetric Torque Measurement System (TTMS). The specifications have been divided into two sections. The first section is the transmitter section. The transmitter includes all components leading from the transducer to transmitter. The second section, the receiver section, consists of the receiver and decoder circuitry. These two sections make up the TTMS. The specification for the system are given below.

(**R** = Requirement, **G** = Goal, **P** = Preference)

1. The torque measurement system must be capable of measuring unidirectional torque values ranging from 0 ft-lb. to 110 ft-lb. (0lb-in to 1320 lb-in) on a 1" diameter shaft of a snowmobile. **R**
2. The torque measurement system must be capable of measuring strains on the shaft of a snowmobile that will be present on a carbon steel shaft with a modulus of elasticity (G) of approximately 30,000,000 psi. **R**

3. The torque measurement system must operate at shaft rotation speeds up to 9000 revolutions per minute. **G**
4. The transmitter section must have an axial mounting length on the shaft of less than 1.5". The outer diameter of the transmitter section must be less than 2.5". **R**
5. The transmitter section must have a self contained power supply (i.e. a battery). **R**
6. The transmitter section must have a battery life greater than or equal to one hour. **G**
7. The transmitter section must modulate an FM carrier signal with a frequency proportional to the strain measured by the transducer. **R**
8. The instantaneous frequency of the transmitted signal must be within the range of 100Hz to 10kHz. **R**
9. The carrier frequency of the FM transmitter must be adjustable from 88MHz to 108Mhz. **R**
10. The transmitter section and receiver section must operate properly at a distance of 10 feet apart. **R**
11. The output of the torque measurement system must be a voltage that is proportional to the torque being applied to the shaft of the unit under test. **R**
12. The cost of the torque measurement system must be kept to a minimum. The absolute maximum cost for components is $2000. **R**
13. The torque measurement system must not entail manufacturing processes that are not within the ability of Smiths Industries or that of the design team. **R**

The above specifications led to a design concept for the TTMS shown in figure 3.

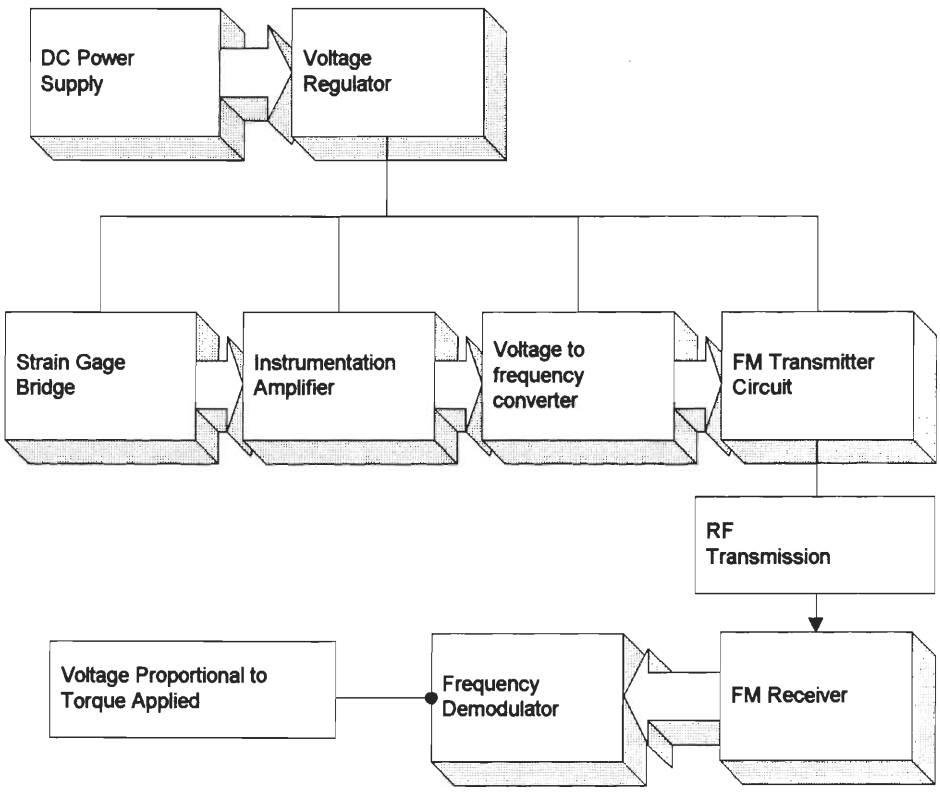


Figure 3 - Telemetric Torque Measurement System

The system concept is built upon the use of a strain gage bridge as a torque transducer. Strain gages are capable of detecting deflection in a rotating shaft (strain) and converting the strain signal to an differential voltage that is proportional to torque applied. Strain gages function by changing their resistance with changes in strain. By measuring the change in resistance of the strain gages, the strain can indirectly be measured. On approach to measuring this change in resistance is placing four strain gages in a Wheatstone bridge formation with opposite legs measuring positive strain and the adjacent legs measuring negative strain. By applying a voltage to the bridge, a differential voltage

that is proportional to the change in resistance is developed that can be measured. Since torque is related to strain by a constant that is dependant on the material of the shaft, and change in strain gage resistance can be related to torque, and thus to differential voltage.

Typical changes in the resistance of strain gages are very small. Because of this, the differential voltage produced by a Wheatstone bridge is also very small. In order to improve transmission of the voltage signal that is proportional to torque, an amplifier must be used. To minimize the effects of noise on the system, a instrumentation amplifier was selected because of its high common mode rejection ratio.

The output signal of the instrumentation amplifier is converted to a frequency in the audio band (20Hz – 20kHz) that is proportional to torque applied via a voltage to frequency converter. The output of the voltage to frequency converter(VFC) is transmitted to an FM receiver via an FM transmitter in the FM broadcast band (88 – 108 MHz).

The modulated FM signal is transmitted a short distance (approx. 10ft.) and demodulated by the FM receiver. The output of the receiver is the audio tone and is proportional to the torque measured by the strain gage array. A tone decoding circuit then converts the audio tone into a voltage proportional to the torque transmitted by the jack-shaft. Adjustable gain and offset features were added to the frequency demodulator circuit to allow for fine tuning and calibration of the TTMS. The output voltage from the frequency demodulator circuit can be fed into a volt-meter, an oscilloscope, or a chart recorder, depending on the needs of the user.

The circuits that were developed for the TTMS are shown in figure 4 and figure 5 . A parts list of the TTMS is also shown in Table AI of Appendix A.

The strain gage array was simulated with potentiometers to produce the varying differential voltage of the Wheatstone Bridge. A 9VDC power supply was substituted for batteries in this test circuit. The output of the Wheatstone Bridge is a voltage with a range of 0 to 2.24mV, based on a gage factor of 2. This signal is fed into the AMP04 instrumentation amplifier. The 0 to 2.24mV range corresponds to a torque range of 0 to 110 ft-lb. The AMP04 has a gain of 125, and has an offset of 1.12V that is set by the OP90 in a voltage follower configuration to align the zero torque frequency of the voltage to frequency converter. The output of the AMP04 is then attenuated by a voltage divider, R_{lp1} and R_{lp2}, resulting in a voltage swing from .666V to 1.000V for positive torque. This voltage is then fed into a voltage to frequency converter. The frequency output of the AD654(VFC) swings between 2000Hz and about 2500Hz. The output of the voltage to frequency converter is then fed into a FM-5 transmitter for broadcast in the 88MHz to 108MHz FM band. A signal flow block diagram is shown in figure 6.

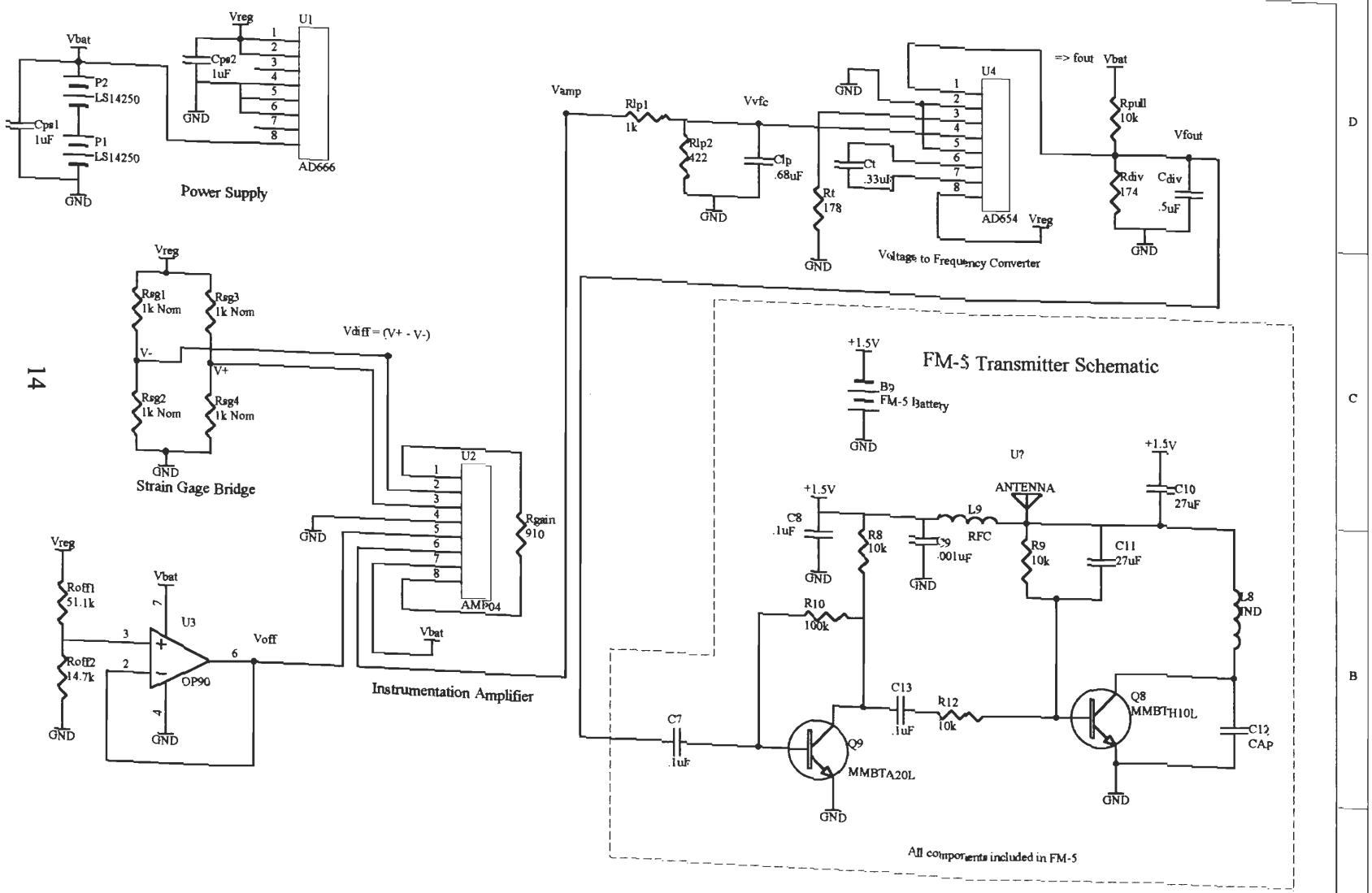


Figure 4

Title	Strain Gage Transmitter Circuit		
Size: A	Number:		Revision: A
Date:	13-Apr-1997	Sheet 6f	
File:	C:\DATA\...\TRANS2.SCH	Drawn By:	

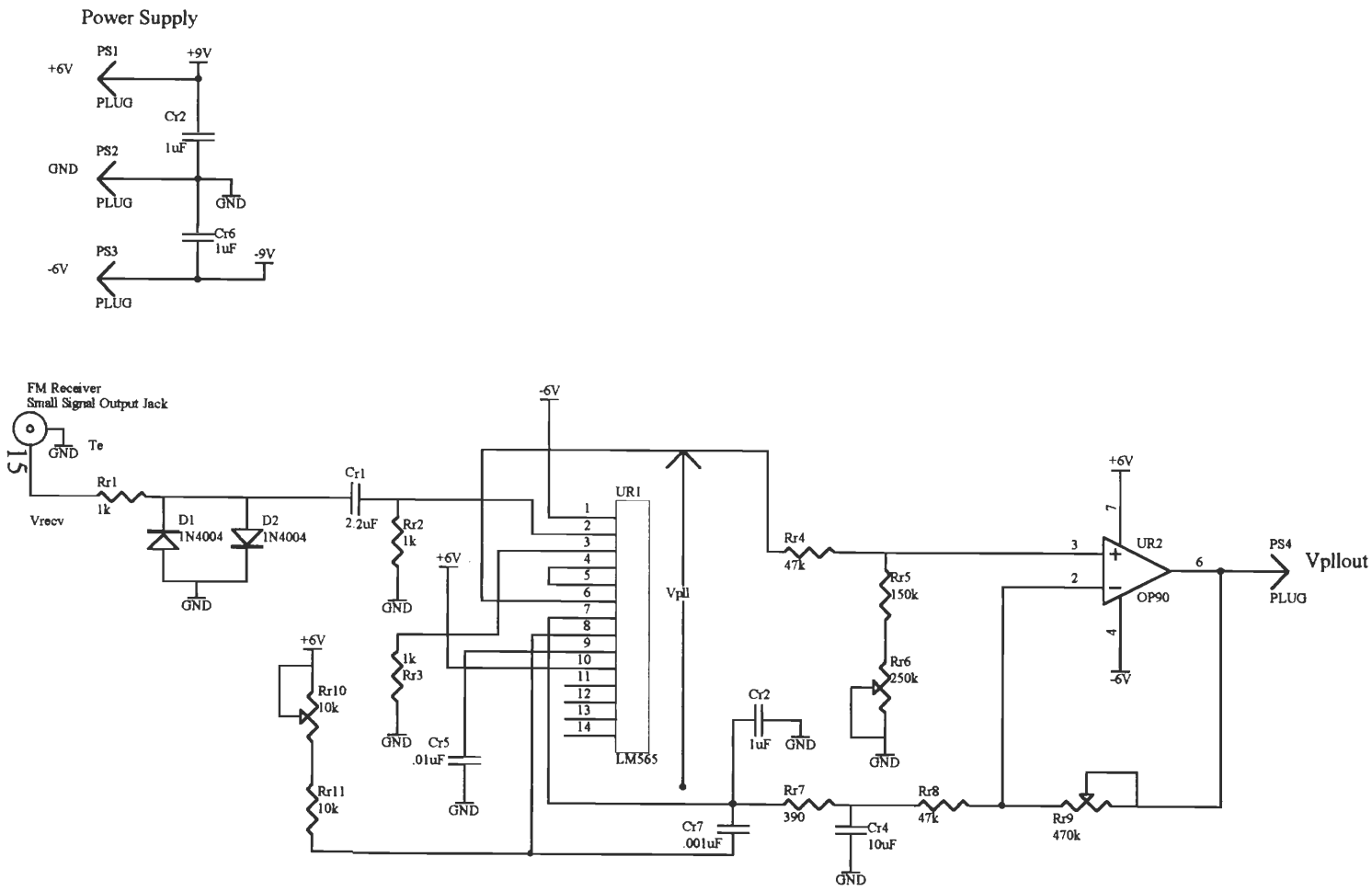


Figure 5

Title: Frequency Demodulator Circuit		
Size: A	Number:	Revision:
Date: 13-Apr-1997		Sheet of
File: C:\DATA\..\RCVR.SCH		Drawn By:

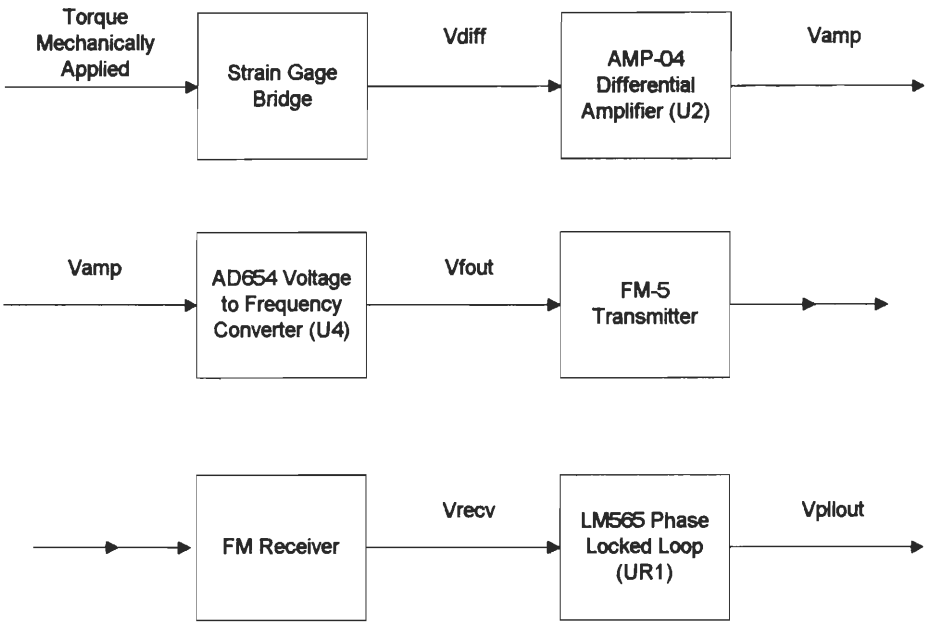


Figure 6 – Signal Flow Block Diagram

A signal timing diagram of the TTMS is shown in figure 7.

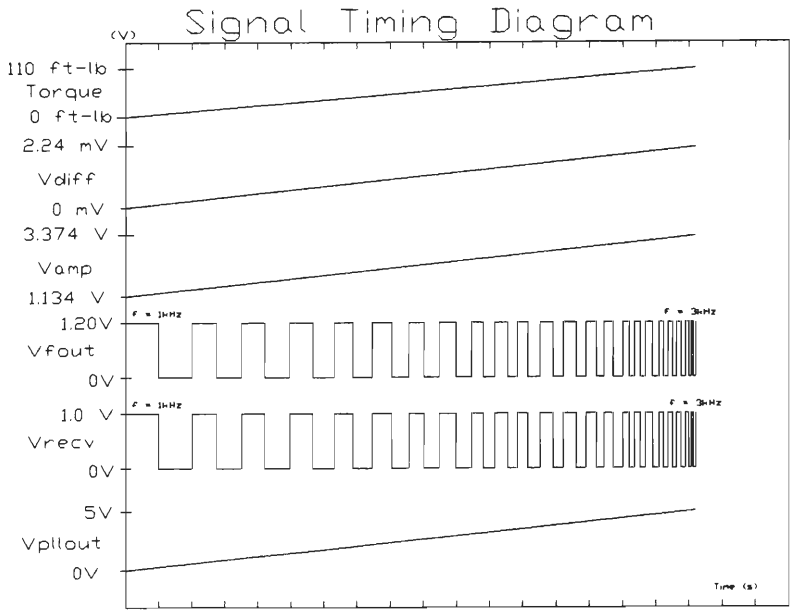


Figure 7 – Signal Timing Diagram

A JVC model RX555 FM receiver was used to receive the transmitted FM signal. The attached headphone jack was used as an output of the receiver to the frequency demodulator circuitry. The output of the receiver is an audio tone that contains the encoded torque signal. Two 9-Volt batteries are connected in series to give the frequency demodulator a ±9V power supply. The demodulator circuit uses a LM565 phase locked loop. The output of the LM565 is amplified using an OP90 operational amplifier, and potentiometers are used to adjust offset and gain. The output signal of the frequency demodulator is a voltage that is proportional to torque applied to the snowmobile shaft.

Several things were learned during the final phases of the TTMS project. After observing the output signal from the frequency demodulator, it was noticed that the gain of the TTMS was much too high to allow large changes in torque to be properly measured. The main problem became the phase locked loop's inability to lock on to frequencies in excess of 2.7kHz. This presented a problem, seeing that the original design

used frequencies ranging from 1kHz to 3kHz. For this reason, R_{GAIN} was changed to 800Ω. After the gain was adjusted, it was noticed that the phase locked loop would not lock on to frequencies that were near the edges of its operation. For this reason, the zero torque operating frequency was changed from 1kHz to 2kHz by changing the value of R_t. This allowed the phase locked loop to gain lock on power up without having to apply torque to the system to produce 2kHz and then remove the torque to begin testing. Although the overall sensitivity of the system was reduced, the TTMS gained the ability to measure bi-directional torque if the need should ever arise. These minor changes to the TTMS produced very desirable results, and are considered the final TTMS design. The original design specifications are fully detailed in the TTMS project proposal

TEST PROCEDURES AND RESULTS

A single printed circuit was fabricated and a housing was built to accommodate the transmitter section of the TTMS. The circuit board layout is shown in figure 8 and figure 9. A diagram of the TTMS housing is shown in figure 10. A line drawing of the TTMS mounting scheme is shown in figure 11. The testing procedure for the system is outlined below.

Test #1 – Breadboard Model of the TTMS

The purpose of this test was to test the operation of the TTMS design and determine any necessary circuit modifications. All voltages and frequencies were checked and compared to calculated values in each stage of the circuit.

- Potentiometers are used to simulate the strain gages.
- The TTMS was energized and the potentiometers were varied to produce a bridge output voltage ranging from 0mV to 2.24mV. The output voltage from the AMP04 and frequency output of the AD654 were measured and compared signal values as shown in figure 7.
- The output of the phase locked loop is monitored on an oscilloscope and the gain and offset controls of the frequency demodulator are adjusted to give –5V to +5V readings as the bridge output is varied from 0mV to 2.24mV.

TTMS Component Layout

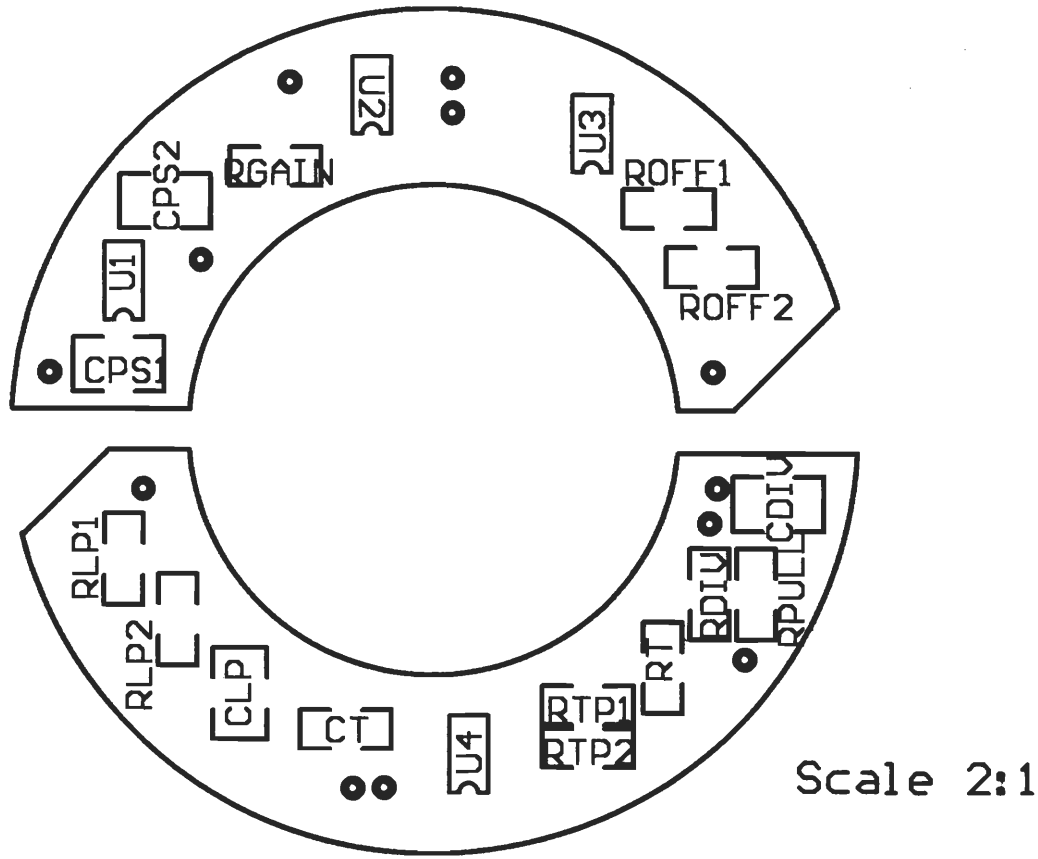
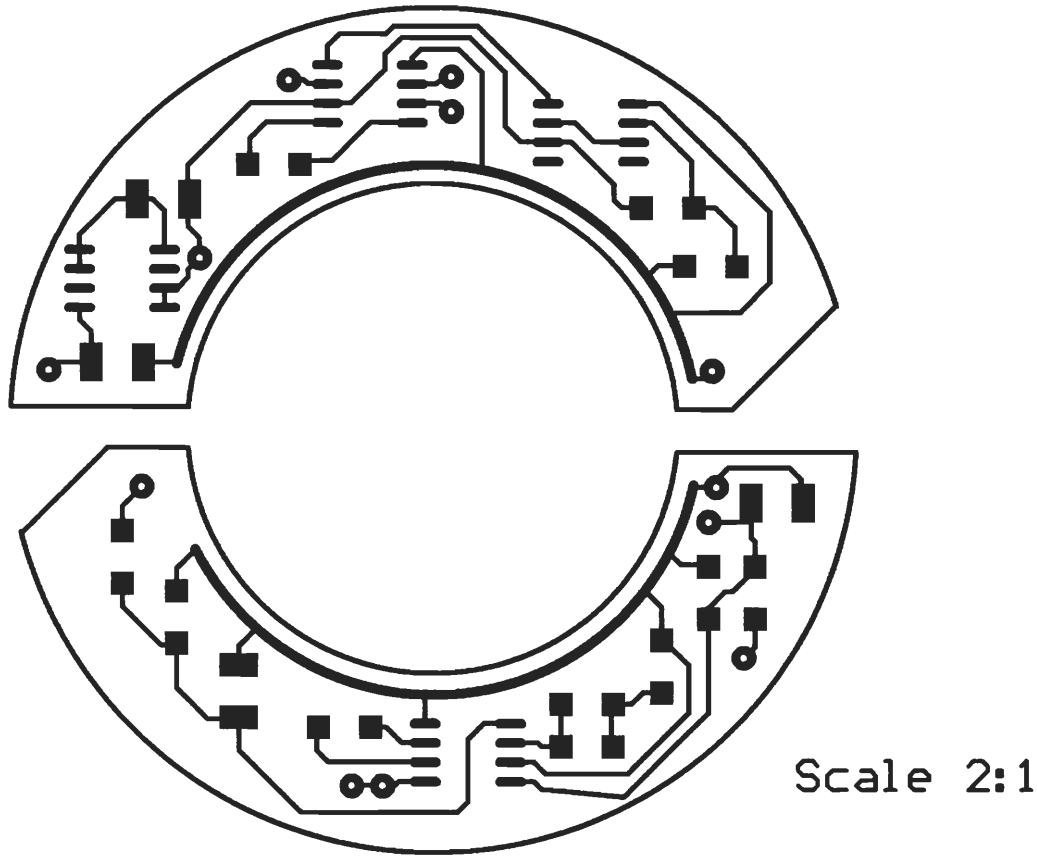


figure 8

TTMS Trace Layout



Scale 2:1

figure 9

TTMS Housing Diagram

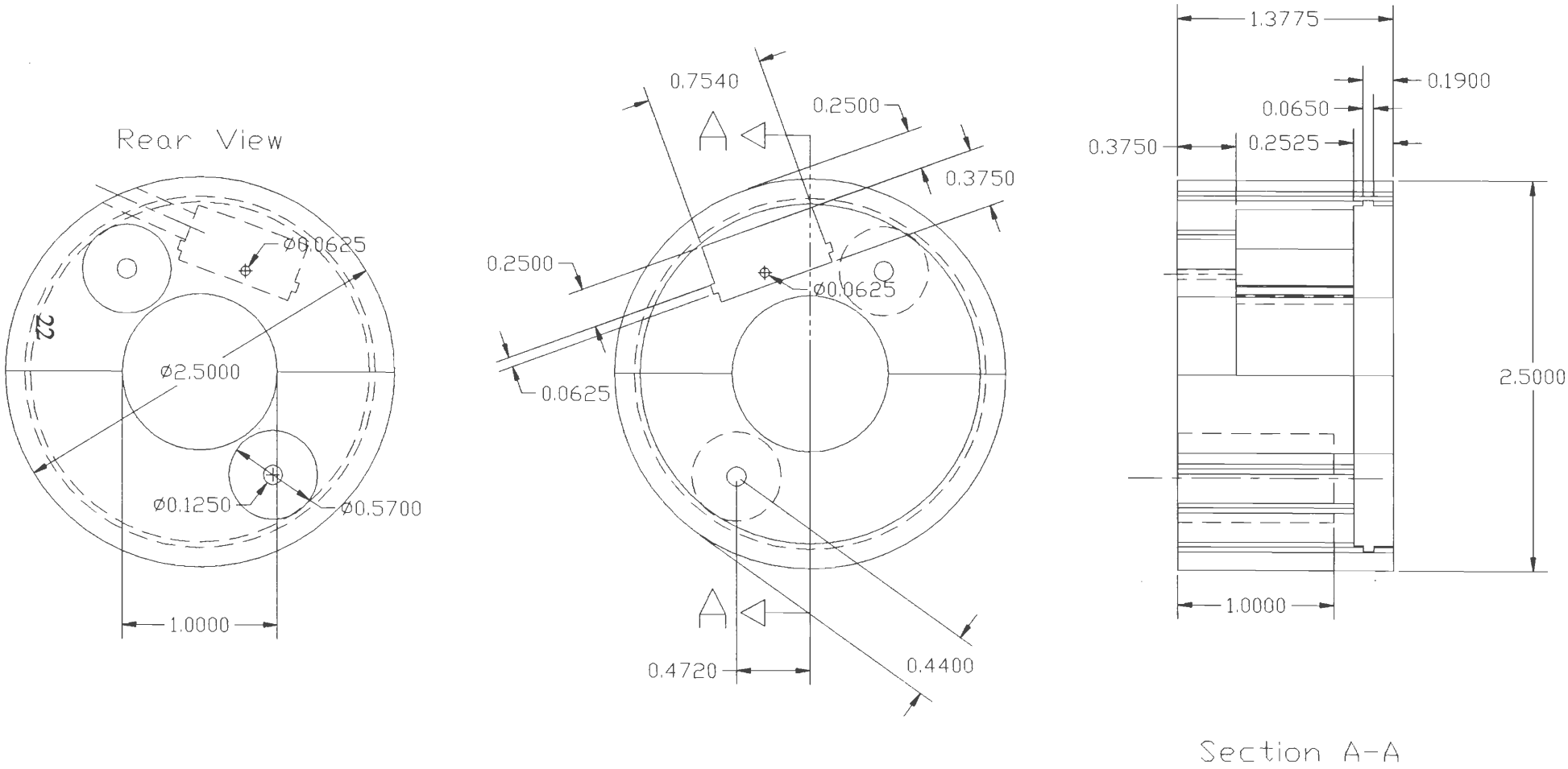
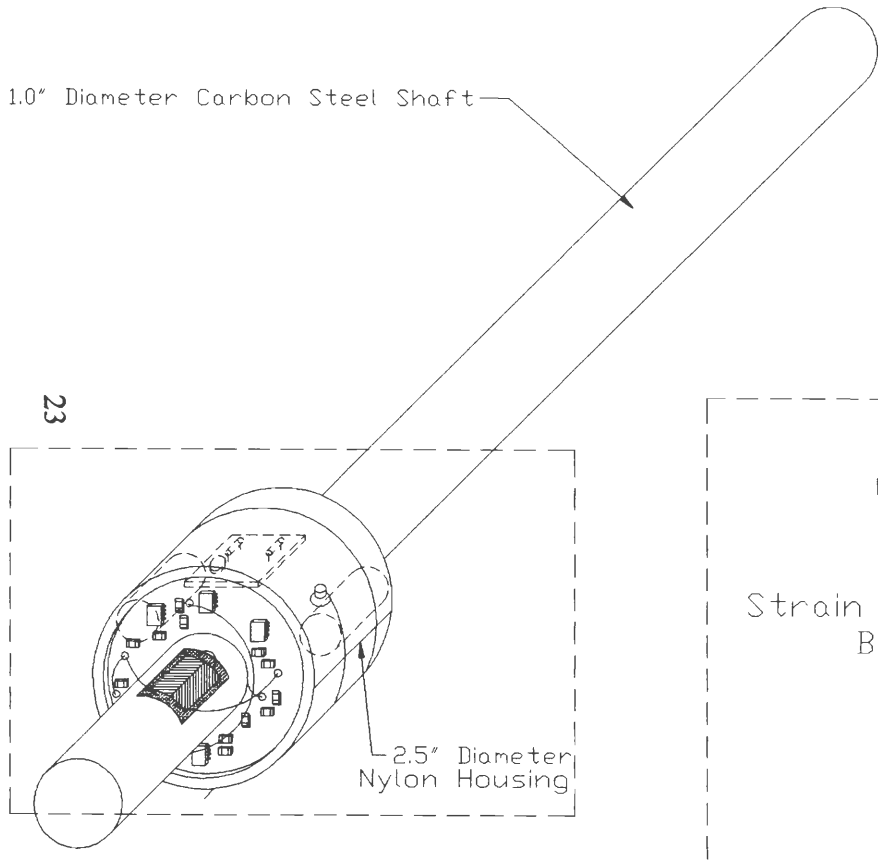


figure 10

Telemetric Torque Measurement System



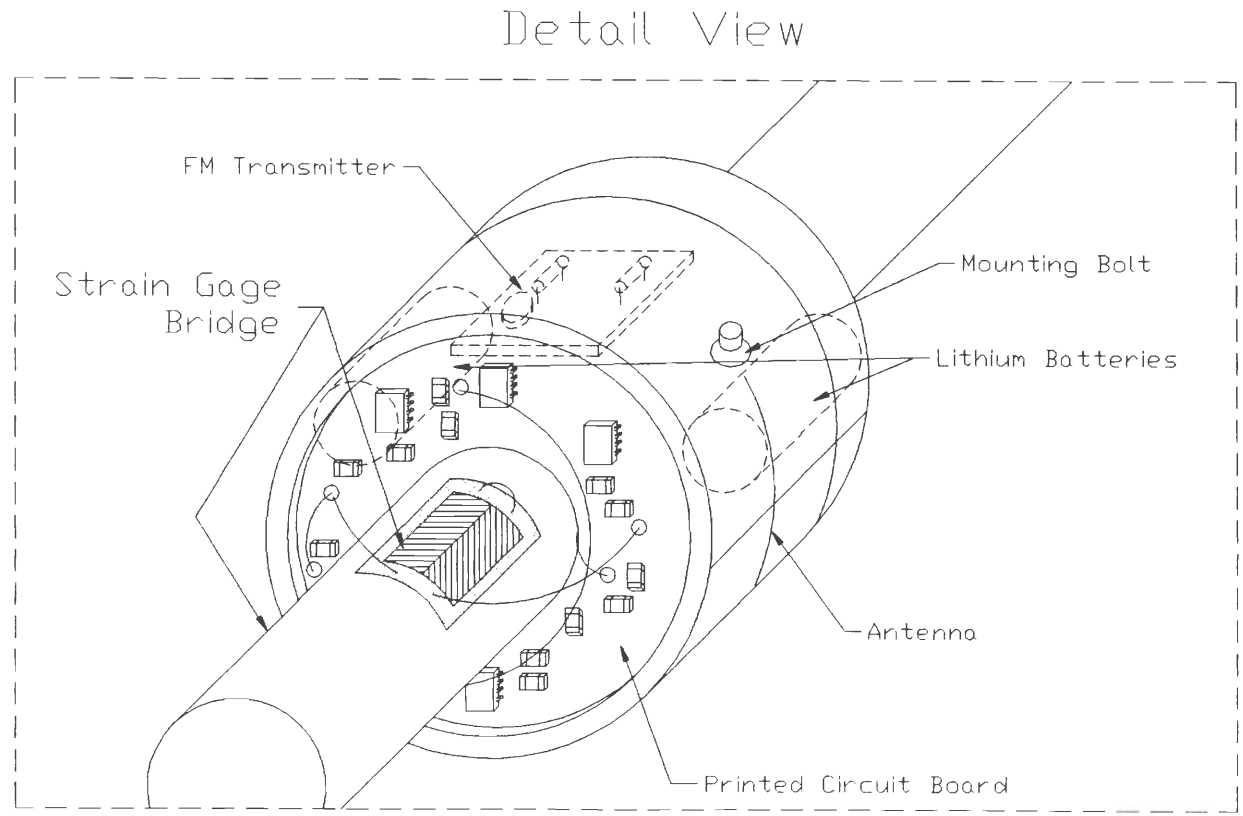


figure 11

Test #2 – Calibration Test

The purpose of this test is to calibrate the TTMS using known values of torque and verify the torque measurement ability of the TTMS.

- Strain gages were mounted on a 1" diameter carbon steel shaft.
- The TTMS was connected to the strain gages and energised
- Variable torque ranging from 0 to 110ft-lb in 10 ft-lb increments and output voltages from the frequency decoder (V_{pllout}) were recorded.

Test #3 – Battery Life Test

The purpose of this test was to determine the life of the batteries used in the TTMS.

- The TTMS and strain gages were mounted to a 1" diameter carbon steel shaft.
- The TTMS was energized and zero torque was applied to the shaft.
- The output of the frequency demodulator was monitored and the time until the circuit stopped operating was measured.

Test #4 – Rotation Test

The purpose of this test was to determine the ability of the TTMS to spin at high speeds and remain in tact.

- The TTMS and shaft were mounted on a lathe machine to incorporate spinning of the system.
- The shaft was rotated at 2000 RMP for at least one minute.

- The TTMS was removed and examined for mechanical failures and structural stability.

Test #5 – Operational Range Test

The purpose of this test was to verify the transmission ability of the TTMS to the stationary receiver at a distance greater than 10 feet.

- The receiver and frequency demodulator circuit were placed 15 feet away from the TTMS transmitter section.
- The TTMS was energized and the output of the frequency demodulator (V_{pllout}) was monitored for proper operation with different torque inputs.

The above tests were completed and the following results were obtained.

Test #1 Results

After the breadboard model was tested, it was determined that the circuit operated as expected. As the bridge voltage (V_{Diff}) was varied from 0mV to 2.24mV, V_{fout} was monitored and its frequency visually inspected. It was noted that when V_{Diff} was set to 0mV, the frequency of V_{fout} was approximately 2kHz. As V_{Diff} was increased to 2.24mV, the frequency of V_{fout} increased to approximately 2.5kHz. The output of the frequency demodulator (V_{pllout}) was also monitored as V_{Diff} was varied. It was noted that V_{pllout} changed from approximately 0V to +6V as V_{Diff} was varied.

Test #2 Results

The test data from the calibration test is shown in Table B1 in Appendix B. The average value of the three sets of test data was then plotted and is shown in figure 12.

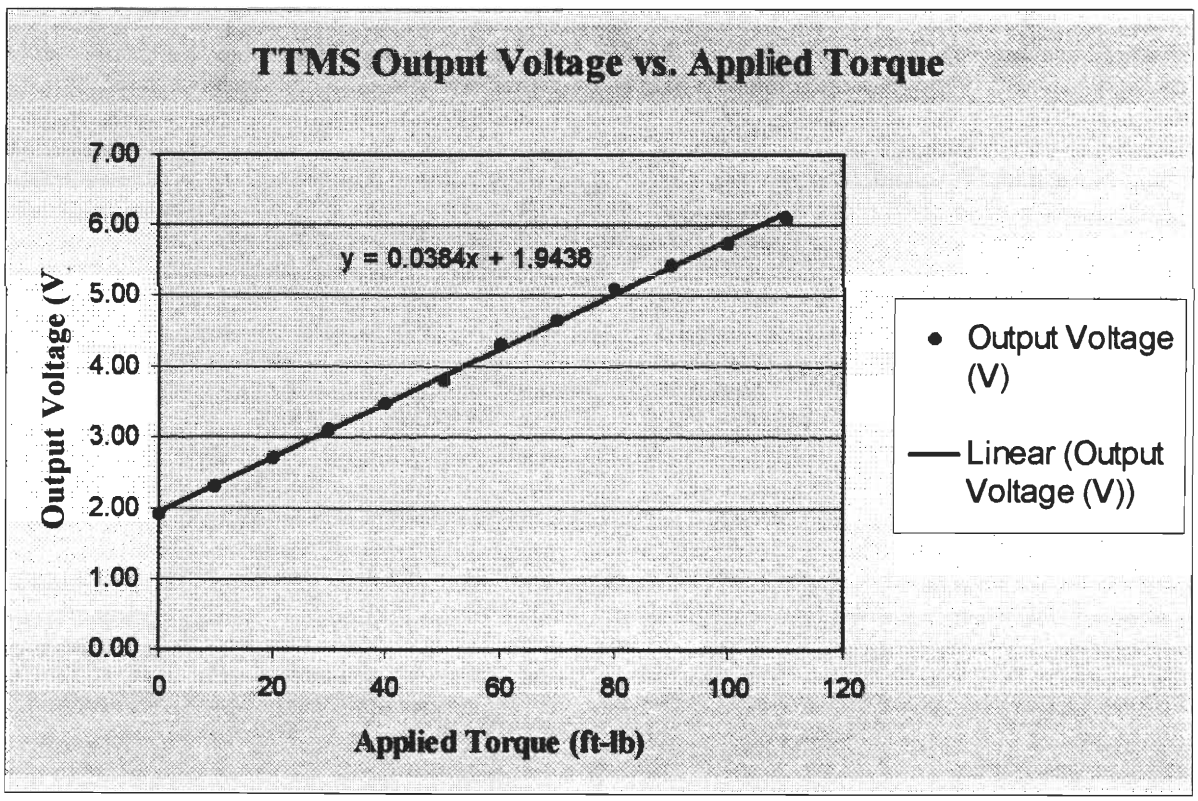


Figure 12 – Calibration Test Data

The calibration test data shows a linear relationship between torque applied to a shaft and V_{PllOut} from the TTMS. The offset in the curve at 1.94V is adjustable, and was set to 1.94V to verify that the phase locked loop was in lock at all times. The curve shows a slope of .0384. This constant relates the torque input to the voltage output of the TTMS, and can be used to measure torque on a 1" diameter shaft.

Test #3 Results

The battery life test was conducted. The two Lithium Ion batteries that powered the transmitter section of the TTMS lasted well over three hours. The test was not conducted until the circuit stopped functioning because of the limited supply of batteries available for testing. The FM transmitter batteries have continued to supply adequate power throughout the testing procedure. The two 9V batteries used for the frequency demodulator circuit lasted over six hours. The TTMS has a battery life greater than one hour, therefore, it meets the battery life specification.

Test #4 Results

The TTMS was mounted on a 1" diameter steel shaft and placed in a lathe machine. The machine was energized and the maximum speed was approximately 2000 RPM. The TTMS was allowed to spin for 1 minute and was then removed from the lathe. The circuit was examined for component failures and missing wire connections. All components and wires remained in tact, and no physical deterioration was noticed. Because of the limits of the test equipment, it is unknown whether or not the TTMS will function at speeds of up to 9000 RPM.

Test #5 Results

The operational range test was completed. The TTMS operated properly at a distance of 15 feet and registered voltage changes when different values of torque were

placed on the shaft. The TTMS meets specifications and operates properly at distances greater than 10 feet.

The TTMS meets many of the design specifications. Many of the specifications could not be tested because of equipment limitations and lack of equipment. The overall performance of the TTMS, however, was very satisfying. The TTMS accurately measures torque applied on a 1" diameter shaft, and produces a linear output that is proportional to torque applied.

Conclusion

The Telemetric Torque Measurement System (TTMS) was found to operate successfully. The TTMS is capable of measuring torque up to 110 ft-lb on a 1" diameter shaft. The overall size is within the allowable limits of the design specifications. The battery life of the TTMS is much greater than one hour. The TTMS operates properly at distances greater than 10 feet, and can rotate at high speeds. The test data (shown in Table B1 in Appendix B) shows that the TTMS produces a linear relationship between output voltage and input torque. Although several changes were made to component values of the TTMS during the testing phases, the overall system design remains unchanged.

By utilizing a zero torque center frequency at 2kHz and allowing positive and negative torque to be applied, the performance of the TTMS was much improved. Without centering the frequency of the voltage to frequency converter, the phase locked loop was unpredictable in its lock ability. The frequency must be centered for the phase locked loop to operate properly.

The gain of the instrumentation amplifier was also decreased to limit the voltage swing of the phase locked loop. As frequencies reached the outer limits of the phase locked loop's lock range, operation became unpredictable, and the phase locked loop occasionally was reset to zero volts output.

These modifications allowed the TTMS to meet design specifications in most areas. The calibration test showed a linear relationship between torque and output voltage that can be used for future measurements of unknown torque. The battery life of the

TTMS was much greater than required, and the mounting dimensions were within the limits specified in the design. Although the performance of the TTMS could not be tested at speeds greater than 2000 RPM, the solid nylon housing provided firm support for all internal components and there was no indication of fatigue or failure by any of the components.

Listed below are several suggestions for improving the performance of the TTMS.

- Improve the layout of the printed circuit board
  - Remove surface jumper wires and mount the batteries directly on the circuit board
  - Combine the FM transmitter and the existing printed circuit board on to one printed circuit board to save space and wiring hassles
- Reduce the size of the lithium ion batteries
- Improve the layout of the frequency demodulator circuit
  - Design and build a printed circuit board to house the components for the frequency demodulator section of the TTMS
- Improve the design of the FM transmitter
  - Improve transmission stability

Appendix A – Parts List

Table AI Parts List						
Qty	Component	Source	Description	Max Tolerance	Dimensions (in)	Cost ea ($)
2	LS14250	Avex	Lithium Battery	N/A	.571D X .98L	$6.00
1	AD666AR-8	Analog Devices	Voltage Regulator	N/A	.244W X .197L X .102H	$0.52
1	AMP04SO-8	Analog Devices	Instrumentation Amplifier	N/A	.244W X .197L X .102H	$0.82
2	EA-06-250TK-10C	Micro-Measurements	Strain Gage	N/A	.74L X .55W	$19.40
2	OP-90GS	Analog Devices	Operational Amplifier	N/A	.244W X .197L X .102H	$0.52
1	AD654JR	Analog Devices	Voltage to Frequency Converter	N/A	.244W X .197L X .102H	$0.68
1	FM-5	Ramsey Electronics	FM Transmitter Kit	N/A	.75W X .8 L X .375H	$20.00
1	PCB	Stock	Printed Circuit Board	N/A	N/A	$50.00
1	LM565CN	National Semiconductor	Phase Locked Loop IC	N/A	.25W X .74L X .145H	$2.00
2	1N4004	Stock	Diode	N/A	1/4 Watt Package	$0.10
1	10kΩ Pot	Stock	10k Potentiometer	N/A	N/A	$0.37
1	250kΩ Pot	Stock	250k Potentiometer	N/A	N/A	$0.42
1	470kΩ Pot	Stock	470k Potentiometer	N/A	N/A	$0.35
2	1uF Chip Cap	Stock	1uF Surface Mount Cap (10V)	20%	N/A	$0.12
1	.33uF Chip Cap	Stock	.33uF Surface Mount Cap (10V)	1%	N/A	$0.18
1	15k Chip Res	Stock	15k Surface Mount Res (1/4 W)	1%	1/4 Watt Package	$0.08
1	10uF Cap	Stock	10uF Ceramic Cap (10V)	20%	N/A	$0.15
3	1uF Cap	Stock	1uF Ceramic Cap (10V)	20%	N/A	$0.12
1	2.2uF Cap	Stock	2.2uF Ceramic Cap (10V)	20%	N/A	$0.15
1	.01uF Cap	Stock	.01uF Mylar Wrap Cap (10V)	1%	N/A	$0.19
1	.001uF Cap	Stock	.001uF Ceramic Cap (10V)	20%	N/A	$0.08
2	1k Res	Stock	1k Res (1/4 Watt)	10%	1/4 Watt Package	$0.06
2	47k Res	Stock	47k Res (1/4 Watt)	10%	1/4 Watt Package	$0.06
1	150k	Stock	150k Res (1/4 Watt)	10%	1/4 Watt Package	$0.12
1	390 Res	Stock	390 Res (1/4 Watt)	10%	1/4 Watt Package	$0.06
1	178 Chip Res	Stock	178 Res (1/4 Watt) Surface Mount	10%	1/4 Watt Package	$0.18
1	51.1k Chip Res	Stock	51.1k Res (1/4 Watt) Surface Mount	1%	1/4 Watt Chip Resistor	$0.18
1	14.7k Chip Res	Stock	14.7k Res (1/4 Watt) Surface Mount	1%	1/4 Watt Chip Resistor	$0.18
1	910 Chip Res	Stock	100 Res (1/4 Watt) Surface Mount	5%	1/4 Watt Chip Resistor	$0.18
1	422 Chip Res	Stock	422 Res (1/4 Watt) Surface Mount	5%	1/4 Watt Chip Resistor	$0.18
1	1k Chip Res	Stock	1k Res (1/4 Watt) Surface Mount	5%	1/4 Watt Chip Resistor	$0.18
1	10k Chip Res	Stock	10k Res (1/4 Watt) Surface Mount	1%	1/4 Watt Chip Resistor	$0.18
1	174 Chip Res	Stock	174 Res (1/4 Watt) Surface Mount	1%	1/4 Watt Chip Resistor	$0.18
1	.5uF Chip Cap	Stock	.5uF Cap (10V) Surface Mount	20%	N/A	$0.22
1	.68uF Chip Cap	Stock	.68uF Cap (10V) Surface Mount	20%	N/A	$0.25
					Total Cost	**$104.46**

Note: Parts Designated as "Stock" are stocked in Smiths Industries inventory. Package sizes and tolerances may vary based on supplies.

Appendix B – Test Data

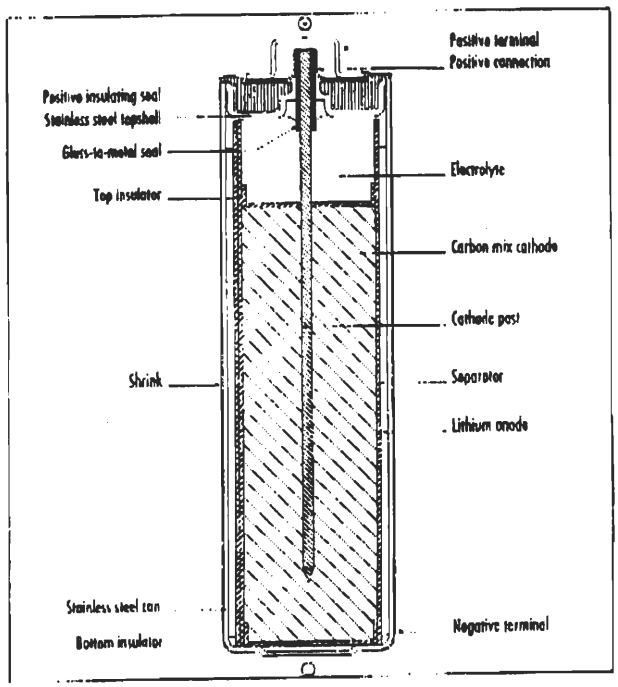
Table BI - Calibration Test Data				
Applied Torque (ft-lb)	Output Voltage (V) Run #1	Output Voltage (V) Run #1	Output Voltage (V) Run #1	**Average Output Voltage (V)**
0	1.90	2.00	1.88	1.93
10	2.28	2.32	2.31	2.30
20	2.66	2.75	2.72	2.71
30	3.17	3.09	3.07	3.11
40	3.60	3.48	3.37	3.48
50	3.90	3.77	3.73	3.80
60	4.40	4.35	4.22	4.32
70	4.70	4.67	4.56	4.64
80	5.10	5.17	4.96	5.08
90	5.60	5.48	5.21	5.43
100	5.90	5.76	5.61	5.76
110	6.18	6.14	5.95	6.09

Appendix C – LS14250 Lithium Ion Battery

Supplied by House of Batteries
16512 Burke Lane
Huntington Beach, CA 92647
(800) 432-3385

Saft 3.6 V low rate system: LS small size series

All-round production automation of the Saft LS small size series cells delivers a high-reliability, cost-effective solution. LS cells feature a high operating voltage (3.6 V), wide operating temperature range (- 55°/+ 100 °C) and very high energy-density of up to 900 Wh/dm³. Their lack of toxic materials, low pressure system and reliable glass-to-metal feedthrough all guarantee safe operation. In fact, Saft LS cells offer designers not just a better power source, but often their only viable solution.



Chemistry
Anode: lithium (Li)
Cathode: thionyl chloride ($SOCl_2$)
Electrolyte: lithium tetrachloro aluminate in thionyl chloride

Electrochemical reaction
$4\ Li + 2\ SOCl_2 \rightarrow 4\ LiCl + SO_2 + S$

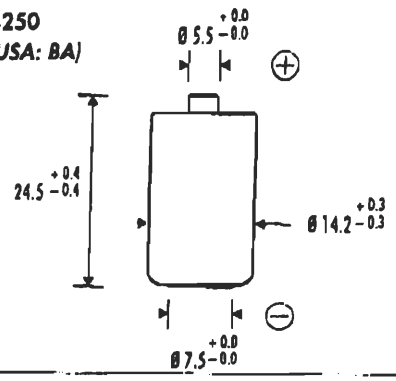
Design
Cell electrode: bobbin construction
Container material: stainless steel
Sealing system: glass-to-metal feedthrough
Safety system: venting

Cell		LS14250	LS14500	LS 9 V**
Size	IEC	1/2R6	R6	-
	ANSI	1/2AA	AA	-
Electrical features		**LS14250**	**LS14500**	**LS 9 V**
Nominal capacity at C/700/20°C/68°F/2.0 V cut off	Ah	0.95	2.1	0.95
Open circuit voltage (at 20°C/68°F)	volts	3.67	3.67	11.0
Nominal voltage at C/700/20°C/68°F	volts	3.5	3.5	10.6
Maximum recommended constant current (50% yield) at 20°C/68°F	mA	35	70	35
Temperature		**LS14250**	**LS14500**	**LS 9 V**
Operating*	°C	-55/+85*	-55/+85*	-40/+85
	°F	-67/+185*	-67/+185*	-40/+185
Storage	°C	-55/+85	-55/+85	-40/+85
	°F	-67/+185	-67/+185	-40/+185
Physical features		**LS14250**	**LS14500**	**LS 9 V**
Diameter (max) or l x l	mm	14.5	14.5	26.5 x 17.3
	in	0.571	0.571	1.043 x 0.68
Height (max)	mm	24.9	50.4	48.6
	in	0.980	1.984	1.913
Weight	g	7.5	15.0	33.5
	oz	0.26	0.525	1.172
References		**LS14250**	**LS14500**	**LS 9 V**
UL Recognition		•	•	•

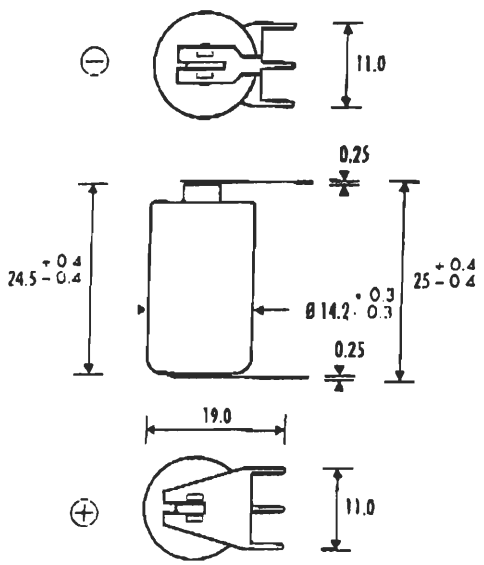
* 100 °C/212 °F possible for short periods of time
** LS 9 V D: version with diode

Available models of LS small size cells (dimensions in mm are for sleeved and labelled cells)

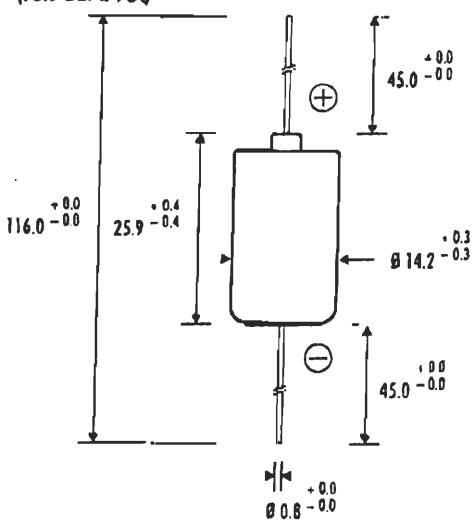
LS 14250
(ref. USA: BA)



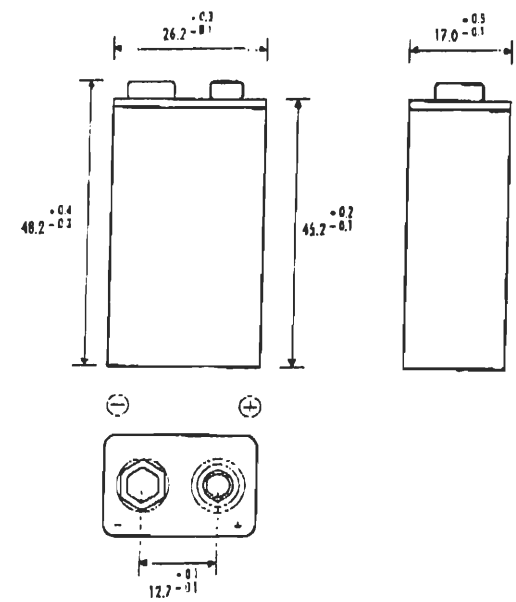
LS 14250 3PF
(ref. USA: 3PF)



LS 14250 CNA
(ref. USA: AX)

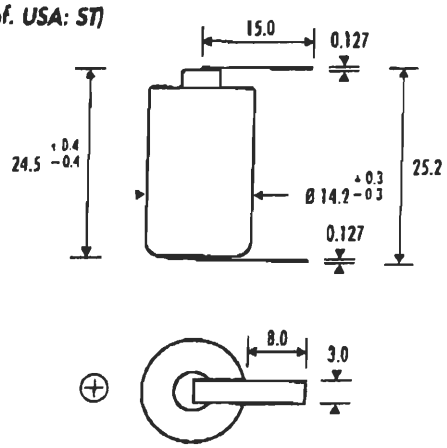


LS 9 V/LS 9 VD



Rigid plastic cased

LS 14250 CNR
(ref. USA: ST)

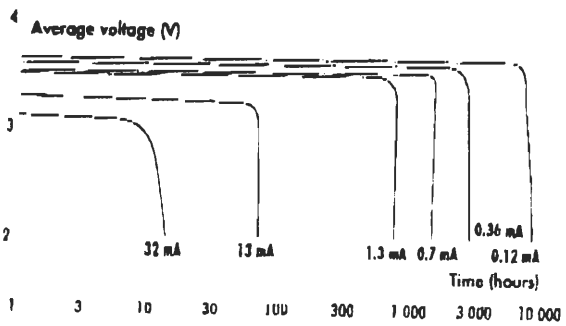


(For other terminals, please contact Saft)

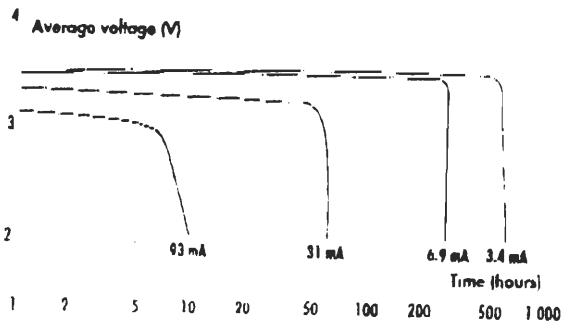
C-2

Typical discharge curves of LS batteries

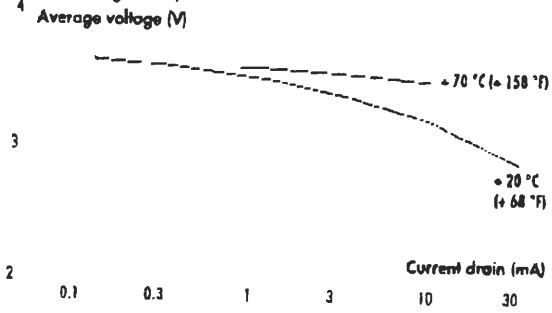
LS 14250 Discharge profiles at + 20 °C (68 °F)



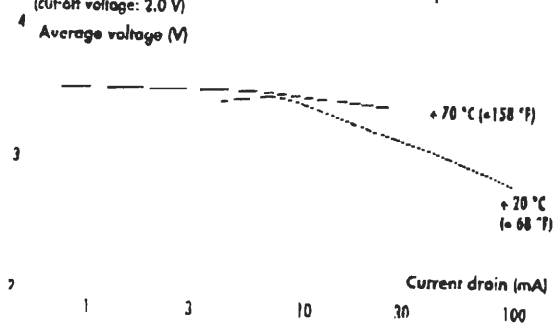
LS 14500 Discharge profiles at + 20 °C (68 °F)



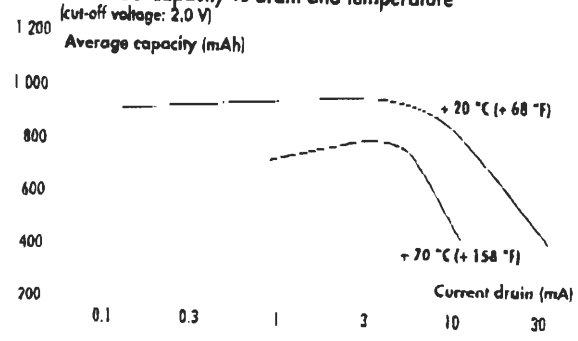
LS 14250 Operating voltage vs drain and temperature
(cut-off voltage: 2.0 V)



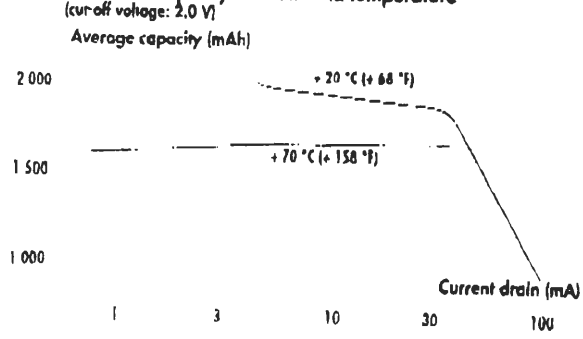
LS 14500 Operating voltage vs drain and temperature
(cut-off voltage: 2.0 V)



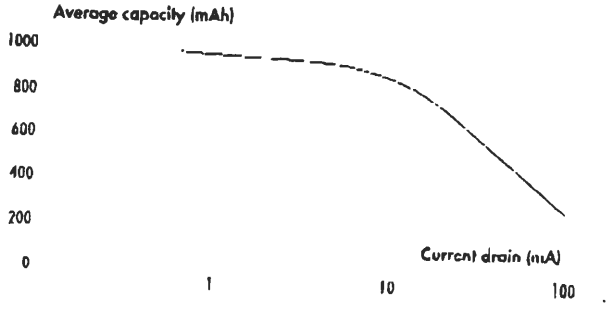
LS 14250 Capacity vs drain and temperature
(cut-off voltage: 2.0 V)



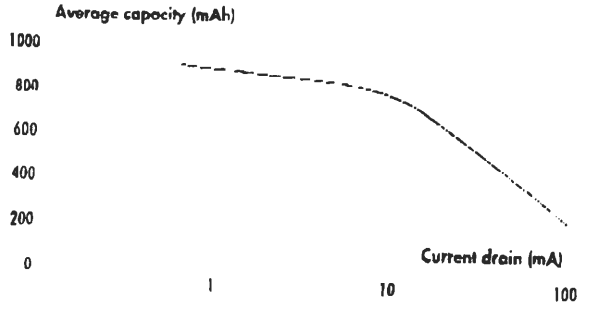
LS 14500 Capacity vs drain and temperature
(cut-off voltage: 2.0 V)



LS 9 V Capacity vs drain at + 20 °C (68 °F)
(cut-off voltage: 5.0 V)



LS 9 VD Capacity vs drain at + 20 °C (68 °F)
(cut-off voltage: 5.0 V)



Appendix D – EA-06-250TK-10C Strain Gages

Manufactured by Micro Measurements
P.O. Box 27777
Raleigh, NC 27611
(919) 365-3800

2.0 Gage Selection Parameters

2.1 Strain-Sensing Alloys

The principal component which determines the operating characteristics of a strain gage is the strain-sensitive alloy used in the foil grid. However, the alloy is not in every case an independently selectable parameter. This is because each Micro-Measurements strain gage series (identified by the first two, or three, letters in the alphanumeric gage designation — see diagram on page 11) is designed as a complete system. That system is comprised of a particular foil and backing combination, and usually incorporates additional gage construction features (such as encapsulation, integral leadwires, or solder dots) specific to the series in question.

Micro-Measurements supplies a variety of strain gage alloys as follows (with their respective letter designations):

A: Constantan in self-temperature-compensated form.

P: Annealed constantan.

D: Isoelastic.

K: Nickel-chromium alloy, a modified Karma in self-temperature-compensated form.

2.1.1 Constantan Alloy

Of all modern strain gage alloys, constantan is the oldest, and still the most widely used. This situation reflects the fact that constantan has the best overall combination of properties needed for many strain gage applications. This alloy has, for example, an adequately high strain sensitivity, or gage factor, which is relatively insensitive to strain level and temperature. Its resistivity is high enough to achieve suitable resistance values in even very small grids, and its temperature coefficient of resistance is not excessive. In addition, constantan is characterized by good fatigue life and relatively high elongation capability. It must be noted, however, that constantan tends to exhibit a continuous drift at temperatures above +150°F *(+65°C)*; and this characteristic should be taken into account when zero stability of the strain gage is critical over a period of hours or days.

Very importantly, constantan can be processed for self-temperature compensation (see box at right) to match a wide range of test material expansion coefficients. Micro-Measurements A alloy is a self-temperature-compensated form of constantan. A alloy is supplied in self-temperature-compensation (S-T-C) numbers 00, 03, 05, 06, 09, 13, 15, 18, 30, 40 and 50, for use on test materials with corresponding thermal expansion coefficients (expressed in ppm/°F).

For the measurement of very large strains, 5% (50 000$\mu\epsilon$) or above, annealed constantan (P alloy) is the grid material normally selected. Constantan in this form is very ductile; and, in gage lengths of 0.125 in *(3 mm)* and longer, can be strained to >20%. It should be borne in mind, however, that under high *cyclic* strains the P alloy will exhibit some permanent resistance change with each cycle, and cause a corresponding zero shift in the strain gage. Because of this characteristic, and the tendency for premature grid failure with repeated straining, P alloy is not ordinarily recommended for cyclic strain applications. P alloy is available with S-T-C numbers of 08 and 40 for use on metals and plastics, respectively.

2.1.2 Isoelastic Alloy

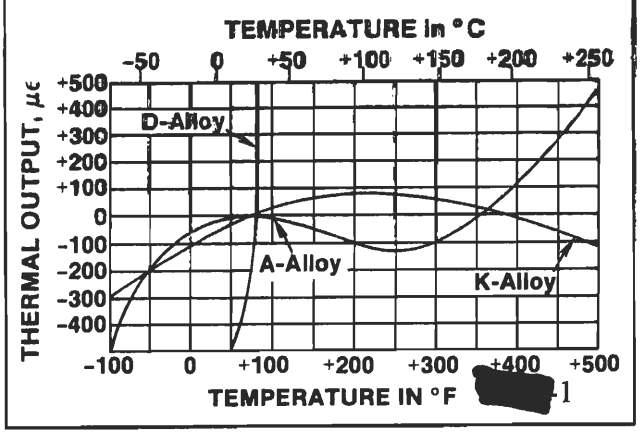
When purely dynamic strain measurements are to be made — that is, when it is not necessary to maintain a stable reference zero — isoelastic (D alloy) offers certain advantages. Principal among these are superior fatigue life, compared to A alloy, and a high gage factor (approximately 3.2) which improves the signal-to-noise ratio in dynamic testing.

Self-Temperature Compensation

An important property shared by constantan and modified Karma strain gage alloys is their responsiveness to special processing for self-temperature compensation. Self-temperature-compensated strain gages are designed to produce minimum thermal output (temperature-induced apparent strain) over the temperature range from about –50° to +400°F *(–45° to +200°C)*. When selecting either constantan (A-alloy) or modified Karma (K-alloy) strain gages, the self-temperature-compensation (S-T-C) number must be specified. The S-T-C number is the approximate thermal expansion coefficient in ppm/°F of the structural material on which the strain gage will display minimum thermal output.

The accompanying graph illustrates typical thermal output characteristics for A and K alloys. The thermal output of uncompensated isoelastic alloy is included in the same graph for comparison purposes. In normal practice, the S-T-C number for an A- or K-alloy gage is selected to most closely match the thermal expansion coefficient of the test material. However, the thermal output curves for these alloys can be rotated about the room-temperature reference point to favor a particular temperature range. This is done by intentionally mismatching the S-T-C number and the expansion coefficient in the appropriate direction. When the selected S-T-C number is lower than the expansion coefficient, the curve is rotated counterclockwise. An opposite mismatch produces clockwise rotation of the thermal output curve. Under conditions of S-T-C mismatch, the thermal output curves for A and K alloys (supplied with each package of strain gages) do not apply, of course, and it will generally be necessary to calibrate the installation for thermal output as a function of temperature.

For additional information on strain gage temperature effects, see Measurements Group Tech Note TN-504.



D-1

suring strains in a concrete structure it is ordinarily desirable to use a strain gage of sufficient gage length to span several pieces of aggregate in order to measure the representative strain in the structure. In other words, it is usually the *average* strain that is sought in such instances, not the severe local fluctuations in strain occurring at the interfaces between the aggregate particles and the cement. In general, when measuring strains on structures made of composite materials of any kind, the gage length should normally be large with respect to the dimensions of the inhomogeneities in the material.

As a generally applicable guide, when the foregoing considerations do not dictate otherwise, gage lengths in the range from 0.125 to 0.25 in *(3 to 6 mm)* are preferable. The largest selection of gage patterns and stock gages is available in this range of lengths. Furthermore, larger or smaller sizes generally cost more, and larger gages do not noticeably improve fatigue life, stability, or elongation, while shorter gages are usually inferior in these characteristics.

2.5 Gage Pattern

The gage pattern refers cumulatively to the shape of the grid, the number and orientation of the grids in a multiple-grid gage, the solder tab configuration, and various construction features which are standard for a particular pattern. All details of the grid and solder tab configurations are illustrated in the "Gage Pattern" columns of Catalog 500. The wide variety of patterns in the list is designed to satisfy the full range of normal gage installation and strain measurement requirements.

With single-grid gages, pattern suitability for a particular application depends primarily on the following:

Solder tabs — These should, of course, be compatible in size and orientation with the space available at the gage installation site. It is also important that the tab arrangement be such as to not excessively tax the proficiency of the installer in making proper leadwire connections.

Grid width — When severe strain gradients perpendicular to the gage axis exist in the test specimen surface, a narrow grid will minimize the averaging error. Wider grids, when available and suitable to the installation site, will improve the heat dissipation and enhance gage stability — particularly when the gage is to be installed on a material or specimen with poor heat transfer properties.

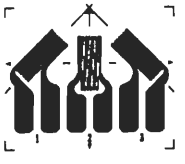
Gage resistance — In certain instances, the only difference between two gage patterns available in the same series is the grid resistance — typically 120 ohms vs. 350 ohms. When the choice exists, the higher-resistance gage is preferable in that it reduces the heat generation rate by a factor of three (for the same applied voltage across the gage). Higher gage resistance also has the advantage of decreasing leadwire effects such as circuit desensitization due to leadwire resistance, and unwanted signal variations caused by leadwire resistance changes with temperature fluctuations. Similarly, when the gage circuit includes switches, slip rings, or other sources of random resistance change, the signal-to-noise ratio is improved with higher resistance gages operating at the same power level.

In experimental stress analysis, a single-grid gage would normally be used only when the stress state at the point of measurement is known to be uniaxial and the directions of the principal axes are known with reasonable accuracy (±5°).

These requirements severely limit the meaningful applicability of single-grid strain gages in stress analysis; and failure to consider biaxiality of the stress state can lead to large errors in the stress magnitude inferred from measurements made with a single-grid gage.

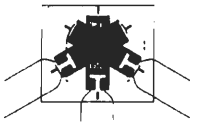

90-degree rosette

For a biaxial stress state — a common case necessitating strain measurement — a two- or three-element rosette is required in order to determine the principal stresses. When the directions of the principal axes are known in advance, a two-element 90-degree (or "tee") rosette can be employed with the gage axes aligned to coincide with the principal axes. The directions of the principal axes can sometimes be determined with sufficient accuracy from one of several considerations. For example, the shape of the test object and the mode of loading may be such that the directions of the principal axes are obvious from the symmetry of the situation, as in a cylindrical pressure vessel. The principal axes can also be defined by testing with photoelastic coatings.


45-degree rosette


60-degree rosette

In the most general case of surface stresses, when the directions of the principal axes are not known from other considerations, a three-element rosette must be used to obtain the principal stress magnitudes. The rosette can be installed with any orientation, but is usually mounted so that one of the grids is aligned with some significant axis of the test object. Three-element rosettes are available in both 45-degree rectangular and 60-degree delta configurations. The usual choice is the rectangular rosette since the data-reduction task is somewhat simpler for this configuration.


Stacked rosette

When a rosette is to be employed, careful consideration should always be given to the difference in characteristics between single-plane and stacked rosettes. For any given gage length, the single-plane rosette is superior to the stacked rosette in terms of heat transfer to the test specimen, generally providing better stability and accuracy for static strain measurements. Furthermore, when there is a significant strain gradient perpendicular to the test surface (as in bending), the single-plane rosette will produce more accurate strain data because all grids are as close as possible to the test surface. Still another consideration is that stacked rosettes are generally less conformable to contoured surfaces than single-plane rosettes.

On the other hand, when there are large strain gradients in the plane of the test surface, as is often the case, the single-plane rosette can produce errors in strain indication because the grids sample the strain at different points. For these applications the stacked rosette is ordinarily preferable. The stacked rosette is also advantageous when the space for mounting the rosette is limited.

Super Stock Gage Listings Section

GAGE DESIGNATION AND PATTERN

EA-XX-125BT-120

General-purpose pattern with narrow grid and compact geometry.

2X

EA-XX-125BZ-350

Narrow high-resistance pattern with compact geometry.

2X

EA-XX-125RA-120

General-purpose 3-element 45° rectangular rosette. Compact geometry.

CEA-XX-125UR-120
CEA-XX-125UR-350

General-purpose 45° single-plane rosette. Compact geometry. Exposed tab area is 0.08 x 0.06 in *(2.0 x 1.5 mm)*.

EA-XX-125TM-120

General-purpose 2-element 90° 'tee' rosette. Sections are electrically independent.

CEA-XX-125UT-120
CEA-XX-125UT-350

2-element 90° 'tee' rosette for general-purpose use. Exposed tab area is 0.10 x 0.07 in *(2.5 x 1.8 mm)*.

EA-XX-125TK-350

High-resistance 2-element 90° gage for torque applications.

EA-06-250TK-10C

GAGE DESIGNATION AND PATTERN

CEA-XX-187UV-120
CEA-XX-187UV-350

2-element 90° rosette for torque and shear-strain measurements. Sections have a common electrical connection. Exposed tab area is 0.13 x 0.06 in *(3.3 x 2.0 mm)*.

EA-XX-250AE-350

Large general-purpose gage. Used when high power-dissipation is required.

EA-XX-250AF-120

Large general-purpose gage. Used when high power-dissipation is required.

EA-XX-250BG-120
EP-08-250BG-120
WA-XX-250BG-120
WK-XX-250BG-350

Widely used general-purpose pattern. EP Series capable of elongation > 20%.

EA-XX-250BF-350

General-purpose pattern with high-resistance grid. Compact geometry. Similar to 250BG pattern except for resistance.

CEA-XX-250UN-120
CEA-XX-250UN-350

Narrow general-purpose gage pattern. Exposed tab area is 0.08 x 0.05 in *(2.0 x 1.1 mm)*.

CEA-XX-250UW-120
CEA-XX-250UW-350

Larger grid and tab than 250UN pattern. Exposed tab area is 0.10 x 0.07 in *(2.5 x 1.8 mm)*.

GAGE DESIGNATION AND PATTERN

EA-XX-250BK-10C

Very high-resistance (1000Ω) pattern. Recommended for high bridge voltages or for use on plastics.

CEA-06-W250A-120
CEA-06-W250A-350

Lowest-cost, most flexible and conformable linear weldable gage pattern. See page 8 for more details.

CEA-XX-250UR-120
CEA-XX-250UR-350

Large 3-element 45° single-plane rosette. Exposed tab area is 0.13 x 0.08 in *(3.3 x 2.0 mm)*.

EA-XX-500BH-120

Long general-purpose gage in a compact geometry.

CEA-XX-500UW-120

Widely used long gage pattern. Exposed tab area is 0.10 x 0.07 in *(2.5 x 1.8 mm)*.

-3

D-3

Standard Strain Gage Series Selection Chart

EA	Constantan foil in combination with a tough, flexible, polyimide backing. Wide range of options available. Primarily intended for general-purpose static and dynamic stress analysis. Not recommended for highest accuracy transducers.	Normal: –100° to +350°F *(–75° to +175°C)* Special or Short-Term: –320° to +400°F *(–195° to +205°C)*	±3% for gage lengths under 1/8 in *(3.2 mm)* ±5% for 1/8 in and over	±1800 ±1500 ±1200	10^5 10^6 10^8
CEA	Universal general-purpose strain gages. Constantan grid completely encapsulated in polyimide, with large, rugged copper-coated tabs. Primarily used for general-purpose static and dynamic stress analysis. 'C'-Feature gages are specially highlighted throughout the gage listings of Catalog 500.	Normal: –100° to +350°F *(–75° to +175°C)* Stacked rosettes limited to +150°F *(+65°C)*	±3% for gage lengths under 1/8 in *(3.2 mm)*; ±5% for 1/8 in and over	±1500 ±1500	10^5 10^6*
				*Fatigue life improved using low-modulus solder.	
N2A	Open-faced constantan foil gages with a thin, laminated, polyimide-film backing. Primarily recommended for use in precision transducers, the N2A Series is characterized by low and repeatable creep performance. Also recommended for stress analysis applications employing large gage patterns, where the especially flat matrix eases gage installation.	Normal Static Transducer Service: –100° to +200°F *(–75° to +95°C)*	±3%	±1700 ±1500	10^6 10^7
WA	Fully encapsulated constantan gages with high-endurance leadwires. Useful over wider temperature ranges and in more extreme environments than EA Series. Option W available on some patterns, but restricts fatigue life to some extent.	Normal: –100° to +400°F *(–75° to +205°C)* Special or Short-Term: –320° to +500°F *(–195° to +260°C)*	±2%	±2000 ±1800 ±1500	10^5 10^6 10^7
SA	Fully encapsulated constantan gages with solder dots. Same matrix as WA Series. Same uses as WA Series but derated somewhat in maximum temperature and operating environment because of solder dots.	Normal: –100° to +400°F *(–75° to +205°C)* Special or Short-Term: –320° to +450°F *(–195° to +230°C)*	±2%	±1800 ±1500	10^6 10^7
EP	Specially annealed constantan foil with tough, high-elongation polyimide backing. Used primarily for measurements of large post-yield strains. Available with Options E, L, and LE (may restrict elongation capability).	–100° to +400°F *(–75° to +205°C)*	±10% for gage lengths under 1/8 in *(3.2 mm)* ±20% for 1/8 in and over	±1000	10^4
				EP gages show zero shift under high-cyclic strains.	
ED	Isoelastic foil in combination with tough, flexible polyimide film. High gage factor and extended fatigue life excellent for dynamic measurements. Not normally used in static measurements due to very high thermal-output characteristics.	Dynamic: –320° to +400°F *(–195° to +205°C)*	±2% Nonlinear at strain levels over ±0.5%	±2500 ±2200	10^6 10^7
WD	Fully encapsulated isoelastic gages with high-endurance leadwires. Used in wide-range dynamic strain measurement applications in severe environments.	Dynamic: –320° to +500°F *(–195° to +260°C)*	±1.5% — nonlinear at strain levels over ±0.5%	±3000 ±2500 ±2200	10^5 10^7 10^8
SD	Equivalent to WD Series, but with solder dots instead of leadwires.	Dynamic: –320° to +400°F *(–195° to +205°C)*	±1.5% See above note	±2500 ±2200	10^6 10^7
EK	K-alloy foil in combination with a tough, flexible polyimide backing. Primarily used where a combination of higher grid resistances, stability at elevated temperature, and greatest backing flexibility are required.	Normal: –320° to +350°F *(–195° to +175°C)* Special or Short-Term: –452° to +400°F *(–269° to +205°C)*	±1.5%	±1800	10^7
WK	Fully encapsulated K-alloy gages with high-endurance leadwires. Widest temperature range and most extreme environmental capability of any general-purpose gage when self-temperature compensation is required. Option W available on some patterns, but restricts both fatigue life and maximum operating temperature.	Normal: –452° to +550°F *(–269° to +290°C)* Special or Short-Term: –452° to +750°F *(–269° to +400°C)*	±1.5%	±2400 ±2200 ±2000	10^6 10^7 10^8
SK	Fully encapsulated K-alloy gages with solder dots. Same uses as WK Series, but derated in maximum temperature and operating environment because of solder dots.	Normal: –452° to +450°F *(–269° to +230°C)* Special or Short-Term: –452° to +500°F *(–269° to +260°C)*	±1.5%	±2200 ±2000	10^6 10^7
S2K	K-alloy foil laminated to 0.001 in *(0.025 mm)* thick, high-performance polyimide backing, with a laminated polyimide overlay fully encapsulating the grid and solder tabs. Provided with large solder pads for ease of leadwire attachment.	Normal: –100° to +250°F *(–75° to +120°C)* Special or Short-Term: –300° to +300°F *(–185° to +150°C)*	±1.5%	±1800 ±1500	10^6 10^7

The performance data given here are *nominal*, and apply primarily to gages of 0.125-in *(3-mm)* gage length or larger.

Appendix E – ADM666 Voltage Regulator

Manufactured by Analog Devices
1 Technology Way
P.O. Box 9106
Norwood, MA 02062
(800) 262-5643

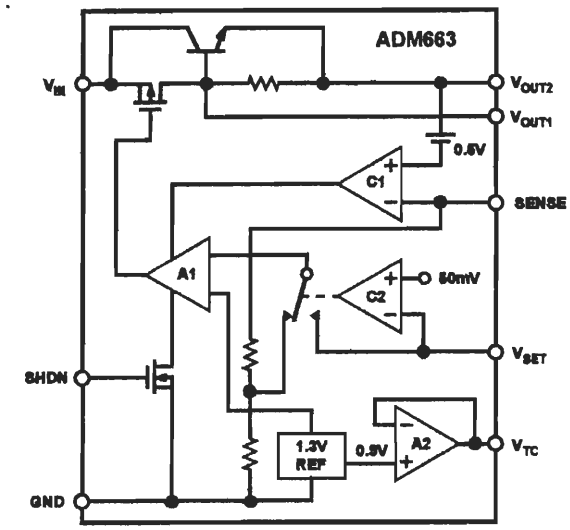
+5 V Fixed, Adjustable Micropower Linear Voltage Regulators

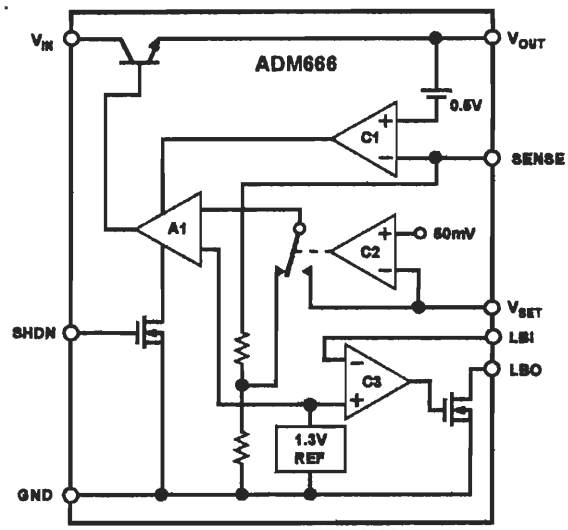
ADM663/ADM666

FEATURES
5 V Fixed or +1.3 V to +16 V Adjustable
Low Power CMOS: 12 µA max Quiescent Current
40 mA Output Current
Current Limiting
Pin Compatible with MAX663/666
+2 V to +16.5 V Operating Range
Low Battery Detector ADM666
No Overshoot on Power-Up

APPLICATIONS
Handheld Instruments
LCD Display Systems
Pagers
Remote Data Acquisition

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The ADM663/ADM666 are precision voltage regulators featuring a maximum quiescent current of 12 µA. They can be used to give a fixed +5 V output with no additional external components or can be adjusted from 1.3 V to 16 V using two external resistors. Fixed or adjustable operation is automatically selected via the V_{SET} input. The low quiescent current makes these devices especially suitable for battery powered systems. The input voltage range is 2 V to 16.5 V and an output current up to 40 mA is provided. The ADM663 can directly drive an external pass transistor for currents in excess of 40 mA. Additional features include current limiting and low power shutdown. Thermal shutdown circuitry is also included for additional safety.

The ADM666 features additional low battery monitoring circuitry to detect for low battery voltages.

The ADM663/ADM666 are pin-compatible replacements for the MAX663/666. Both are available in 8-pin DIP and in narrow surface mount (SOIC) packages.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM663AN	-40°C to +85°C	N-8
ADM663AR	-40°C to +85°C	R-8
ADM666AN	-40°C to +85°C	N-8
ADM666AR	-40°C to +85°C	R-8

REV. 0

One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

ADM663/ADM666–SPECIFICATIONS (V_{IN} = +9 V, V_{OUT} = + 5 V, T_A = + 25°C unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Input Voltage, V_{IN}	2.0		16.5	V	$T_A = T_{MIN}$ to T_{MAX}
Quiescent Current, I_Q					No Load, V_{IN} = +16.5 V
		6	12	µA	T_A = +25°C
			15	µA	$T_A = T_{MIN}$ to T_{MAX}
Output Voltage, V_{OUT}	4.75	5.0	5.25	V	$T_A = T_{MIN}$ to T_{MAX}, V_{SET} = GND
Line Regulation, $\Delta V_{OUT}/\Delta V_{IN}$		0.03	0.35	%/V	+2 V ≤ V_{IN} ≤ +15 V, $V_{OUT} = V_{REF}$
Load Regulation, $\Delta V_{OUT}/\Delta I_{OUT}$		3.0	7.0	Ω	ADM663, 1 mA ≤ I_{OUT2} ≤ 20 mA
		1.0	5.0	Ω	ADM663, 50 µA ≤ I_{OUT1} ≤ 5 mA
		3.0	7.0	Ω	ADM666, 1 mA ≤ I_{OUT} ≤ 20 mA
Reference Voltage, V_{SET}	1.27		1.33	V	$V_{OUT} = V_{SET}$
Reference Tempco, $\Delta V_{SET}/\Delta T$		±100		ppm/°C	$T_A = T_{MIN}$ to T_{MAX}
V_{SET} Internal Threshold, $V_{F/A}$		50		mV	$V_{SET} < V_{F/A}$ for +5 V Out;
					$V_{SET} > V_{F/A}$ for Adj. Out
V_{SET} Input Current, I_{SET}		±0.01	±10	nA	$T_A = T_{MIN}$ to T_{MAX}
Shutdown Input Voltage, V_{SHDN}	1.4			V	V_{SHDN} High = Output Off
			0.3	V	V_{SHDN} Low = Output On
Shutdown Input Current, I_{SHDN}		±0.01	±10	nA	
SENSE Input Threshold, V_{OUT}-V_{SENSE}		0.5		V	Current Limit Threshold
SENSE Input Resistance, R_{SENSE}		3		MΩ	
Input-Output Saturation Resistance, R_{SAT}					
ADM663 V_{OUT1}		200	500	Ω	V_{IN} = +2 V, I_{OUT} = 1 mA
		70	150	Ω	V_{IN} = +9 V, I_{OUT} = 2 mA
		50	150	Ω	V_{IN} = +15 V, I_{OUT} = 5 mA
Output Current from $V_{OUT(2)}$, I_{OUT}	40			mA	+3 V ≤ V_{IN} ≤ +16.5 V, V_{IN}-V_{OUT} = +1.5 V
Minimum Load Current, $I_{L(MIN)}$			1.0	µA	T_A = +25°C
			5.0	µA	$T_A = T_{MIN}$ to T_{MAX}
LBI Input Threshold, V_{LBI}	1.21	1.28	1.37	V	ADM666
LBI Input Current, I_{LBI}		±0.01	±10	nA	ADM666
LBO Output Saturation Resistance, R_{SAT}		35	100	Ω	ADM666, I_{SAT} = 2 mA
LBO Output Leakage Current		10		nA	ADM666, LBI = 1.4 V
V_{TC} Open Circuit Voltage, V_{TC}		0.9		V	ADM663
V_{TC} Sink Current, I_{TC}	2.0	8.0		mA	ADM663
V_{TC} Temperature Coefficient		+2.5		mV/°C	ADM663

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

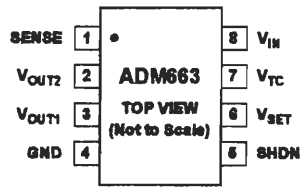
(T_A = +25°C unless otherwise noted)

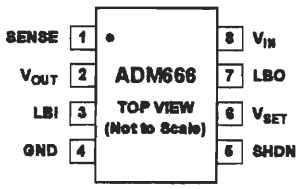
Input Voltage, V_{IN} ..... +18 V
Terminal Voltage
(ADM663) Pins 1, 3, 5, 6, 7
..... (GND - 0.3 V) to (V_{IN} + 0.3 V)
(ADM666) Pins 1, 2, 3, 5, 6
..... (GND - 0.3 V) to (V_{IN} + 0.3 V)
(ADM663) Pin 2 ..... (GND - 0.3 V) to (V_{OUT1} + 0.3 V)
(ADM666) Pin 7 ..... (GND - 0.3 V) to +16.5 V
Output Source Current
(ADM663, ADM666) Pin 2 ..... 50 mA
(ADM663) Pin 3 ..... 25 mA
Output Sink Current,
(ADM663, ADM666) Pin 7 .....-20 mA

Power Dissipation, N-8 .....625 mW
(Derate 8.3 mW/°C above +50°C)
θ_{JA}, Thermal Impedance ..... 120°C/W
Power Dissipation R-8 .....450 mW
(Derate 6 mW/°C above +50°C)
θ_{JA}, Thermal Impedance ..... 170°C/W
Operating Temperature Range
Industrial (A Version) .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
ESD Rating .....>5000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DIP & SOIC PIN CONFIGURATIONS





PIN FUNCTION DESCRIPTION

Mnemonic	Function
$V_{OUT(1)\ (2)}$	Voltage Regulator Output(s)
V_{IN}	Voltage Regulator Input
SENSE	Current Limit Sense Input. (Referenced to $V_{OUT(2)}$.) If not used it should be connected to $V_{OUT(2)}$
GND	Ground Pin. Must be connected to 0 V
LBI	Low Battery Detect Input. Compared with 1.3 V
LBO	Low Battery Detect Output. Open Drain Output
SHDN	Digital Input. May be used to disable the device so that the power consumption is minimized
V_{SET}	Voltage Setting Input. Connect to GND for +5 V output or connect to resistive divider for adjust able output
V_{TC}	Temperature-Proportional Voltage for negative TC Output

GENERAL INFORMATION

The ADM663/ADM666 contains a micropower bandgap reference voltage source, an error amplifier A1, two comparators C1, C2 and a series pass output transistor. A P-channel FET and an NPN transistor are used on the ADM663 while the ADM666 uses an NPN output transistor.

CIRCUIT DESCRIPTION

The internal bandgap reference is trimmed to 1.3 V ± 30 mV. This is used as a reference input to the error amplifier A1. The feedback signal from the regulator output is supplied to the other input by an on-chip voltage divider or by two external resistors. When V_{SET} is at ground, the internal divider provides the error amplifier's feedback signal giving a +5 V output. When V_{SET} is at more than 50 mV above ground, the error amplifier's input is switched directly to the V_{SET} pin, and external resistors are used to set the output voltage. The external resistors are selected so that the desired output voltage gives 1.3 V at V_{SET}.

Comparator C1 monitors the output current via the SENSE input. This input, referenced to $V_{OUT(2)}$, monitors the voltage drop across a load sense resistor. If the voltage drop exceeds 0.5 V, then the error amplifier A_1 is disabled and the output current is limited.

The ADM663 has an additional amplifier, A2, which provides a temperature-proportional output, V_{TC}. If this is summed into the inverting input of the error amplifier, a negative temperature coefficient results at the output. This is useful when powering liquid crystal displays over wide temperature ranges.

The ADM666 has an additional comparator, C3 which compares the voltage on the Low Battery Input, LBI, pin to the internal +1.3 V reference. The output from the comparator drives an open drain FET connected to the Low Battery Output pin, LBO. The Low Battery Threshold may be set using a suitable voltage divider connected to LBI. When the voltage on LBI falls below 1.3 V, the open drain output LBO is pulled low.

Both the ADM663 and the ADM666 contain a shutdown (SHDN) input which can be used to disable the error amplifier and hence the voltage output. The quiescent current in shutdown is less than 12 µA.

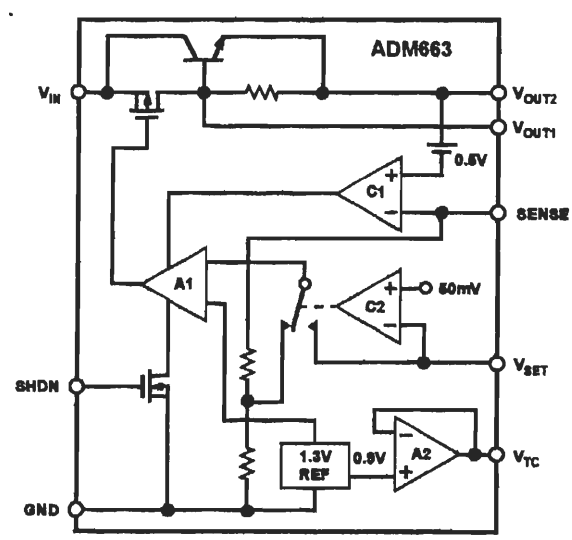


Figure 1. ADM663 Functional Block Diagram

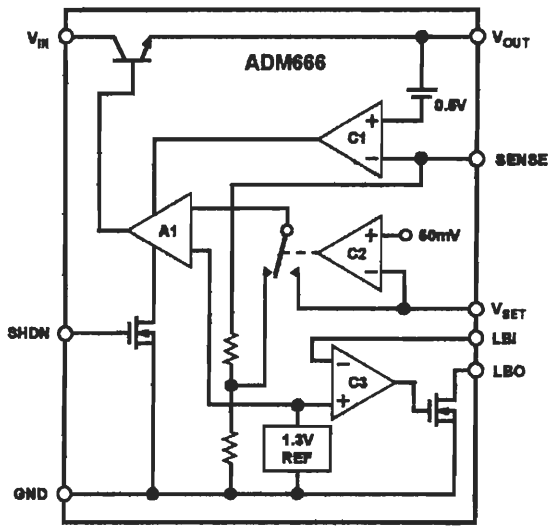


Figure 2. ADM666 Functional Block Diagram

Circuit Configurations

For a fixed +5 V output the V_{SET} input is grounded and no external resistors are necessary. This basic configuration is shown in Figure 3. Current limiting is not being utilized so the SENSE input is connected to $V_{OUT(2)}$. The input voltage can range from +6 V to +16 V and output currents up to 40 mA are available provided that the maximum package power dissipation is not exceeded.

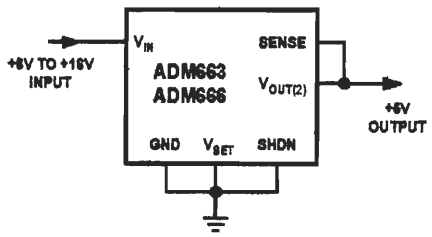


Figure 3. ADM663/ADM666 Fixed +5 V Output

Output Voltage Setting

If V_{SET} is not connected to GND, the output voltage is set according to the following equation.

$$V_{OUT} = V_{SET} \times \frac{R1 + R2}{R1} \quad where\ V_{SET} = 1.30\ V$$

The resistor values may be selected by firstly choosing a value for R1 and then selecting R2 according to the following equation.

$$R2 = R1 \times \left(\frac{V_{OUT}}{1.30} - 1 \right)$$

The input leakage current on V_{SET} is 10 nA maximum. This allows large resistor values to be chosen for R1 and R2 with little degradation in accuracy. For example, a 1 MΩ resistor may be selected for R1 and then R2 may be calculated accordingly. The tolerance on V_{SET} is guaranteed at less than ±30 mV so in most applications, fixed resistors will be suitable.

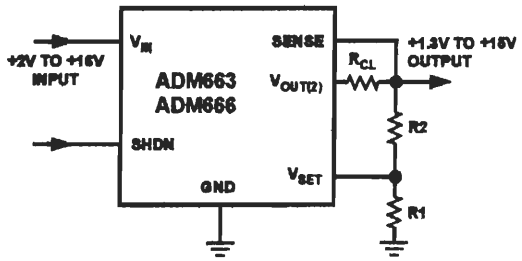


Figure 4. ADM663/ADM666 Adjustable Output

Current Limiting

Current limiting may be achieved by using an external current sense resistor in series with $V_{OUT(2)}$. When the voltage across the sense resistor exceeds the internal 0.5 V threshold, current limiting is activated. The sense resistor is therefore chosen such that the voltage across it will be 0.5 V when the desired current limit is reached.

$$R_{CL} = \frac{0.5}{I_{CL}}$$

where R_{CL} is the current sense resistor, I_{CL} is the maximum current limit.

The value chosen for R_{CL} should also ensure that the current is limited to less than the 50 mA absolute maximum rating and also that the power dissipation will also be within the package maximum ratings.

If current limiting is employed, there will be an additional voltage drop across the sense resistor which must be considered when determining the regulators dropout voltage.

If current limiting is not used, the SENSE input should be connected to $V_{OUT(2)}$.

Shutdown Input (SHDN)

The SHDN input allows the regulator to be switched off with a logic level signal. This will disable the output and reduce the current drain to a low quiescent (12 µA maximum) current. This is very useful for low power applications. The SHDN input should be driven with a CMOS logic level signal since the input threshold is 0.3 V. In TTL systems, an open collector driver with a pull-up resistor may be used.

If the shutdown function is not being used, then SHDN should be connected to GND.

Low Supply or Low Battery Detection

The ADM666 contains on-chip circuitry for low power supply or battery detection. If the voltage on the LBI pin falls below the internal 1.3 V reference, then the open drain output LBO will go low. The low threshold voltage may be set to any voltage above 1.3 V by appropriate resistor divider selection.

$$R3 = R4 \times \left(\frac{V_{BATT}}{1.30} - 1 \right)$$

where R3 and R4 are the resistive divider resistors and V_{BATT} is the desired low voltage threshold.

Since the LBI input leakage current is less than 10 nA, large values may be selected for R3 and R4 in order to minimize loading. For example, a 6 V low threshold, may be set using 10 MΩ for R3 and 2.7 MΩ for R4.

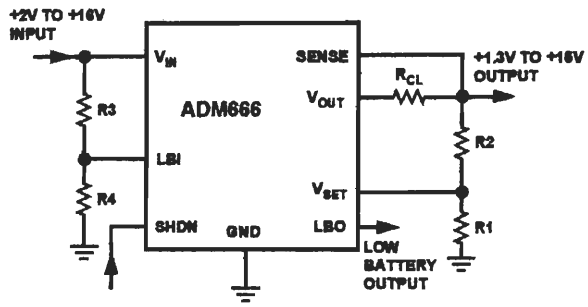


Figure 5. ADM666 Adjustable Output with Low Battery Detection

High Current Operation

The ADM663 contains an additional output, V_{OUT1}, suitable for directly driving the base of an external NPN transistor. Figure 6 shows a configuration which can be used to provide +5 V with boosted current drive. A 1 Ω current sensing resistor limits the current at 0.5 A.

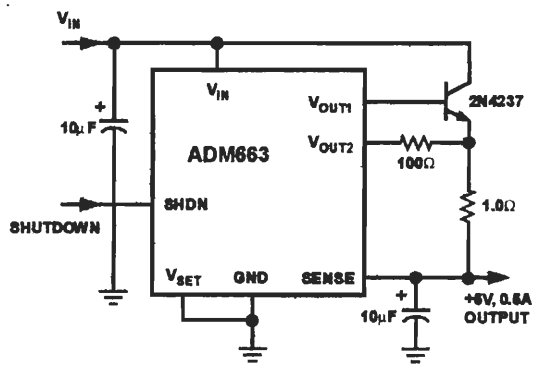


Figure 6. ADM663 Boosted Output Current (0.5 A)

Temperature Proportional Output

The ADM663 contains a V_{TC} output with a positive temperature coefficient of +2.5 mV/°C. This may be connected to the summing junction of the error amplifier (V_{SET}) through a resistor resulting in a negative temperature coefficient at the output of the regulator.

This is especially useful in multiplexed LCD displays to compensate for the inherent negative temperature coefficient of the LCD threshold. At 25°C the voltage at the VTC output is typically 0.9 V. The equations for setting both the output voltage and the tempco are given below. If this function is not being used, then V_{TC} should be left unconnected.

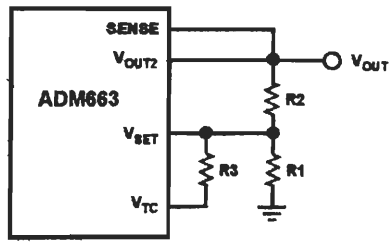


Figure 7. ADM663 Temperature Proportional Output

$$V_{OUT} = V_{SET} \times \left(1 + \frac{R2}{R1}\right) + \frac{R2}{R3} \times \left(V_{SET} - V_{TC}\right)$$

$$TCV_{OUT} = \frac{-R2}{R3} \times TVC_{TC}$$

where $V_{SET} = +1.3\,V$, $V_{TC} = +0.9\,V$, $TCV_{TC} = +2.5\,mV/°C$

APPLICATION HINTS

Input-Output (Dropout Voltage)

A regulator's minimum input-output differential or dropout voltage determines the lowest input voltage for a particular output voltage. The ADM663/ADM666 dropout voltage is 0.8 V at its rated output current. For example when used as a fixed +5 V regulator the minimum input voltage is +5.8 V. At lower output currents, (I_{OUT} < 5 mA), on the ADM663, V_{OUT1} may be used as the output driver in order to achieve lower dropout voltages. Please refer to Figure 9. In this case the dropout voltage depends on the voltage drop across the internal FET transistor. This may be calculated by multiplying the FET's saturation resistance by the output current. As the current limit circuitry is referenced to V_{OUT2}, V_{OUT2} should be connected to V_{OUT1}. For high current operation V_{OUT2} should be used alone and V_{OUT1} left unconnected.

Bypass Capacitors

The high frequency performance of the ADM663/ADM666 may be improved by decoupling the output using a filter capacitor. A capacitor value of 10 µF is suitable.

An input capacitor helps reduce noise and improves dynamic performance. A suitable input capacitor of 0.1 µF or greater may be used.

ADM663/ADM666–Typical Performance Characteristics

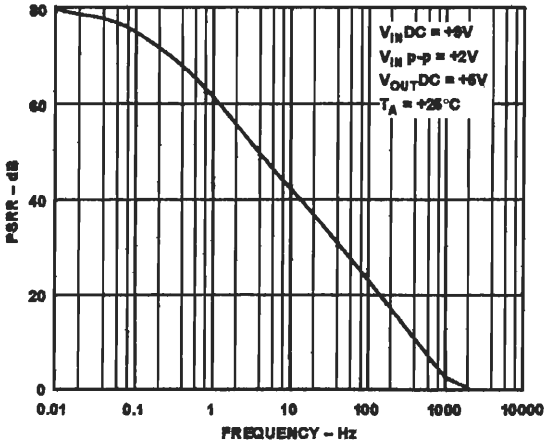


Figure 8. Power Supply Rejection Ratio vs. Frequency

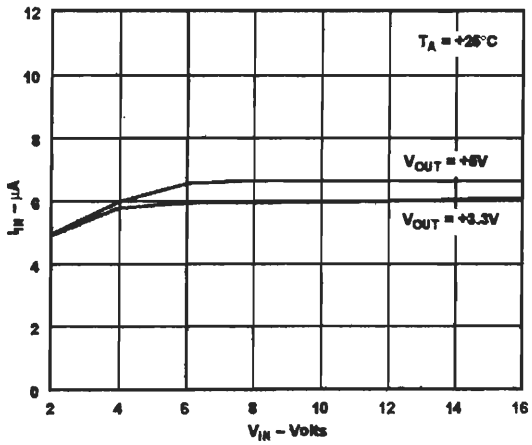


Figure 10. Quiescent Current vs. Input Voltage

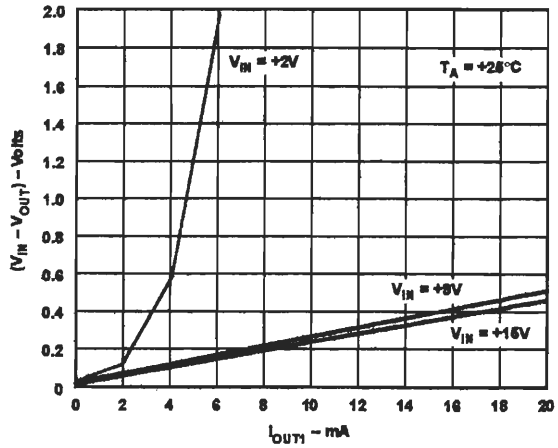


Figure 9. V_{OUT1} Input-Output Differential vs. Output Current

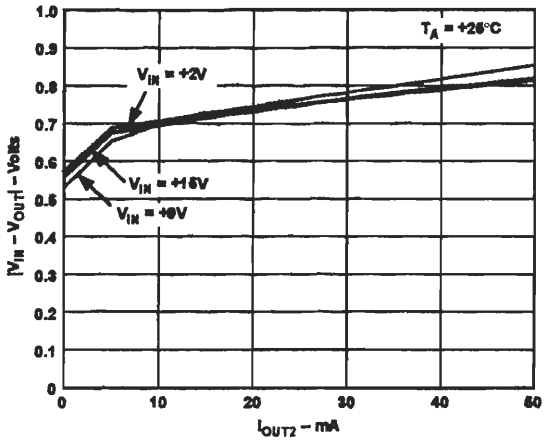
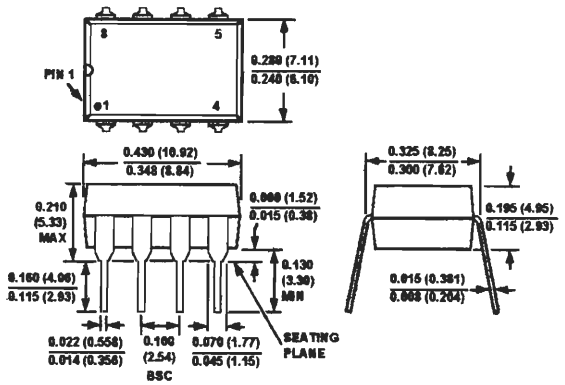


Figure 11. $V_{OUT(2)}$ Input-Output Differential vs. Output Current

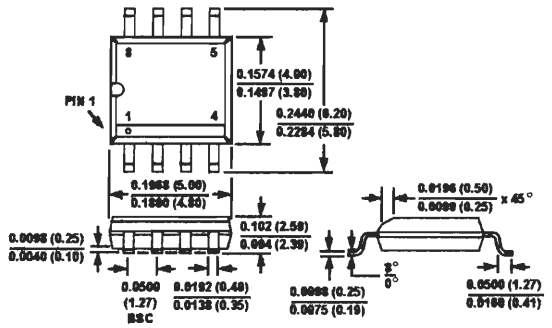
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP (N-8)



8-Lead Narrow-Body (R-8)



ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM663AN	-40°C to +85°C	N-8
ADM663AR	-40°C to +85°C	R-8
ADM666AN	-40°C to +85°C	N-8
ADM666AR	-40°C to +85°C	R-8

*For outline information see Package Information section.

FOR CATALOG

ADM663/ADM666 ADM663/ADM666

ADM663/ADM666 ADM663/ADM666

Appendix F – AMP04 Instrumentation Amplifier

Manufactured by Analog Devices
1 Technology Way
P.O. Box 9106
Norwood, MA 02062
(800) 262-5643

ANALOG DEVICES

(16)

Precision Single Supply Instrumentation Amplifier

AMP-04*

FEATURES

Single Supply Operation
Low Supply Current: 700 μA max
Wide Gain Range: 1 to 1000
Low Offset Voltage: 150 μV max
Zero-In/Zero-Out
Single-Resistor Gain Set
8-pin Mini-DIP and SO packages

APPLICATIONS

Strain Gages
Thermocouples
RTDs
Battery Powered Equipment
Medical Instrumentation
Data Acquisition Systems
PC Based Instruments
Portable Instrumentation

GENERAL DESCRIPTION

The AMP-04 is a single-supply instrumentation amplifier designed to work over a +5 volt to ±15 volt supply range. It offers an excellent combination of accuracy, low power consumption, wide input voltage range, and excellent gain performance.

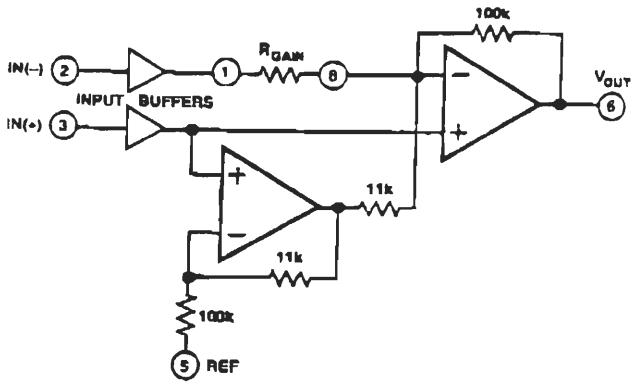
Gain is set by a single external resistor and can be from 1 to 1000. Input common-mode voltage range allows the AMP-04 to handle signals with full accuracy from ground to within 1 volt of the positive supply. And the output can swing to within 1 volt of the positive supply. Gain bandwidth is over 700 kHz. In addition to being easy to use, the AMP-04 draws only 700 μA of supply current.

For high resolution data acquisition systems, laser trimming of low drift thin-film resistors limits the input offset voltage to under 150 μV, and allows the AMP-04 to offer gain nonlinearity of 0.005% and a gain tempco of 30 ppm/°C.

A proprietary input structure limits input offset currents to less than 5 nA with drift of only 8 pA/°C, allowing direct connection of the AMP-04 to high impedance transducers and other signal sources.

*Protected by U.S. Patent No: 5,075,633.

FUNCTIONAL BLOCK DIAGRAM

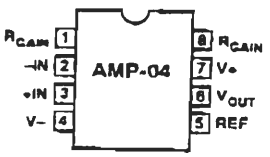


The AMP-04 is specified over the extended industrial (−40°C to +85°C) temperature range. AMP-04s are available in plastic and ceramic DIP plus SO-8 surface mount packages.

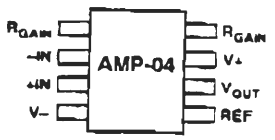
Contact your local sales office for MIL-STD-883 data sheet and availability.

PIN CONNECTIONS

8-Lead Epoxy DIP (P Suffix)



8-Lead Narrow-Body SO (S Suffix)



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700
Fax: 617/326-8703

AMP-04—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +5 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	AMP-04E Min	AMP-04E Typ	AMP-04E Max	AMP-04F Min	AMP-04F Typ	AMP-04F Max	Units
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}			30	150			300	μV
		−40°C ≤ T_A ≤ +85°C			300			600	μV
Input Offset Voltage Drift	TCV_{IOS}				3			6	μV/°C
Output Offset Voltage	V_{OOS}			0.5	1.5			3	mV
		−40°C ≤ T_A ≤ +85°C			3			6	mV
Output Offset Voltage Drift	TCV_{OOS}				30			50	μV/°C
INPUT CURRENT									
Input Bias Current	I_B			22	30			40	nA
		−40°C ≤ T_A ≤ +85°C			50			60	nA
Input Bias Current Drift	TCI_B			65			65		pA/°C
Input Offset Current	I_{OS}			1	5			10	nA
		−40°C ≤ T_A ≤ +85°C			10			15	nA
Input Offset Current Drift	TCI_{OS}			8			8		pA/°C
INPUT									
Common-Mode Input Resistance				4			4		GΩ
Differential Input Resistance				4			4		GΩ
Input Voltage Range	V_{IN}		0		3.0	0		3.0	V
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 3.0 V							
		G = 1	60	80		55			dB
		G = 10	80	100		75			dB
		G = 100	90	105		80			dB
		G = 1000	90	105		80			dB
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 2.5 V, −40°C ≤ T_A ≤ +85°C							
		G = 1	55			50			dB
		G = 10	75			70			dB
		G = 100	85			75			dB
		G = 1000	85			75			dB
Power Supply Rejection	PSRR	4.0 V ≤ V_S ≤ 12 V, −40°C ≤ T_A ≤ +85°C							
		G = 1	95			85			dB
		G = 10	105			95			dB
		G = 100	105			95			dB
		G = 1000	105			95			dB
GAIN (G = 100 K/R_{GAIN})									
Gain Equation Accuracy		G = 1 to 100		0.2	0.5			0.75	%
		G = 1 to 100, −40°C ≤ T_A ≤ +85°C			0.8			1.0	%
		G = 1000		0.4			0.75		%
Gain Range	G		1		1000	1		1000	V/V
Nonlinearity		G = 1, R_L = 5 kΩ		0.005					%
		G = 10, R_L = 5 kΩ		0.015					%
		G = 100, R_L = 5 kΩ		0.025					%
Gain Temperature Coefficient	ΔG/ΔT			30			50		ppm/°C
OUTPUT									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	4.0	4.2		4.0			V
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C	3.8			3.8			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ, −40°C ≤ T_A ≤ +85°C			2.0			2.5	mV
Output Current Limit		Sink		30			30		mA
		Source		15			15		mA

Parameter	Symbol	Conditions	AMP-04E Min	AMP-04E Typ	AMP-04E Max	AMP-04F Min	AMP-04F Typ	AMP-04F Max	Units
NOISE									
Noise Voltage Density, RTI	e_N	f = 1 kHz, G = 1		270			270		nV/√Hz
		f = 1 kHz, G = 10		45			45		nV/√Hz
		f = 100 Hz, G = 100		30			30		nV/√Hz
		f = 100 Hz, G = 1000		25			25		nV/√Hz
Noise Current Density, RTI	i_N	f = 100 Hz, G = 100		4			4		pA/√Hz
Input Noise Voltage	e_N p-p	0.1 to 10 Hz, G = 1		7			7		µV p-p
		0.1 to 10 Hz, G = 10		1.5			1.5		µV p-p
		0.1 to 10 Hz, G = 100		0.7			0.7		µV p-p
DYNAMIC RESPONSE									
Small Signal Bandwidth	BW	G = 1, −3 dB		300			300		kHz
POWER SUPPLY									
Supply Current	I_{SY}			550	700			700	µA
		−40°C ≤ T_A ≤ +85°C			850			850	µA

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (V_S = ±15 V, V_{CM} = 0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	AMP-04E Min	AMP-04E Typ	AMP-04E Max	AMP-04F Min	AMP-04F Typ	AMP-04F Max	Units
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}			80	400			600	µV
		−40°C ≤ T_A ≤ +85°C			600			900	µV
Input Offset Voltage Drift	TCV_{IOS}				3			6	µV/°C
Output Offset Voltage	V_{OOS}			1	3			6	mV
		−40°C ≤ T_A ≤ +85°C			6			9	mV
Output Offset Voltage Drift	TCV_{OOS}				30			50	µV/°C
INPUT CURRENT									
Input Bias Current	I_B			17	30			40	nA
		−40°C ≤ T_A ≤ +85°C			50			60	nA
Input Bias Current Drift	TCI_B			65			65		pA/°C
Input Offset Current	I_{OS}			2	5			10	nA
		−40°C ≤ T_A ≤ −85°C			15			20	nA
Input Offset Current Drift	TCI_{OS}			28			28		pA/°C
INPUT									
Common-Mode Input Resistance				4					GΩ
Differential-Mode Input Resistance				4					GΩ
Input Voltage Range	V_{IN}		−12		+12	−12		+12	V
Common-Mode Rejection	CMR	−12 V ≤ V_{CM} ≤ +12 V							
		G = 1	60	80		55			dB
		G = 10	80	100		75			dB
		G = 100	90	105		80			dB
		G = 1000	90	105		80			dB
	CMR	−11 V ≤ V_{CM} ≤ +11 V							
		−40°C ≤ T_A ≤ +85°C							
		G = 1	55			50			dB
		G = 10	75			70			dB
		G = 100	85			75			dB
		G = 1000	85			75			dB
Power Supply Rejection	PSRR	±2.5 V ≤ V_S ≤ ±18 V							
		−40°C ≤ T_A ≤ +85°C							
		G = 1	75			70			dB
		G = 10	90			80			dB
		G = 100	95			85			dB
		G = 1000	95			85			dB

Parameter	Symbol	Conditions	AMP-04E Min	AMP-04E Typ	AMP-04E Max	AMP-04F Min	AMP-04F Typ	AMP-04F Max	Units
GAIN (G = 100 K/R_{GAIN})									
Gain Equation Accuracy		G = 1 to 100		0.2	0.5			0.75	%
		G = 1000		0.4			0.75		%
		G = 1 to 100							
		−40°C ≤ T_A ≤ +85°C			0.8			1.0	%
Gain Range	G		1		1000	1		1000	V/V
Nonlinearity		G = 1, R_L = 5 kΩ		0.005			0.005		%
		G = 10, R_L = 5 kΩ		0.015			0.015		%
		G = 100, R_L = 5 kΩ		0.025			0.025		%
Gain Temperature Coefficient	ΔG/ΔT			30			50		ppm/°C
OUTPUT									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	+13	+13.4		+13			V
		R_L = 2 kΩ							
		−40°C ≤ T_A ≤ +85°C	+12.5			+12.5			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ							
		−40°C ≤ T_A ≤ + 85°C			−14.5			−14.5	V
Output Current Limit		Sink		30			30		mA
		Source		15			15		mA
NOISE									
Noise Voltage Density, RTI	e_N	f = 1 kHz, G = 1		270			270		nV/√Hz
		f = 1 kHz, G = 10		45			45		nV/√Hz
		f = 100 Hz, G = 100		30			30		nV/√Hz
		f = 100 Hz, G = 1000		25			25		nV/√Hz
Noise Current Density, RTI	i_N	f = 100 Hz, G = 100		4			4		pA/√Hz
Input Noise Voltage	e_N p-p	0.1 to 10 Hz, G = 1		5			5		μV p-p
	e_N p-p	0.1 to 10 Hz, G = 10		1			1		μV p-p
	e_N p-p	0.1 to 10 Hz, G = 100		0.5			0.5		μV p-p
DYNAMIC RESPONSE									
Small Signal Bandwidth	BW	G = 1, −3 dB		700			700		kHz
POWER SUPPLY									
Supply Current	I_{SY}			750	900			900	μA
	I_{SY}	−40°C ≤ T_A ≤ +85°C			1100			1100	μA

Specifications subject to change without notice.

WAFER TEST LIMITS (V_S = +5 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
OFFSET VOLTAGE				
Input Offset Voltage	V_{IOS}		300	μV max
Output Offset Voltage	V_{OOS}		3	mV max
INPUT CURRENT				
Input Bias Current	I_B		40	nA max
Input Offset Current	I_{OS}		10	nA max
INPUT				
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 3.0 V		
		G = 1	55	dB min
		G = 10	75	dB min
		G = 100	80	dB min
		G = 1000	80	dB min
Common-Mode Rejection	CMR	V_S = ±15 V, −12 V ≤ V_{CM} ≤ +12 V		
		G = 1	55	dB min
		G = 10	75	dB min
		G = 100	80	dB min
		G = 1000	80	dB min

Parameter	Symbol	Conditions	Limit	Units
Power Supply Rejection	PSRR	4.0 V ≤ V_S ≤ 12 V		
		G = 1	85	dB min
		G = 10	95	dB min
		G = 100	95	dB min
		G = 1000	95	dB min
GAIN (G = 100 K/R_{GAIN})				
Gain Equation Accuracy		G = 1 to 100	0.75	% max
OUTPUT				
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	4.0	V min
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ	2.5	mV max
POWER SUPPLY				
Supply Current	I_{SY}	V_S = ±15	900	μA max
			700	μA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Common-Mode Input Voltage[2] . . . . . ±18 V
Differential Input Voltage . . . . . 36 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
Z Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
AMP-04A . . . . . −55°C to +125°C
AMP-04E, F . . . . . −40°C to +85°C
Junction Temperature Range
Z Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

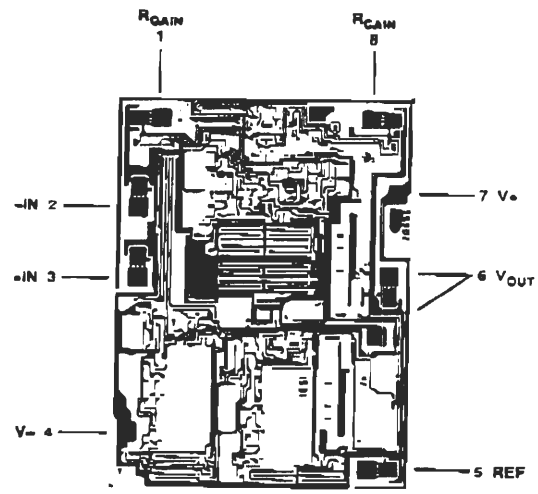
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

V_{OS} @ +5 V T_A = +25°C	Cerdip 8-Pin	Plastic 8-Pin	Temperature Range
*	AMP04AZ/883		MIL
150 μV		AMP04EP	XIND
300 μV		AMP04FP	XIND
300 μV		AMP04FS	XIND
300 μV		AMP04GBC	+25°C

*Consult MIL-STD-883 data sheet.

DICE CHARACTERISTICS



AMP-04 Die Size 0.075 × 0.99 inch, 7,425 sq. mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 81.

APPLICATIONS

Common-Mode Rejection

The purpose of the instrumentation amplifier is to amplify the difference between the two input signals while ignoring offset and noise voltages common to both inputs. One way of judging the device's ability to reject this offset is the common-mode gain, which is the ratio between a change in the common-mode voltage and the resulting output voltage change. Instrumentation amplifiers are often judged by the common-mode rejection ratio, which is equal to 20 × $\log_{10}$ of the ratio of the user-selected differential signal gain to the common-mode gain, commonly called the CMRR. The AMP-04 offers excellent CMRR, guaranteed to be greater than 90 dB at gains of 100 or greater. Input offsets attain very low temperature drift by proprietary laser-trimmed thin-film resistors and high gain amplifiers.

Input Common-Mode Range Includes Ground

The AMP-04 employs a patented topology (Figure 1) that uniquely allows the common-mode input voltage to truly extend to zero volts where other instrumentation amplifiers fail. To illustrate, take for example the single supply, gain of 100 instrumentation amplifier as in Figure 2. As the inputs approach zero volts, in order for the output to go positive, amplifier A's output (V_{OA}) must be allowed to go below ground, to −0.094 volts. Clearly this is not possible in a single supply environment. Consequently this instrumentation amplifier configuration's input common-mode voltage cannot go below about 0.4 volts. In comparison, the AMP-04 has no such restriction. Its inputs will function with a zero-volt common-mode voltage.

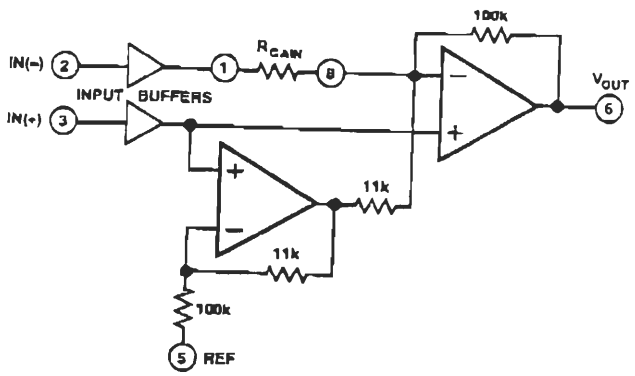


Figure 1. Functional Block Diagram

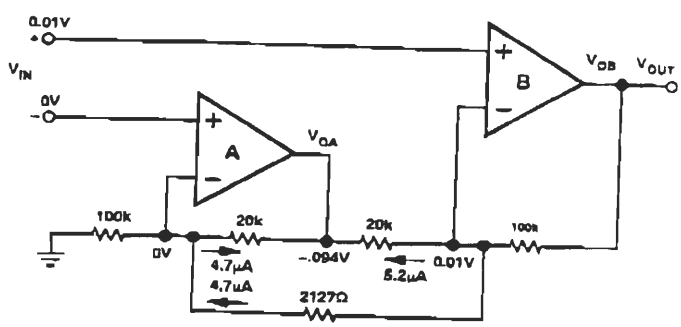


Figure 2. Gain = 100 Instrumentation Amplifier

Input Common-Mode Voltage Below Ground

Although not tested and guaranteed, the AMP-04 inputs are biased in a way that they can amplify signals linearly with common-mode voltage as low as −0.25 volts below ground. This holds true over the industrial temperature range from −40°C to +85°C.

Extended Positive Common-Mode Range

On the high side, other instrumentation amplifier configurations, such as the three op amp instrumentation amplifier, can have severe positive common-mode range limitations. Figure 3 shows an example of a gain of 1001 amplifier, with an input common-mode voltage of 10 volts. For this circuit to function, V_{OB} must swing to 15.01 volts in order for the output to go to 10.01 volts. Clearly no op amp can handle this swing range (given a +15 V supply) as the output will saturate long before it reaches the supply rails. Again the AMP-04's topology does not have this limitation. Figure 4 illustrates the AMP-04 operating at the same common-mode conditions as in Figure 3. None of the internal nodes has a signal high enough to cause amplifier saturation. As a result, the AMP-04 can accommodate much wider common-mode range than most instrumentation amplifiers.

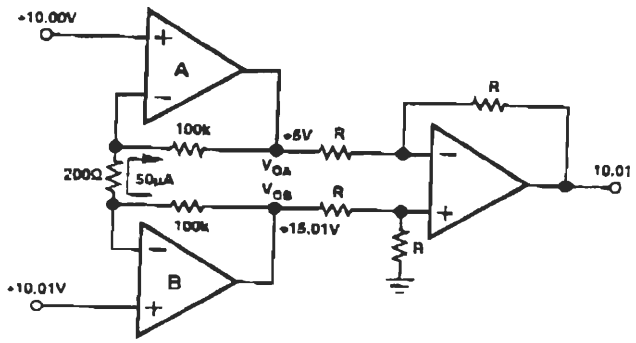


Figure 3. Gain = 1001, Three Op Amp Instrumentation Amplifier

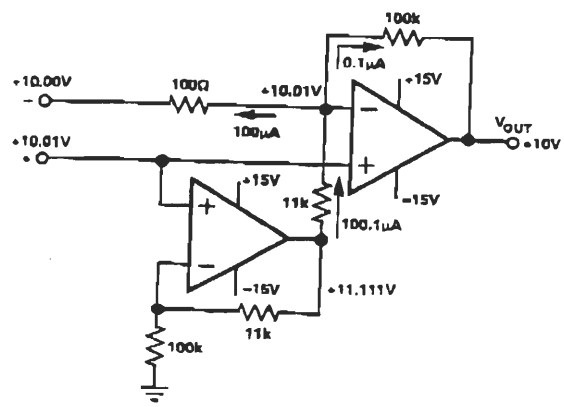


Figure 4. Gain = 1000, AMP-04

Programming the Gain

The gain of the AMP-04 is programmed by the user by selecting a single external resistor—R_{GAIN}:

$$Gain = 100\ k\Omega/R_{GAIN}$$

The output voltage is then defined as the differential input voltage times the gain.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times Gain$$

In single supply systems, offsetting the ground is often desired for several reasons. Ground may be offset from zero to provide a quieter signal reference point, or to offset "zero" to allow a unipolar signal range to represent both positive and negative values.

In noisy environments such as those having digital switching, switching power supplies or externally generated noise, ground may not be the ideal place to reference a signal in a high accuracy system.

Often, real world signals such as temperature or pressure may generate voltages that are represented by changes in polarity. In a single supply system the signal input cannot be allowed to go below ground, and therefore the signal must be offset to accommodate this change in polarity. On the AMP-04, a reference input pin is provided to allow offsetting of the input range.

The gain equation is more accurately represented by including this reference input.

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times Gain + V_{REF}$$

Grounding

The most common problems encountered in high performance analog instrumentation and data acquisition system designs are found in the management of offset errors and ground noise. Primarily, the designer must consider temperature differentials and thermocouple effects due to dissimilar metals, IR voltage drops, and the effects of stray capacitance. The problem is greatly compounded when high speed digital circuitry, such as that accompanying data conversion components, is brought into the proximity of the analog section. Considerable noise and error contributions such as fast-moving logic signals that easily propagate into sensitive analog lines, and the unavoidable noise common to digital supply lines must all be dealt with if the accuracy of the carefully designed analog section is to be preserved.

Besides the temperature drift errors encountered in the amplifier, thermal errors due to the supporting discrete components should be evaluated. The use of high quality, low-TC components where appropriate is encouraged. What is more important, large thermal gradients can create not only unexpected changes in component values, but also generate significant thermoelectric voltages due to the interface between dissimilar metals such as lead solder, copper wire, gold socket contacts, Kovar lead frames, etc. Thermocouple voltages developed at these junctions commonly exceed the TCV_{OS} contribution of the AMP-04. Component layout that takes into account the power dissipation at critical locations in the circuit and minimizes gradient effects and differential common-mode voltages by taking advantage of input symmetry will minimize many of these errors.

High accuracy circuitry can experience considerable error contributions due to the coupling of stray voltages into sensitive areas, including high impedance amplifier inputs which benefit from such techniques as ground planes, guard rings, and shields. Careful circuit layout, including good grounding and signal routing practice to minimize stray coupling and ground loops is recommended. Leakage currents can be minimized by using high quality socket and circuit board materials, and by carefully cleaning and coating complete board assemblies.

As mentioned above, the high speed transition noise found in logic circuitry is the sworn enemy of the analog circuit designer. Great care must be taken to maintain separation between them to minimize coupling. A major path for these error voltages will be found in the power supply lines. Low impedance, load related variations and noise levels that are completely acceptable in the high thresholds of the digital domain make the digital supply unusable in nearly all high performance analog applications. The user is encouraged to maintain separate power and ground between the analog and digital systems wherever possible, joining only at the supply itself if necessary, and to observe careful grounding layout and bypass capacitor scheduling in sensitive areas.

Input Shield Drivers

High impedance sources and long cable runs from remote transducers in noisy industrial environments commonly experience significant amounts of noise coupled to the inputs. Both stray capacitance errors and noise coupling from external sources can be minimized by running the input signal through shielded cable. The cable shield is often grounded at the analog input common, however improved dynamic noise rejection and a reduction in effective cable capacitance is achieved by driving the shield with a buffer amplifier at a potential equal to the voltage seen at the input. Driven shields are easily realized with the AMP-04. Examination of the simplified schematic shows that the potentials at the gain set resistor pins of the AMP-04 follow the inputs precisely. As shown in Figure 5, shield drivers are easily realized by buffering the potential at these pins by a dual, single supply op amp such as the OP-213. Alternatively, applications with single-ended sources or that use twisted-pair cable could drive a single shield. To minimize error contributions due to this additional circuitry, all components and wiring should remain in proximity to the AMP-04 and careful grounding and bypassing techniques should be observed.

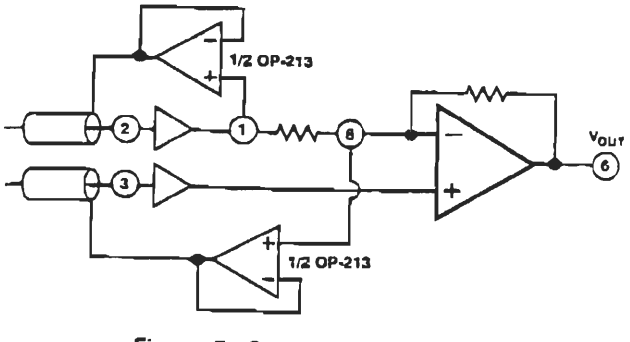


Figure 5. Cable Shield Drivers

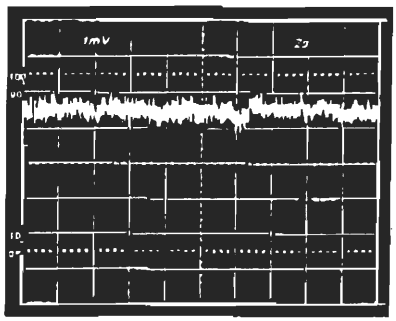


Figure 7c. 10 Hz Low-Pass Filtered Output

Power Supply Considerations

In dual supply applications (for example ±15 V) if the input is connected to a low resistance source less than 100 Ω, a large current may flow in the input leads if the positive supply is applied before the negative supply during power-up. A similar condition may also result upon a loss of the negative supply. If these conditions could be present in you system, it is recommended that a series resistor up to 1 kΩ be added to the input leads to limit the input current.

This condition can not occur in a single supply environment as losing the negative supply effectively removes any current return path.

Offset Nulling in Dual Supply

Offset may be nulled by feeding a correcting voltage at the V_{REF} pin (Pin 5). However, it is important that the pin be driven with a low impedance source. Any measurable resistance will degrade the amplifier's common-mode rejection performance as well as its gain accuracy. An op amp may be used to buffer the offset null circuit as in Figure 8.

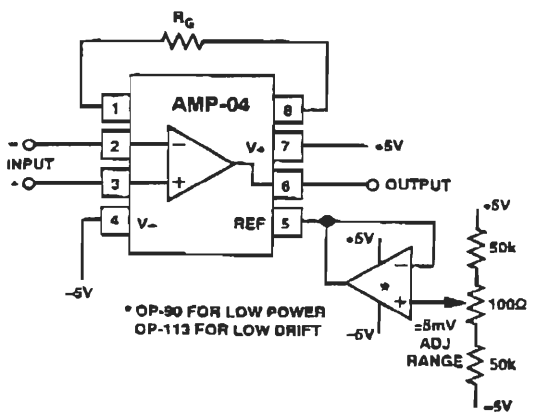


Figure 8. Offset Adjust for Dual Supply Applications

Offset Nulling in Single Supply

Nulling the offset in single supply systems is difficult because the adjustment is made to try to attain zero volts. At zero volts out, the output is in saturation (to the negative rail) and the output voltage is indistinguishable from the normal offset error. Consequently the offset nulling circuit in Figure 9 must be used with caution.

First, the potentiometer should be adjusted to cause the output to swing in the positive direction; then adjust it in the reverse direction, causing the output to swing toward ground, until the output just stops changing. At that point the output is at the saturation limit.

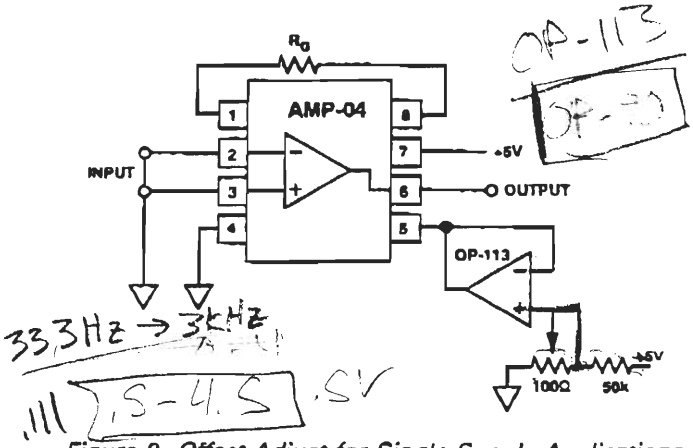


Figure 9. Offset Adjust for Single Supply Applications

Alternative Nulling Method

An alternative null correction technique is to inject an offset current into the summing node of the output amplifier as in Figure 10. This method does not require an external op amp. However the drawback is that the amplifier will move off its null as the input common-mode voltage changes. It is a less desirable nulling circuit than the previous method.

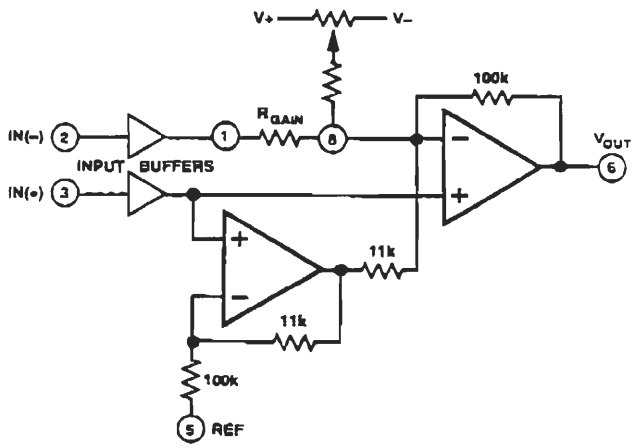


Figure 10. Current Injection Offsetting Is Not Recommended

APPLICATION CIRCUITS

Low Power Precision Single Supply RTD Amplifier

Figure 11 shows a linearized RTD amplifier that is powered off a single +5 volt supply. However, the circuit will work up to 36 volts without modification. The RTD is excited by a 100 μA constant current that is regulated by amplifier A (OP-295). The 0.202 volts reference voltage used to generate the constant current is divided down from the 2.500 volt reference. The AMP-04 amplifies the bridge output to a 10 mV/°C output coefficient.

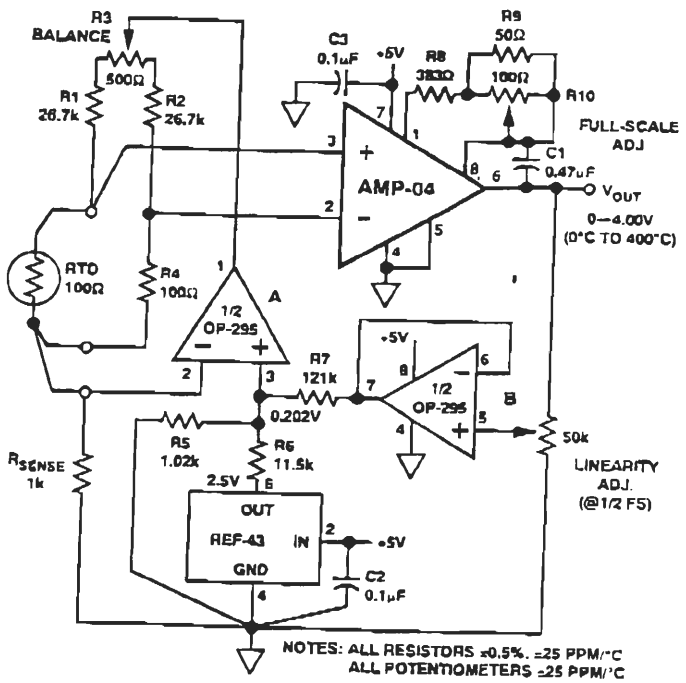


Figure 11. Precision Single Supply RTD Thermometer Amplifier

The RTD is linearized by feeding a portion of the signal back to the reference circuit, increasing the reference voltage as the temperature increases. When calibrated properly, the RTD's nonlinearity error will be canceled.

To calibrate, either immerse the RTD into a zero-degree ice bath or substitute an exact 100 Ω resistor in place of the RTD. Then adjust bridge BALANCE potentiometer R3 for a 0 volt output. Note that a 0 volt output is also the negative output swing limit of the AMP-04 powered with a single supply. Therefore, be sure to adjust R3 to first cause the output to swing positive and then back off until the output just stop swinging negatively.

Next, set the LINEARITY ADJ. potentiometer to the mid-range. Substitute an exact 247.04 Ω resistor (equivalent to 400°C temperature) in place of the RTD. Adjust the FULL-SCALE potentiometer for a 4.000 volts output.

Finally substitute a 175.84 Ω resistor (equivalent to 200°C temperature), and adjust the LINEARITY ADJ potentiometer for a 2.000 volts at the output. Repeat the full-scale and the half-scale adjustments as needed.

When properly calibrated, the circuit achieves better than ±0.5°C accuracy within a temperature measurement range from 0°C to 400°C.

Precision 4–20mA Loop Transmitter With Noninteractive Trim

Figure 12 shows a full bridge strain gage transducer amplifier circuit that is powered off the 4–20 mA current loop. The AMP-04 amplifies the bridge signal differentially and is converted to a current by the output amplifier. The total quiescent current drawn by the circuit, which includes the bridge, the amplifiers, and the resistor biasing, is only a fraction of the 4 mA null current that flows through the current-sense resistor R_{SENSE}. The voltage across R_{SENSE} feeds back to the OP-90's input, whose common-mode is fixed at the current summing reference voltage, thus regulating the output current.

With no bridge signal, the 4 mA null is simply set up by the 50 kΩ NULL potentiometer plus the 976 kΩ resistors that inject an offset that forces an 80 mV drop across R_{SENSE}. At a 50 mV full-scale bridge voltage, the AMP-04 amplifies the voltage-to-current converter for a full-scale of 20 mA at the output. Since the OP-90's input operates at a constant 0 volt common-mode voltage, the null and the span adjustments do

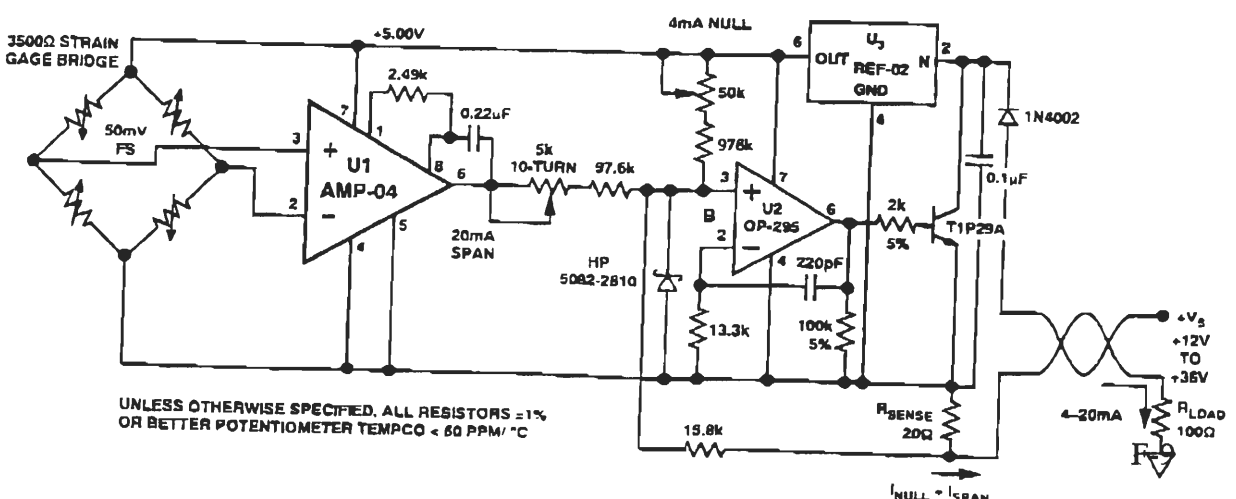


Figure 12. Precision 4–20 mA Loop Transmitter Features Noninteractive Trims

not interact with one another. Calibration is simple and easy with the NULL adjusted first, followed by SPAN adjust. The entire circuit can be remotely placed, and powered from the 4–20 mA 2-wire loop.

4–20 mA Loop Receiver

At the receiving end of a 4–20 mA loop, the AMP-04 makes a convenient differential receiver to convert the current back to a usable voltage (Figure 13). The 4–20 mA signal current passes through a 100 Ω sense resistor. The voltage drop is differentially amplified by the AMP-04. The 4 mA offset is removed by the offset correction circuit.

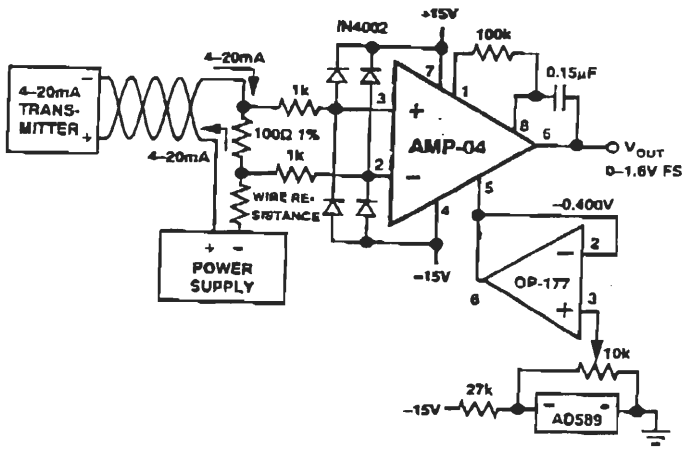


Figure 13. 4 to 20 mA Line Receiver

Low Power, Pulsed Load-Cell Amplifier

Figure 14 shows a 350 Ω load cell that is pulsed with a low duty cycle to conserve power. The OP-295's rail-to-rail output capability allows a maximum voltage of 10 volts to be applied to the bridge. The bridge voltage is selectively pulsed on when a measurement is made. A negative-going pulse lasting 200 ms should be applied to the MEASURE input. The long pulse width is necessary to allow ample settling time for the long time constant of the low-pass filter around the AMP-04. A much faster settling time can be achieved by omitting the filter capacitor.

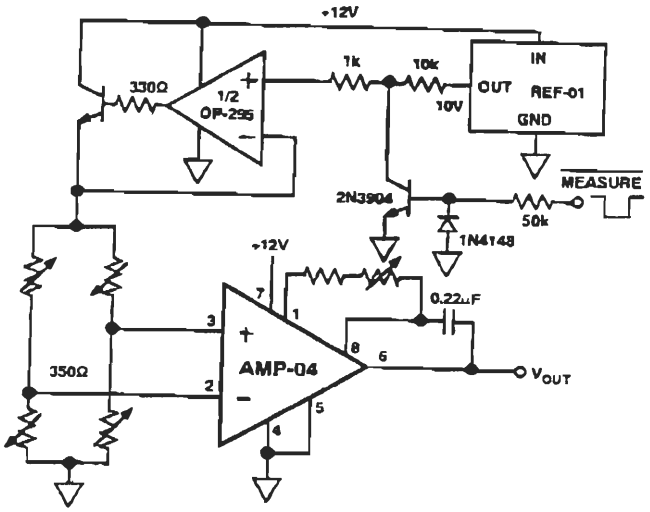


Figure 14. Pulsed Load Cell Bridge Amplifier

Single Supply Programmable Gain Instrumentation Amplifier

Combining with the single supply ADG221 quad analog switch the AMP-04 makes a useful programmable gain amplifier that can handle input and output signals at zero volts. Figure 15 shows the implementation. A logic low input to any of the gain control ports will cause the gain to change by shorting a gain-set resistor across AMP-04's Pins 1 and 8. Trimming is required at higher gains to improve accuracy because the switch ON-resistance becomes a more significant part of the gain-set resistance. The gain of 500 setting has two switches connected in parallel to reduce the switch resistance.

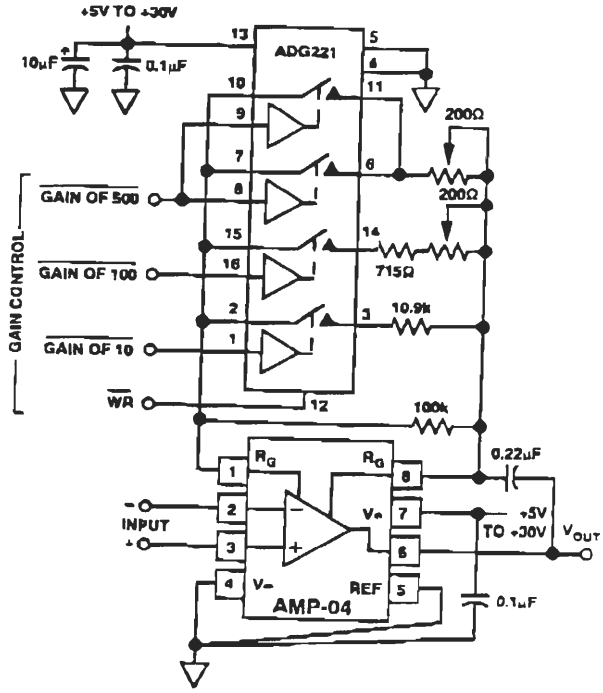


Figure 15. Single Supply Programmable Gain Instrumentation Amplifier

The switch ON resistance is lower if the supply voltage is 12 volts or higher. Additionally the overall amplifier's temperature coefficient also improves with higher supply voltage.

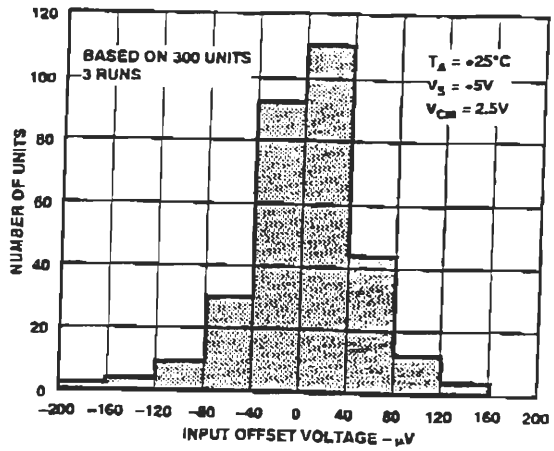


Figure 16. Input Offset (V_{IOS}) Distribution @ +5 V

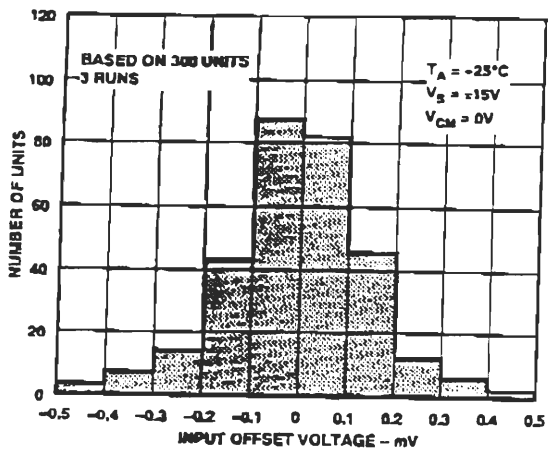


Figure 17. Input Offset (V_{IOS}) Distribution @ ±15 V

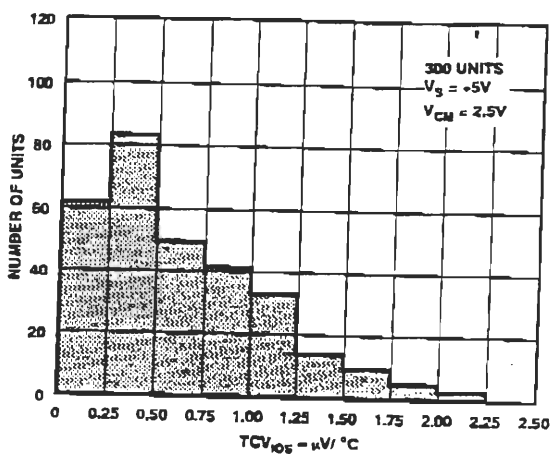


Figure 18. Input Offset Drift (TCV_{IOS}) Distribution @ +5 V

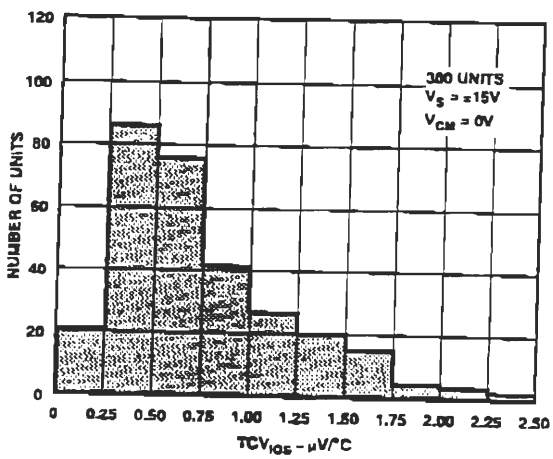


Figure 19. Input Offset Drift (TCV_{IOS}) Distribution @ ±15 V

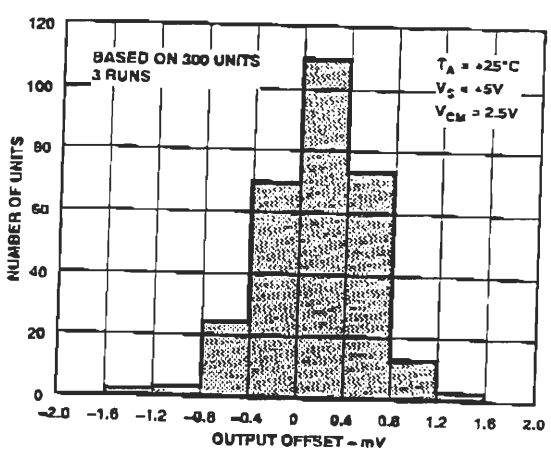


Figure 20. Output Offset (V_{OOS}) Distribution @ +5 V

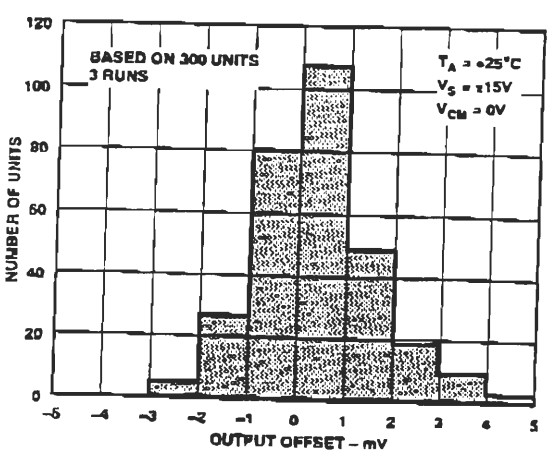


Figure 21. Output Offset (V_{OOS}) Distribution @ ±15 V

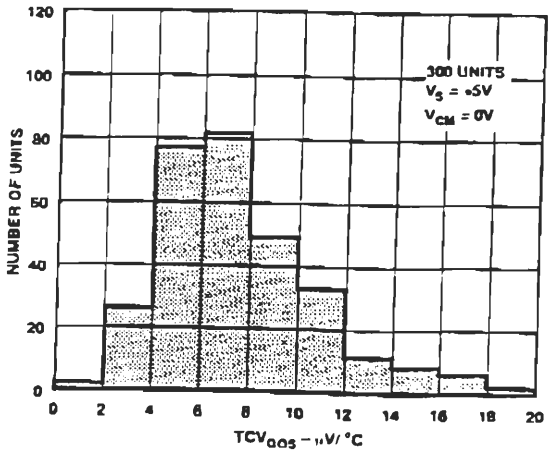


Figure 22. Output Offset Drift (TCV_{OOS}) Distribution @ ±5 V

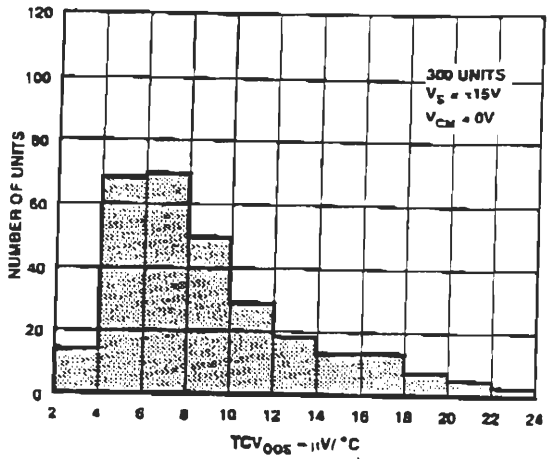


Figure 23. Output Offset Drift (TCV_{OOS}) Distribution @ ±15 V

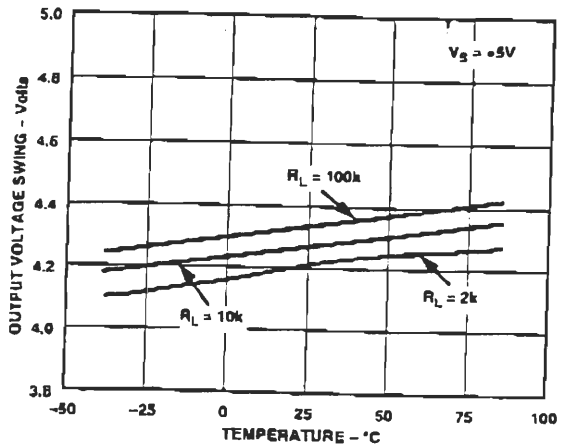


Figure 24. Output Voltage Swing vs. Temperature @ ±5 V

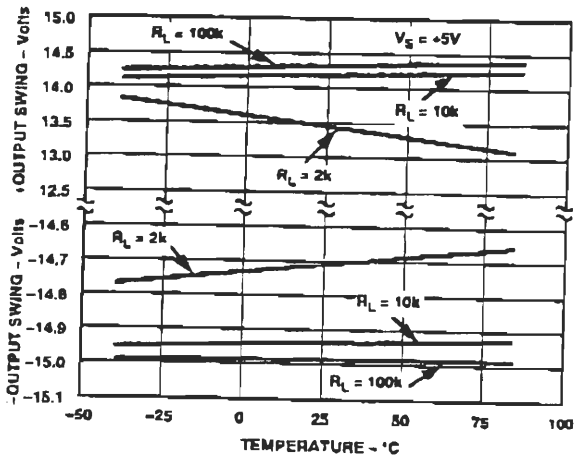


Figure 25. Output Voltage Swing vs. Temperature @ ±15 V

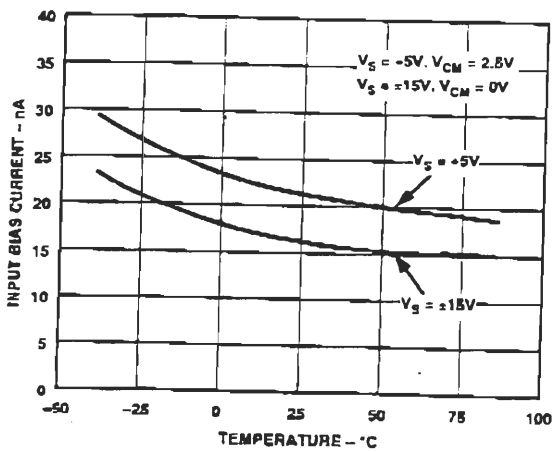


Figure 26. Input Bias Current vs. Temperature

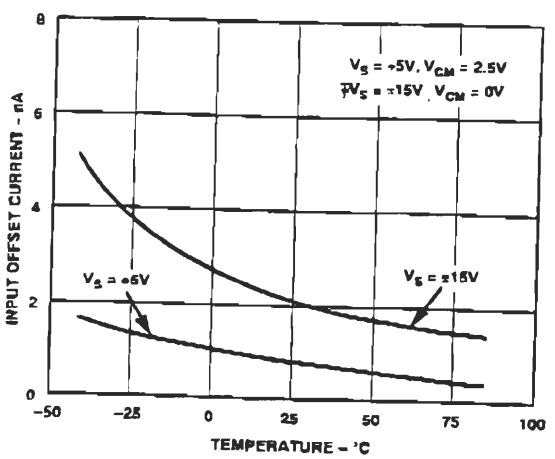


Figure 27. Input Offset Current vs. Temperature

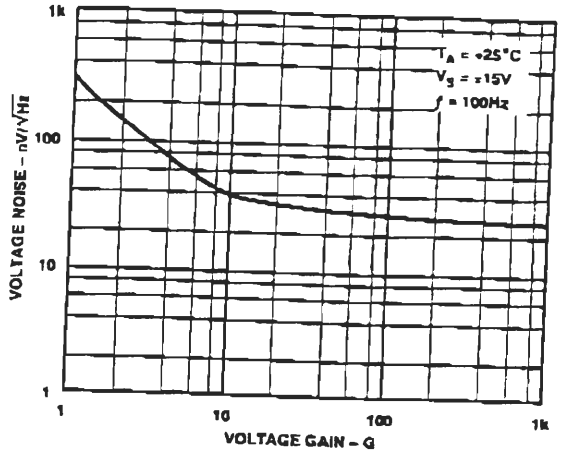


Figure 34. Voltage Noise Density vs. Gain

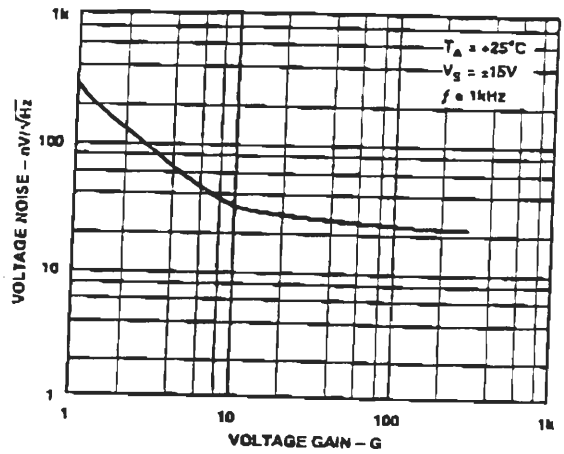


Figure 35. Voltage Noise Density vs. Gain, f = 1 kHz

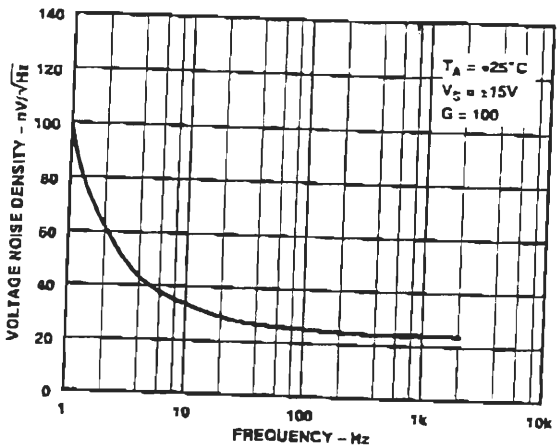


Figure 36. Voltage Noise Density vs. Frequency

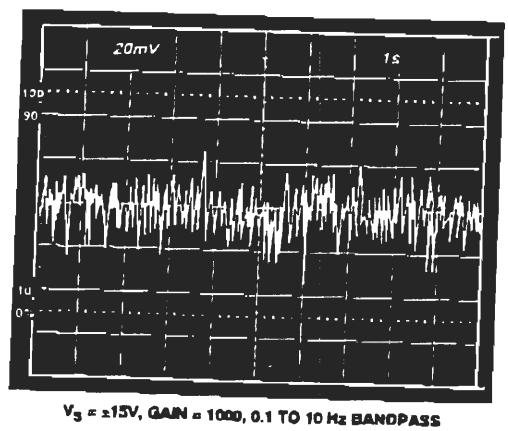


Figure 37. Input Noise Voltage

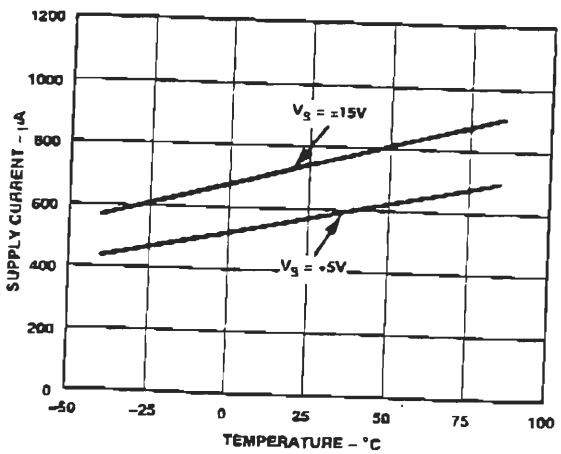


Figure 38. Supply Current vs. Temperature

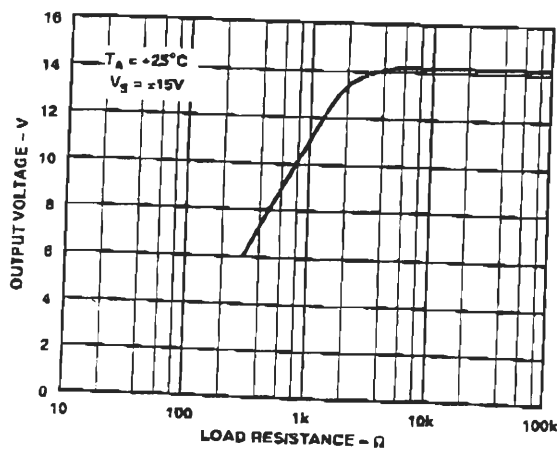
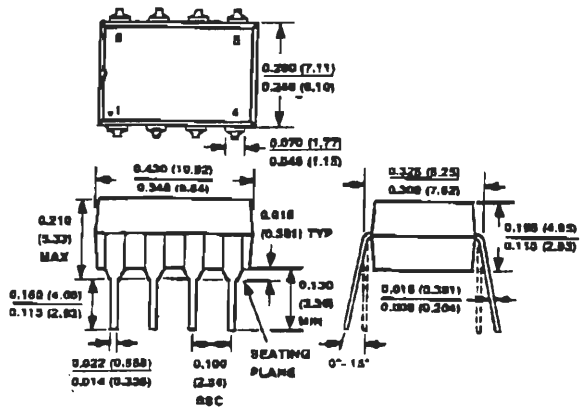


Figure 39. Maximum Output Voltage vs. Load Resistance

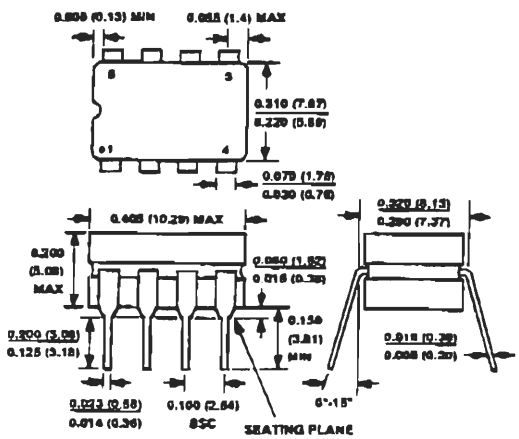
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

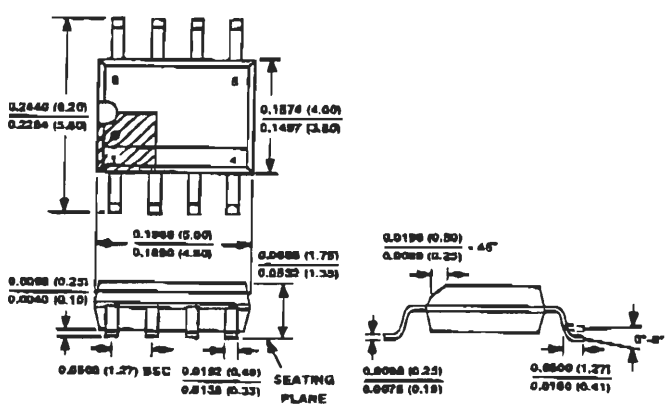
8-Lead Plastic DIP (N-8)



8-Lead Cerdip (Q-8)



8-Lead Narrow-Body SO (S0-8)



Appendix G – OP90 Operational Amplifier

Manufactured by Analog Devices
1 Technology Way
P.O. Box 9106
Norwood, MA 02062
(800) 262-5643

Precision, Low Voltage Micropower Operational Amplifier

OP-90

FEATURES

- **Single/Dual Supply Operation ..... +1.6V to +36V**
  +0.8V to ±18V
- **True Single-Supply Operation; Input and Output Voltage Ranges Include Ground**
- **Low Supply Current ..... 20μA Max**
- **High Output Drive ..... 5mA Min**
- **Low Input Offset Voltage ..... 150μV Max**
- **High Open-Loop Gain ..... 700V/mV Min**
- **Outstanding PSRR ..... 5.6μV/V Max**
- **Standard 741 Pinout with Nulling to V–**
- **Available in Die Form**

GENERAL DESCRIPTION

The OP-90 is a high performance micropower op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ±0.8 to ±18V. Input voltage range includes the negative rail allowing the OP-90 to accommodate input signals down to ground in single supply operation. The OP-90's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

The OP-90 draws less than 20μA of quiescent supply current, while able to deliver over 5mA of output current to a load. Input offset voltage is below 150μV eliminating the need for external nulling. Gain exceeds 700,000 and common-mode rejection is better than 100dB. The power supply-rejection ratio of under 5.6μV/V minimizes offset voltage changes experienced in battery powered systems.

The low offset voltage and high gain offered by the OP-90 bring precision performance to micropower applications. The minimal voltage and current requirements of the OP-90 suit it for battery and solar powered applications, such as portable instruments, remote sensors, and satellites.

ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (mV)	PACKAGE: CERDIP 8-PIN	PACKAGE: PLASTIC 8-PIN	PACKAGE: LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
150	OP90AZ*	–	OP90ARC/883	MIL
150	OP90EZ	–	–	IND
250	OP90FZ	–	–	IND
450	–	OP90GP	–	XIND
450	–	OP90GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

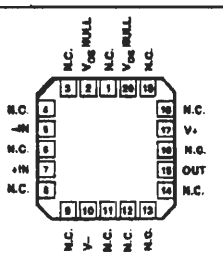
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS

8-PIN HERMETIC DIP
(Z-Suffix)

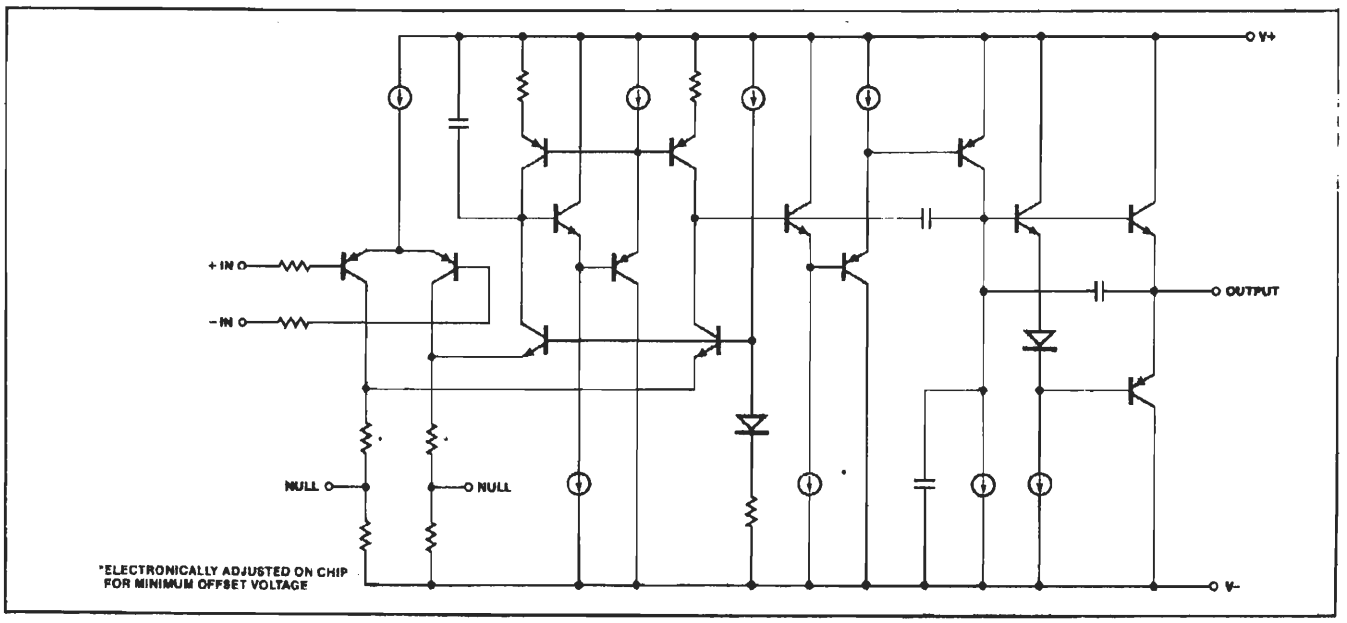
8-PIN EPOXY MINI-DIP
(P-Suffix)

8-PIN SO (S-Suffix)



OP-90 ARC/883
LCC (RC-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Common-Mode Input Voltage
..... [(V–) – 20V] to [(V+) + 20V]
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
Z Package ..... –65°C to +150°C
P Package ..... –65°C to +150°C
Operating Temperature Range
OP-90A ..... –55°C to +125°C
OP-90E, OP-90F ..... –25°C to +85°C
OP-90G ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±1.5V to ±15V, T_A = +25°C, unless otherwise noted.

			OP-90A/E			OP-90F			OP-90G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	50	150	—	75	250	—	125	450	µV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.4	3	—	0.4	5	—	0.4	5	nA
Input Bias Current	I_B	V_{CM} = 0V	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V R_L = 100kΩ	700	1200	—	500	1000	—	400	800	—	V/mV
		R_L = 10kΩ	350	600	—	250	500	—	200	400	—	
		R_L = 2kΩ	125	250	—	100	200	—	100	200	—	
		V+ = 5V, V– = 0V, 1V < V_O < 4V R_L = 100kΩ	200	400	—	125	300	—	100	250	—	
		R_L = 10kΩ	100	180	—	75	140	—	70	140	—	
Input Voltage Range	IVR	V+ = 5V, V– = 0V	0/4	—	—	0/4	—	—	0/4	—	—	V
		V_S = ±15V (Note 2)	–15/13.5	—	—	–15/13.5	—	—	–15/13.5	—	—	
Output Voltage Swing	V_O	V_S = ±15V R_L = 10kΩ	±14	±14.2	—	±14	±14.2	—	±14	±14.2	—	V
		R_L = 2kΩ	±11	±12	—	±11	±12	—	±11	±12	—	
	V_{OH}	V+ = 5V, V– = 0V R_L = 2kΩ	4.0	4.2	—	4.0	4.2	—	4.0	4.2	—	V
	V_{OL}	V+ = 5V, V– = 0V R_L = 10kΩ	—	100	500	—	100	500	—	100	500	µV
Common Mode Rejection	CMR	V+ = 5V, V– = 0V, 0V < V_{CM} < 4V	90	110	—	80	100	—	80	100	—	dB
		V_S = ±15V, –15V < V_{CM} < 13.5V	100	130	—	90	120	—	90	120	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	1.0	5.6	—	3.2	10	µV/V
Slew Rate	SR	V_S = ±15V	5	12	—	5	12	—	5	12	—	V/ms
Supply Current	I_{SY}	V_S = ±1.5V	—	9	15	—	9	15	—	9	15	µA
		V_S = ±15V	—	14	20	—	14	20	—	14	20	
Capacitive Load Stability		A_V = +1 No Oscillations (Note 1)	250	650	—	250	650	—	250	650	—	pF
Input Noise Voltage	e_{np-p}	f_O = 0.1Hz to 10Hz V_S = ±15V	—	3	—	—	3	—	—	3	—	μV_{p-p}
Input Resistance Differential Mode	R_{IN}	V_S = ±15V	—	30	—	—	30	—	—	30	—	MΩ
Input Resistance Common Mode	R_{INCM}	V_S = ±15V	—	20		—	20	—	—	20	—	GΩ

NOTES:
1. Guaranteed but not 100% tested.
2. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-90A MIN	OP-90A TYP	OP-90A MAX	UNITS
Input Offset Voltage	V_{OS}		—	80	400	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2.5	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.0	20	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$				V/mV
		$R_L = 100k\Omega$	225	400	—	
		$R_L = 10k\Omega$	125	240	—	
		$R_L = 2k\Omega$	50	110	—	
		$V+ = 5V$, $V- = 0V$, $1V < V_O < 4V$				
		$R_L = 100k\Omega$	100	200	—	
		$R_L = 10k\Omega$	50	110	—	
Input Voltage Range	IVR	$V+ = 5V$, $V- = 0V$ (Note 1)	0/3.5	—	—	V
		$V_S = \pm 15V$	−15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm 15V$				V
		$R_L = 10k\Omega$	±13.5	±13.7	—	
		$R_L = 2k\Omega$	±10.5	±11.5	—	
	V_{OH}	$V+ = 5V$, $V- = 0V$				V
		$R_L = 2k\Omega$	3.9	4.1	—	
	V_{OL}	$V+ = 5V$, $V- = 0V$				μV
		$R_L = 10k\Omega$	—	100	500	
Common Mode Rejection	CMR	$V+ = 5V$, $V- = 0V$, $0V < V_{CM} < 3.5V$	85	105	—	dB
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	95	115	—	
Power Supply Rejection Ratio	PSRR		—	3.2	10	μV/V
Supply Current	I_{SY}	$V_S = \pm 1.5V$	—	15	25	μA
		$V_S = \pm 15V$	—	19	30	

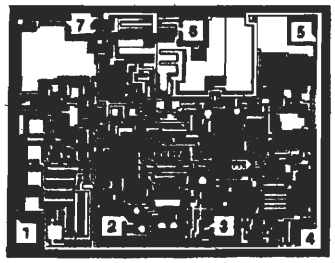
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±1.5V to ±15V, −25°C ≤ T_A ≤ +85°C for OP-90E/F, −40°C ≤ T_A ≤ +85°C for OP-90G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-90E MIN	OP-90E TYP	OP-90E MAX	OP-90F MIN	OP-90F TYP	OP-90F MAX	OP-90G MIN	OP-90G TYP	OP-90G MAX	UNITS
Input Offset Voltage	V_{OS}		—	70	270	—	110	550	—	180	675	µV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2	—	0.6	5	—	1.2	5	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.8	3	—	1.0	5	—	1.3	7	nA
Input Bias Current	I_B	V_{CM} = 0V	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V										V/mV
		R_L = 100kΩ	500	800	—	350	700	—	300	600	—	
		R_L = 10kΩ	250	400	—	175	350	—	150	250	—	
		R_L = 2kΩ	100	200	—	75	150	—	75	125	—	
		V+ = 5V, V− = 0V, 1V < V_O < 4V										
		R_L = 100kΩ	150	280	—	100	220	—	80	160	—	
		R_L = 10kΩ	75	140	—	50	110	—	40	90	—	
Input Voltage Range	IVR	V+ = 5V, V− = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		V_S = ±15V (Note 1)	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Output Voltage Swing	V_O	V_S = ±15V										V
		R_L = 10kΩ	±13.5	±14	—	±13.5	±14	—	±13.5	±14	—	
		R_L = 2kΩ	±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	
	V_{OH}	V+ = 5V, V− = 0V										V
		R_L = 2kΩ	3.9	4.1	—	3.9	4.1	—	3.9	4.1	—	
	V_{OL}	V+ = 5V, V− = 0V										µV
		R_L = 10kΩ	—	100	500	—	100	500	—	100	500	
Common Mode Rejection	CMR	V+ = 5V, V− = 0V, 0V < V_{CM} < 3.5V	90	110	—	80	100	—	80	100	—	dB
		V_S = ±15V, −15V < V_{CM} < 13.5V	100	120	—	90	110	—	90	110	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	3.2	10	—	5.6	17.8	µV/V
Supply Current	I_{SY}	V_S = ±1.5V	—	13	25	—	13	25	—	12	25	µA
		V_S = ±15V	—	17	30	—	17	30	—	16	30	

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.067 inch, 5762 sq. mils
(2.18 × 1.70mm, 3.71 sq. mm)

1. V_{OS} NULL
2. –IN
3. +IN
4. V–
5. V_{OS} NULL
6. OUT
7. V+

WAFER TEST LIMITS at $V_S = \pm1.5V$ to $\pm15V$, $T_A = 25°C$, unless otherwise noted.

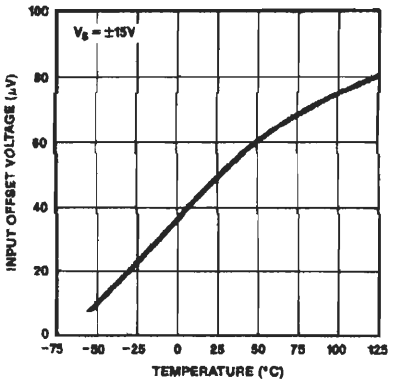
PARAMETER	SYMBOL	CONDITIONS	OP-90GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		250	µV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	5	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	20	nA MAX
Large Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$	 500 250	 V/mV MIN
		V+ = 5V, V– = 0V, $1V < V_O < 4V$ $R_L = 100k\Omega$	 125	 V/mV MIN
Input Voltage Range	IVR	V+ = 5V, V– = 0V (Note 1) $V_S = \pm15V$	0/4 –15/13.5	V MIN
Output Voltage Swing	V_O	$V_S = \pm15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 ±14 ±11	 V MIN
	V_{OH}	V+ = 5V, V– = 0V $R_L = 2k\Omega$	 4.0	V MIN
	V_{OL}	V+ = 5V, V– = 0V $R_L = 10k\Omega$	 500	µV MAX
Common Mode Rejection	CMR	V+ = 5V, V– = 0V, $0V < V_{CM} < 4V$ $V_S = \pm15V$, $-15V < V_{CM} < 13.5V$	80 90	dB MIN
Power Supply Rejection Ratio	PSRR		10	µV/V MAX
Supply Current	I_{SY}	$V_S = \pm15V$	20	µA MAX

NOTES:
1. Guaranteed by CMR test.

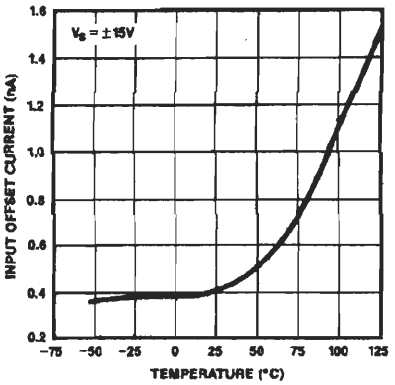
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

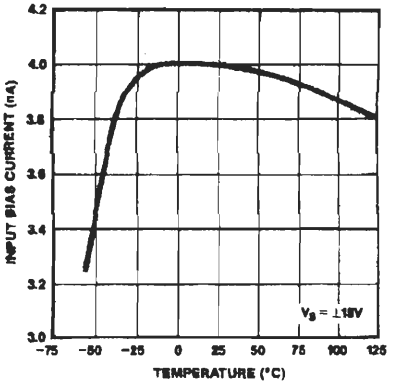
INPUT OFFSET VOLTAGE vs TEMPERATURE



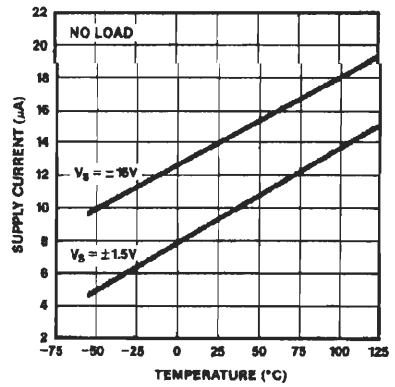
INPUT OFFSET CURRENT vs TEMPERATURE



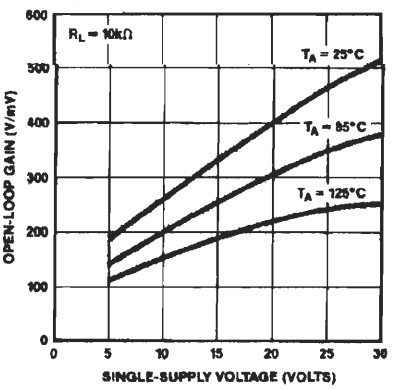
INPUT BIAS CURRENT vs TEMPERATURE



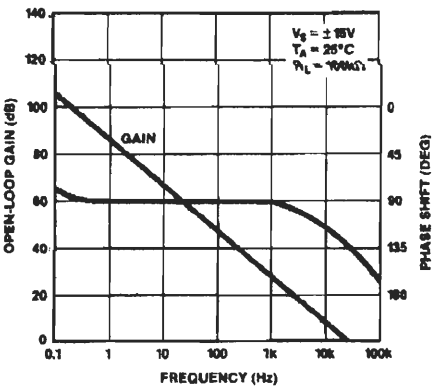
SUPPLY CURRENT vs TEMPERATURE



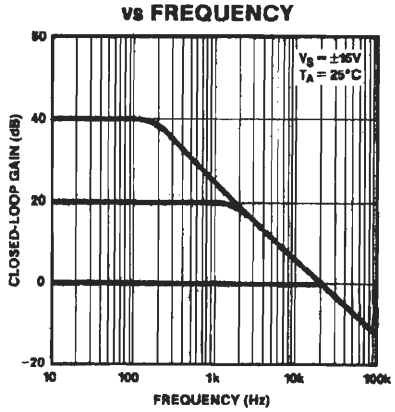
OPEN-LOOP GAIN vs SINGLE-SUPPLY VOLTAGE



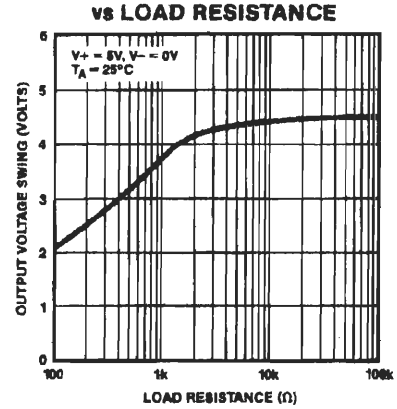
OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



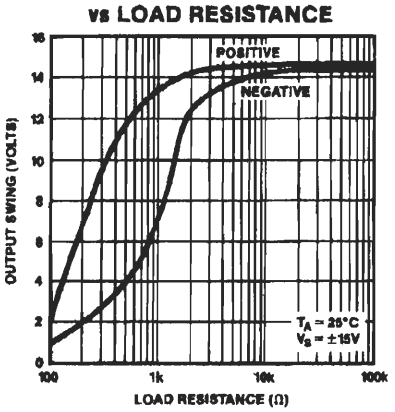
CLOSED-LOOP GAIN vs FREQUENCY



OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

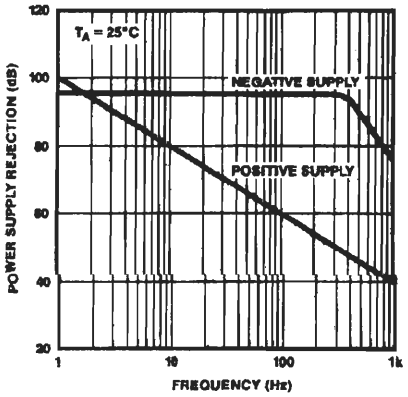


OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

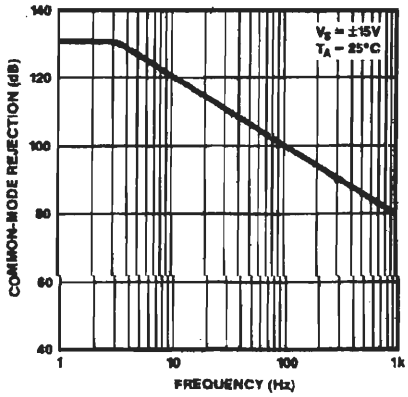


TYPICAL PERFORMANCE CHARACTERISTICS

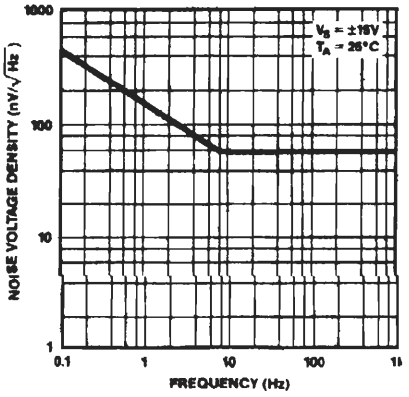
POWER SUPPLY REJECTION vs FREQUENCY



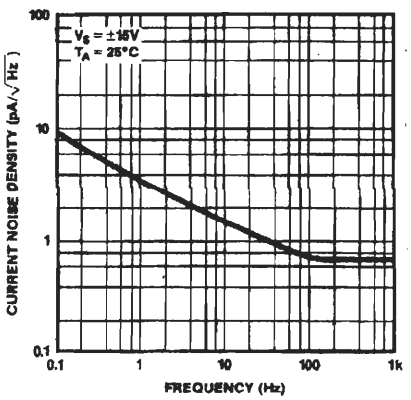
COMMON-MODE REJECTION vs FREQUENCY



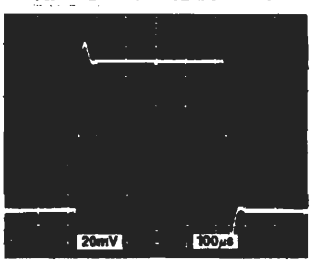
NOISE VOLTAGE DENSITY vs FREQUENCY



CURRENT NOISE DENSITY vs FREQUENCY

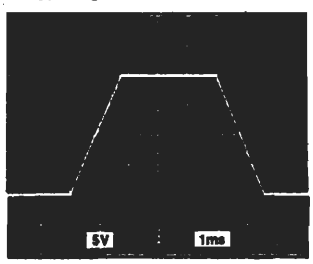


SMALL-SIGNAL TRANSIENT RESPONSE



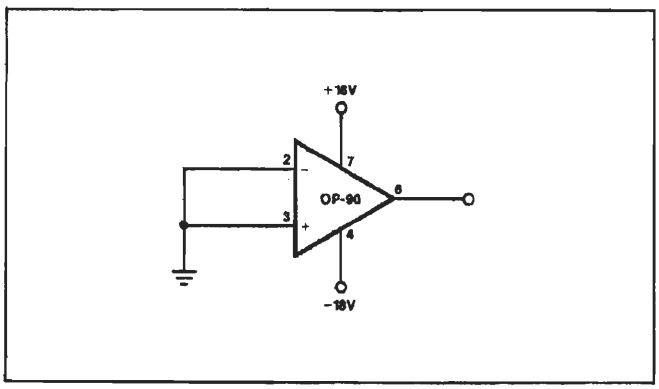
T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

LARGE-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

BURN-IN CIRCUIT



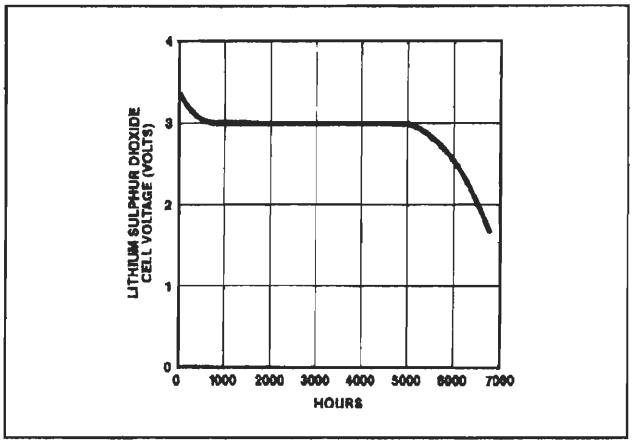
APPLICATIONS INFORMATION

BATTERY-POWERED APPLICATIONS

The OP-90 can be operated on a minimum supply voltage of +1.6V, or with dual supplies ±0.8V, and draws only 14µA of supply current. In many battery-powered circuits, the OP-90 can be continuously operated for thousands of hours before requiring battery replacement, reducing equipment down-time and operating cost.

High-performance portable equipment and instruments frequently use lithium cells because of their long shelf-life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3V and are noted for a flat discharge characteristic. The low supply voltage requirement of the OP-90, combined with the flat discharge characteristic of the lithium cell, indicates that the OP-90 can be operated over the entire useful life of the cell. Figure 1 shows the typical discharge characteristic of a 1Ah lithium cell powering an OP-90 which, in turn, is driving full output swing into a 100kΩ load.

FIGURE 1: Lithium Sulphur Dioxide Cell Discharge Characteristic With OP-90 and 100kΩ Load



INPUT VOLTAGE PROTECTION

The OP-90 uses a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors coupled with the protection resistors provides a large amount of input protection, allowing the inputs to be taken 20V beyond either supply without damaging the amplifier.

OFFSET NULLING

The offset null circuit of Figure 2 provides 6mV of offset adjustment range. A 100kΩ resistor placed in series with the wiper of the offset null potentiometer, as shown in Figure 3, reduces the offset adjustment range to 400μV and is recommended for applications requiring high null resolution. Offset nulling does not affect TCV_{OS} performance.

FIGURE 2: Offset Nulling Circuit

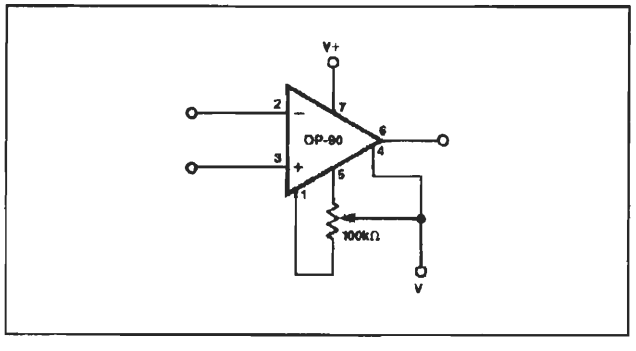
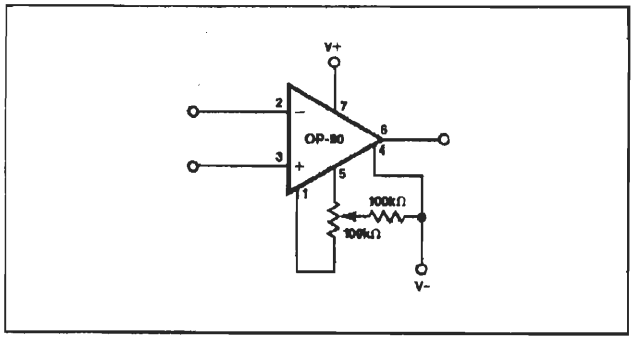


FIGURE 3: High Resolution Offset Nulling Circuit



SINGLE-SUPPLY OUTPUT VOLTAGE RANGE

In single-supply operation the OP-90's input and output ranges include ground. This allows true "zero-in, zero-out" operation. The output stage provides an active pull-down to around 0.8V above ground. Below this level, a load resistance of up to 1MΩ to ground is required to pull the output down to zero.

In the region from ground to 0.8V the OP-90 has voltage gain equal to the data sheet specification. Output current source capability is maintained over the entire voltage range including ground.

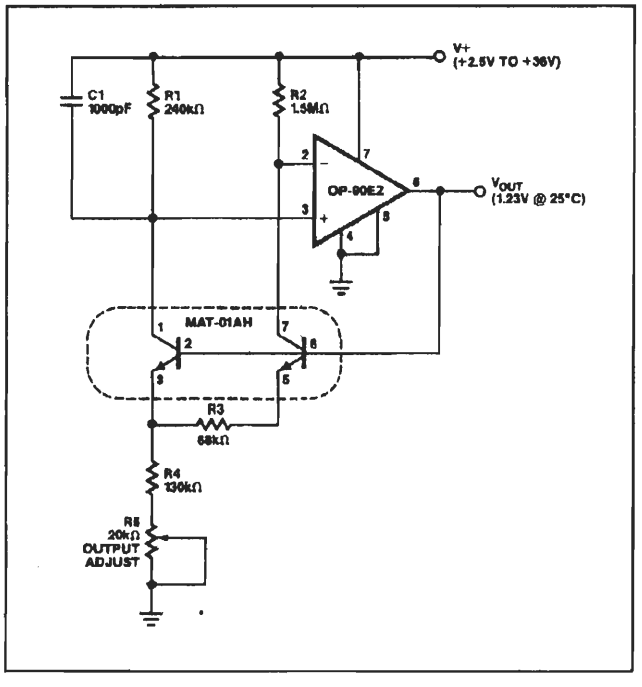
APPLICATIONS

BATTERY-POWERED VOLTAGE REFERENCE

The circuit of Figure 4 is a battery-powered voltage reference that draws only 17μA of supply current. At this level, two AA cells can power this reference over 18 months. At an output voltage of 1.23V @ 25°C, drift of the reference is only 5.5μV/°C over the industrial temperature range. Load regulation is 85μV/mA with line regulation at 120μV/V.

Design of the reference is based on the bandgap technique. Scaling of resistors R1 and R2 produces unequal currents in Q1 and Q2. The resulting V_{BE} mismatch creates a temperature-proportional voltage across R3 which, in turn, produces a larger temperature-proportional voltage across R4 and R5. This voltage appears at the output added to the V_{BE} of Q1, which has an opposite temperature coefficient. Adjusting the

FIGURE 4: Battery Powered Voltage Reference



output to 1.23V at 25°C produces minimum drift over temperature. Bandgap references can have start-up problems. With no current in R1 and R2, the OP-90 is beyond its positive input range limit and has an undefined ouput state. Shorting Pin 5 (an offset adjust pin) to ground forces the output high under these conditions and insures reliable start-up without significantly degrading the OP-90's offset drift.

SINGLE OP AMP FULL-WAVE RECTIFIER

Figure 5 shows a full-wave rectifier circuit that provides the absolute value of input signals up to ±2.5V even though operated from a single 5V supply. For negative inputs, the amplifier acts as an unity gain inverter. Positive signals force the op amp output to ground. The 1N914 diode becomes reversed-biased and the signal passes through R1 and R2 to the output. Since output impedance is dependent on input polarity, load impedances cause an asymmetric output. For constant load impedances, this can be corrected by reducing R2. Varying or heavy loads can be buffered by a second OP-90. Figure 6 shows the output of the full-wave rectifier with a $4V_{p-p}$, 10Hz input signal.

FIGURE 5: Single Op-Amp Full Wave Rectifier

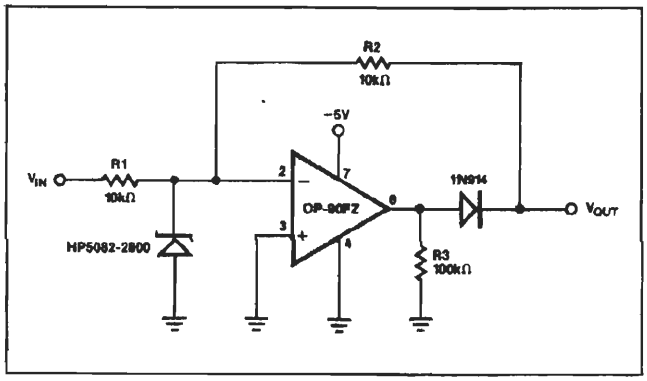
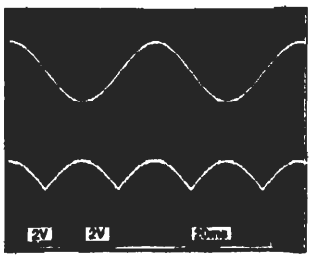


FIGURE 6: Output of Full-Wave Rectifier With $4V_{p-p}$, 10Hz Input



TWO WIRE 4-20mA CURRENT TRANSMITTER

The current transmitter of Figure 7 provides an output of 4mA to 20mA that is linearly proportional to the input voltage. Linearity of the transmitter exceeds 0.004% and line rejection is 0.0005%/volt.

Biasing for the current transmitter is provided by the REF-02EZ. The OP-90EZ regulates the output current to satisfy the current summation at the noninverting node:

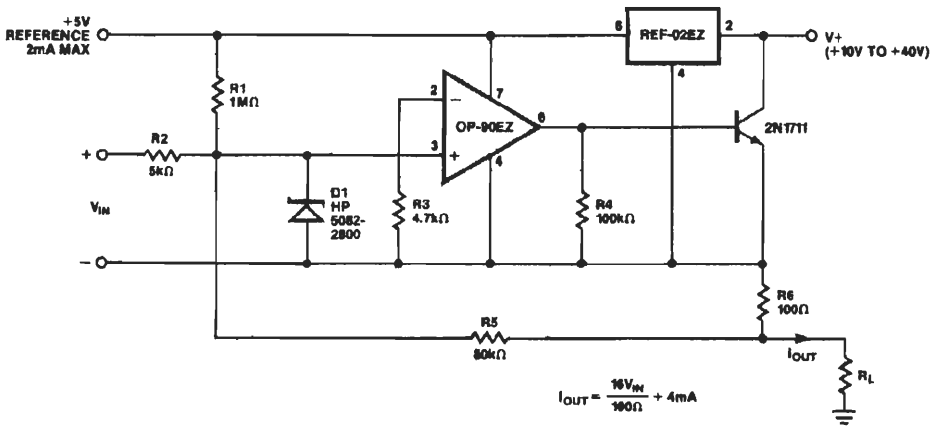
$$I_{OUT} = \frac{1}{R6}\left(\frac{V_{IN}\,R5}{R2} + \frac{5V\,R5}{R1}\right)$$

For the values shown in Figure 7,

$$I_{OUT} = \left(\frac{16}{100\Omega}\right)V_{IN} + 4mA$$

giving a full-scale output of 20mA with a 100mV input. Adjustment of R2 will provide an offset trim and adjustment of R1 will provide a gain trim. These trims do not interact since the noninverting input of the OP-90 is at virtual ground. The Schottky diode, D1, prevents input voltage spikes from pull-

FIGURE 7: Two Wire 4-20mA Transmitter



ing the noninverting input more than 300mV below the inverting input. Without the diode, such spikes could cause phase reversal of the OP-90 and possible latch-up of the transmitter. Compliance of this circuit is from 10V to 40V. The voltage reference output can provide up to 2mA for transducer excitation.

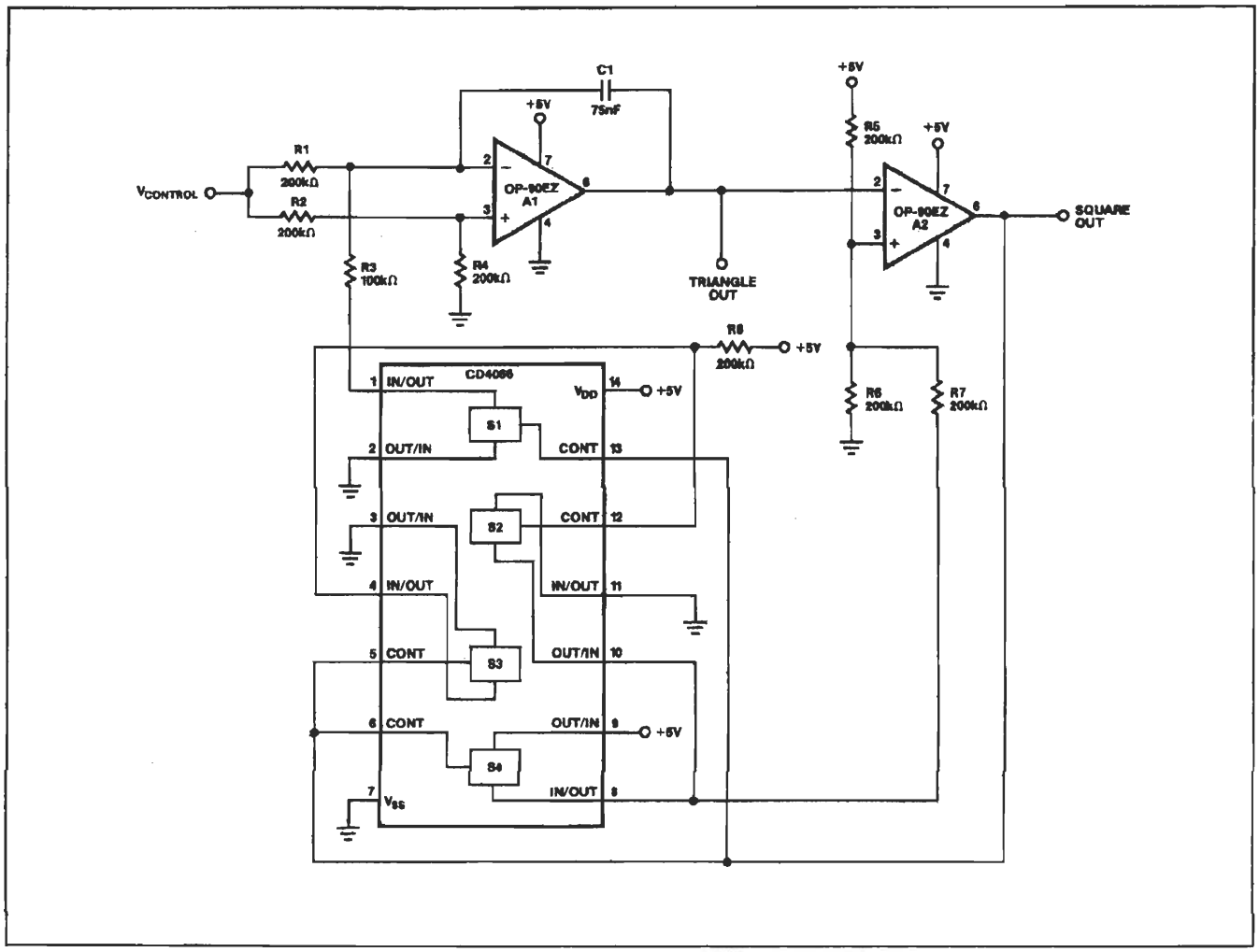
MICROPOWER VOLTAGE-CONTROLLED OSCILLATOR

Two OP-90s in combination with an inexpensive quad CMOS switch comprise the precision VCO of Figure 8. This circuit provides triangle and square wave outputs and draws only 50μA from a single 5V supply. A1 acts as an integrator; S1 switches the charging current symmetrically to yield positive and negative ramps. The integrator is bounded by A2 which acts as a Schmitt trigger with a precise hysteresis of 1.67 volts, set by resistors R5, R6, and R7, and associated CMOS switches. The resulting output of A1 is a triangle wave with upper and lower levels of 3.33 and 1.67 volts. The output of A2 is a square wave with almost rail-to-rail swing. With the components shown, frequency of operation is given by the equation:

$$f_{OUT} = V_{CONTROL}\ (\text{volts}) \times 10\text{Hz/V}$$

but this is easily changed by varying C1. The circuit operates well up to a few hundred hertz.

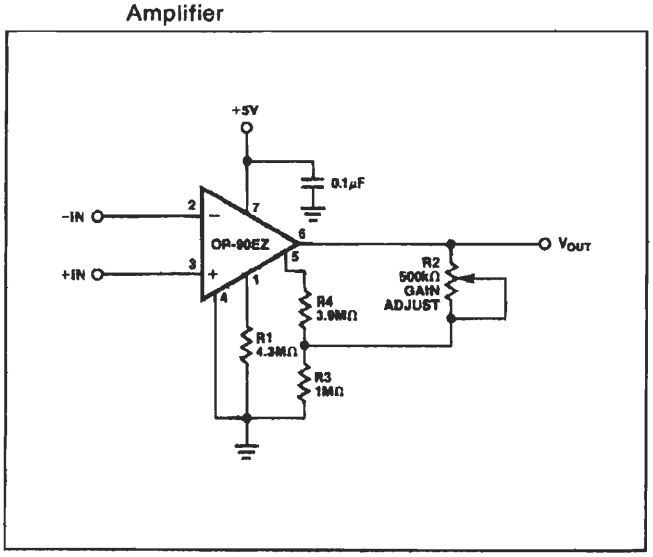
FIGURE 8: Micropower Voltage Controlled Oscillator



MICROPOWER SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER

The simple instrumentation amplifier of Figure 9 provides over 110dB of common-mode rejection and draws only 15μA of supply current. Feedback is to the trim pins rather than to the inverting input. This enables a single amplifier to provide differential to single-ended conversion with excellent common-mode rejection. Distortion of the instrumentation amplifier is that of a differential pair, so the circuit is restricted to high gain applications. Nonlinearity is less than 0.1% for gains of 500 to 1000 over a 2.5V output range. Resistors R3 and R4 set the voltage gain and, with the values shown, yield a gain of 1000. Gain tempco of the instrumentation amplifier is only 50ppm/°C. Offset voltage is under 150μV with drift below 2μV/°C. The OP-90's input and output voltage ranges include the negative rail which allows the instrumentation amplfier to provide true "zero-in, zero-out" operation.

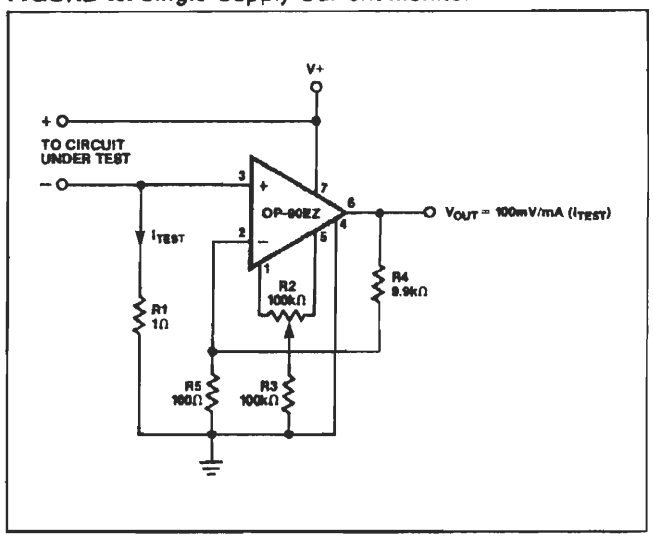
FIGURE 9: Micropower Single-Supply Instrumentation Amplifier



SINGLE-SUPPLY CURRENT MONITOR

Current monitoring essentially consists of amplifying the voltage drop across a resistor placed in series with the current to be measured. The difficulty is that only small voltage drops can be tolerated and with low precision op amps this greatly limits the overall resolution. The single-supply current monitor of Figure 10 has a resolution of 10μA and is capable of monitoring 30mA of current. This range can be adjusted by changing the current sense resistor R1. When measuring total system current, it may be necessary to include the supply current of the current monitor, which bypasses the current sense resistor, in the final result. This current can be measured and calibrated (together with the residual offset) by adjustment of the offset trim potentiometer, R2. This produces a deliberate offset that is temperature dependent. However, the supply current of the OP-90 is also proportional to temperature and the two effects tend to track. Current in R4 and R5, which also bypasses R1, can be accounted for by a gain trim.

FIGURE 10: Single-Supply Current Monitor



Appendix H – AD654 Voltage to Frequency Converter

Manufactured by Analog Devices
1 Technology Way
P.O. Box 9106
Norwood, MA 02062
(800) 262-5643

ANALOG DEVICES

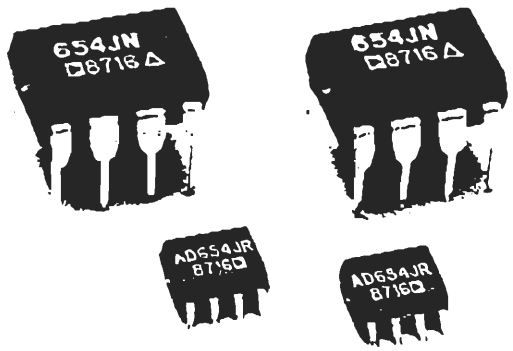
(8)

Low Cost Monolithic Voltage-to-Frequency Converter

AD654

FEATURES

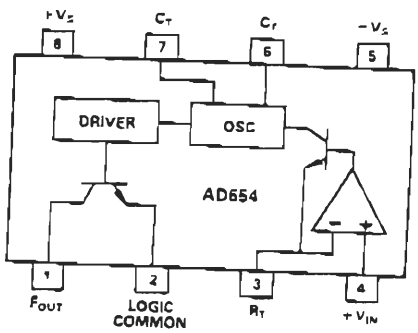
- Low Cost
- Single or Dual Supply, 5 to 36 Volts, ±5V to ±18V
- Full Scale Frequency Up to 500kHz
- Minimum Number of External Components Needed
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Low Power: 2.0mA Quiescent Current
- Low Offset: 1mV



PRODUCT DESCRIPTION

The AD654 is a monolithic V/F converter consisting of an input amplifier, a precision oscillator system, and a high current output stage. A single RC network is all that is required to set up any full scale (F.S.) frequency up to 500kHz and any F.S. input voltage up to ±30V. Linearity error is only 0.03% for a 250kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±50ppm/°C. The AD654 operates from a single supply of 5 to 36V and consumes only 2.0mA quiescent current.

The low drift (4μV/°C typ) input amplifier allows operation directly from small signals such as thermocouples or strain gauges while offering a high (250MΩ) input resistance. Unlike most V/F converters, the AD654 provides a square-wave output, and can drive up to 12 TTL loads, opto-couplers, long cables, or similar loads.



AD654 Pin Configuration

PRODUCT HIGHLIGHTS

1. Packaged in both an 8-pin mini-DIP and an 8-pin SOIC package, the AD654 is a complete V/F converter requiring only an RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of the timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, $f = V/10RC$.
2. A minimum number of low cost external components are necessary. A single RC network is all that is required to set up any full scale frequency up to 500kHz and any full scale input voltage up to ±30V.
3. Plastic packaging allows low cost implementation of the standard VFC applications: A/D conversion, isolated signal transmission, F/V conversion, phase-locked loops, and tuning switched-capacitor filters.
4. Power supply requirements are minimal; only 2.0mA of quiescent current is drawn from the single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to $(+V_S - 4)$ volts. Negative inputs can easily be connected for below ground operation.
5. The versatile open-collector output stage can sink more than 10mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

One Technology Way; P. O. Box 9106; Norwood, MA 02062-9106 U.S.A.
Tel: 617/329-4700
Telex: 924491
Twx: 710/394-6577
Cables: ANALOG NORWOODMASS

SPECIFICATIONS (t_{AMB} = +25°C and V_S (total) = 5 to 16.5V, unless otherwise specified. All testing done @ V_S = +5V)

Model	AD654JN/JR Min	Typ	Max	Units
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0		500	kHz
Nonlinearity[1]				
f_{max} = 250kHz		0.06	**0.1**	%
f_{max} = 500kHz		0.20	0.4	%
Full Scale Calibration Error				
C = 390pF, I_{IN} = 1.000mA	**−10**		**10**	%
vs. Supply ($f_{max} \leq$ 250kHz)				
V_S = +4.75 to +5.25V		0.20	**0.40**	%/V
V_S = +5.25 to +16.5V		0.05	**0.10**	%/V
vs. Temp (0 to 70°C)		50		ppm/°C
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0		(+V_S −4)	V
Dual Supply	−V_S		(+V_S −4)	V
Input Bias Current				
(Either Input)		30	**50**	nA
Input Offset Current		5		nA
Input Resistance (Non-Inverting)		250		MΩ
Input Offset Voltage		0.5	**1.0**	mV
vs. Supply				
V_S = +4.75 to +5.25V		0.1	**0.25**	mV/V
V_S = +5.25 to +16.5V		0.03	**0.1**	mV/V
vs. Temp (0 to 70°C)		4		µV/°C
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"[2]				
V_{OUT} = 0.4V max, 25°C	**10**	20		mA
V_{OUT} = 0.4V max, 0 to 70°C	5	10		mA
Output Leakage Current in Logic "1"		10	**100**	nA
0 to 70°C		50	500	nA
Logic Common Level Range	−V_S		(+V_S −4)	V
Rise/Fall Times (C_T = 0.01µF)				
I_{IN} = 1mA		0.2		µs
I_{IN} = 1µA		1		µs
POWER SUPPLY				
Voltage, Rated Performance	4.5		16.5	V
Voltage, Operating Range				
Single Supply	4.5		36	V
Dual Supply	±5		±18	V
Quiescent Current				
V_S (Total) = 5V		1.5	**2.5**	mA
V_S (Total) = 30V		2.0	**3.0**	mA
TEMPERATURE RANGE				
Operating Range	−40		85	°C
PACKAGE OPTIONS				
SOIC		AD654JR		
Plastic DIP		AD654JN		

NOTES

[1]At f_{max} = 250kHz: R_T = 1kΩ, C_T = 390pF, I_{IN} = 0-1mA.
f_{max} = 500kHz: R_T = 1kΩ, C_T = 200pF, I_{IN} = 0-1mA.

[2]The sink current is the amount of current that can flow into Pin 1 of the AD654 while maintaining a maximum voltage of 0.4V between Pin 1 and Logic Common.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

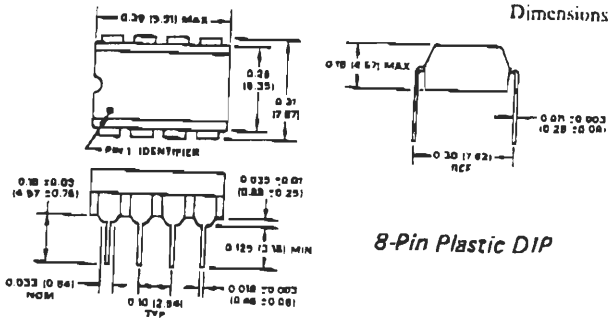
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

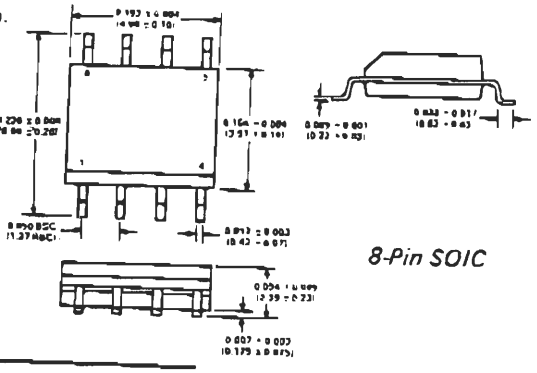
Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage
(Pins 3, 4) to $-V_S$ . . . . . $-300mV$ to $+V_S$
Maximum Output Current
Instantaneous 50mA
Sustained 25mA
Logic Common to $-V_S$ . . . . . $-500mV$ to $(+V_S - 4)$
Storage Temperature Range . . . . . $-65°C$ to $+150°C$

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



8-Pin Plastic DIP



8-Pin SOIC

CIRCUIT OPERATION

The AD654's block diagram appears in Figure 1. A versatile operational amplifier serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter (an astable multivibrator). The drive current provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 100nA to 2mA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a level other than $-V_S$.

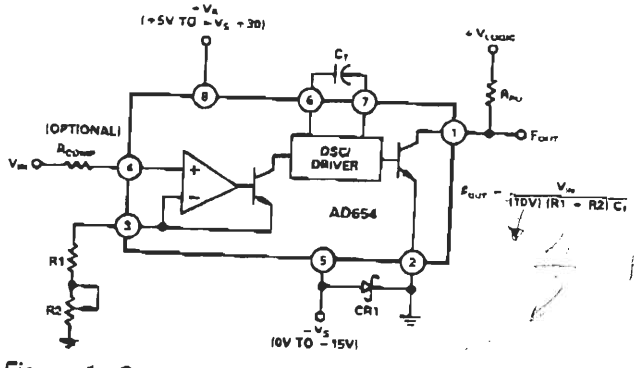


Figure 1. Standard V-F Connection for Positive Input Voltages

V/F CONNECTION FOR POSITIVE INPUT VOLTAGES

In the connection scheme of Figure 1, the input amplifier presents a very high (250MΩ) impedance to the input voltage, which is converted into the proper drive current by the scaling resistors at pin 3. Resistors R1 and R2 are selected to provide a 1mA full scale current with enough trim range to accommodate the AD654's 10% FS error and the components' tolerances. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive. The AD654's positive input voltage range spans from $-V_S$ (ground in single supply operation) to four volts below the positive supply. Power supply rejection degrades as the input exceeds $(+V_S - 3.75V)$ and at $(+V_S - 3.5V)$ the output frequency goes to zero.

As indicated by the scaling relationship in Figure 1, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. Good V/F linearity requires the use of a capacitor with low dielectric absorption (DA), while the most stable operation over temperature calls for a component having a small tempco. Polystyrene, polypropylene, or Teflon* capacitors are preferred for tempco and dielectric absorption; other types will degrade linearity. The capacitor should be wired very close to the AD654. In Figure 1, Schottky diode CR1 (MBD101) prevents logic common from dropping more than 500mV below $-V_S$. This diode is not required if $-V_S$ is equal to logic common.

V/F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

The AD654 can accommodate a wide range of negative input voltages with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance because the signal source must supply the 1mA F.S. drive current. However, large negative voltages beyond the supply can be handled easily by modifying the scaling resistors appropriately. If the input is a true current source, R1 and R2 are not used. Again, diode CR1 prevents latch-up by insuring Logic Common does not drop more than 500mV below $-V_S$. The clamp diode (MBD101) protects the AD654 input from "below $-V_S$" inputs.

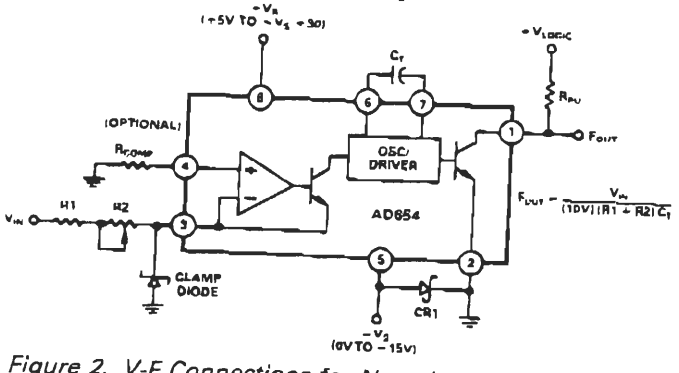


Figure 2. V-F Connections for Negative Input Voltages or Current

*Teflon is a trademark of E. I. Du Pont de Nemours & Co.

OFFSET CALIBRATION

In theory, two adjustments calibrate a V/F: scale and offset. In practice, most applications find the AD654's 1mV max voltage offset sufficiently low to forgo offset calibration. However, the input amplifier's 30nA (typ) bias currents will generate an offset due to the difference in DC source resistance between the input terminals. This offset can be substantial for large values of $R_T = R_1 + R_2$ and will vary as the bias currents drift over temperature. Therefore, to maintain the AD654's low offset, the application may require balancing the DC source resistances at the inputs (pins 3 and 4).

For positive inputs, this is accomplished by adding a compensation resistor nominally equal to R_T in series with the input as shown in Figure 3a. This limits the offset to the product of the 30nA bias current and the mismatch between the source resistance R_T and R_{COMP}. A second, smaller offset arises from the inputs' 5nA offset current flowing through the source resistance R_T or R_{COMP}. For negative input voltage and current connections, the compensation resistor is added at pin 4 as shown in Figure 3b in lieu of grounding the pin directly. For both positive and negative inputs, the use of R_{COMP} may lead to noise coupling at pin 4 and should therefore be bypassed for lowest noise operation.

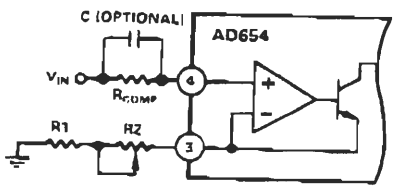


Figure 3a. Bias Current Compensation – Positive Inputs

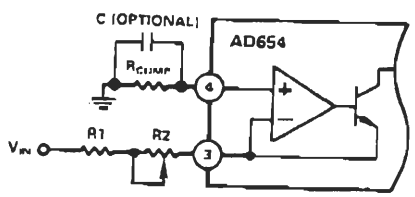


Figure 3b. Bias Current Compensation – Negative Inputs

If the AD654's 1mV offset voltage must be trimmed, the trim must be performed external to the device. Figure 3c shows an optional connection for positive inputs in which R_{OFF1} and R_{OFF2} add a variable resistance in series with R_T. A variable source of ±0.6V applied to R_{OFF1} then adjusts the offset ±1mV. Similarly, a ±0.6V variable source is applied to R_{OFF} in Figure 3d to trim offset for negative inputs. The ±0.6V bipolar source could simply be an AD589 reference connected as shown in Figure 3e.

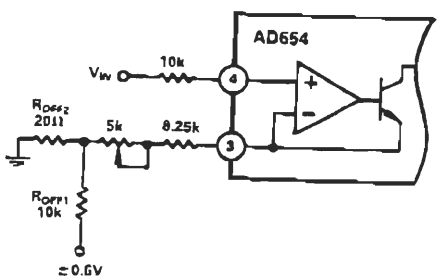


Figure 3c. Offset Trim Positive Input (10V FS)

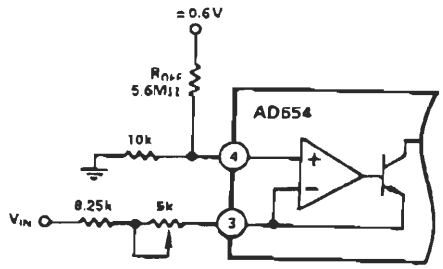


Figure 3d. Offset Trim Negative Input (–10V FS)

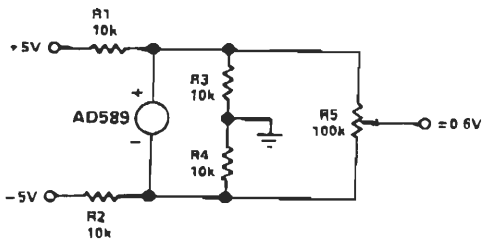


Figure 3e. Offset Trim Bias Network

FULL SCALE CALIBRATION

Full scale trim is the calibration of the circuit to produce the desired output frequency with a full scale input applied. In most cases this is accomplished by adjusting the scaling resistor R_T. Precise calibration of the AD654 requires the use of an accurate voltage standard set to the desired FS value and an accurate frequency meter. A scope is handy for monitoring output waveshape. Verification of converter linearity requires the use of a switchable voltage source or DAC having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. Since each AD654 is factory tested for linearity, it is unnecessary for the end-user to perform this tedious and time consuming test on a routine basis.

Sufficient FS calibration trim range must be provided to accommodate the worst-case sum of all major scaling errors. This includes the AD654's 10% full scale error, the tolerance of the fixed scaling resistor, and the tolerance of the timing capacitor. Therefore, with a resistor tolerance of 1% and a capacitor tolerance of 5%, the fixed part of the scaling resistor should be a maximum of 84% of nominal, with the variable portion selected to allow 116% of the nominal.

If the input is in the form of a negative current source, the scaling resistor is no longer required, eliminating the capability of trimming FS frequency in this fashion. Since it is usually not practical to smoothly vary the capacitance for trimming purposes, an alternative scheme such as the one shown in Figure 4 is needed. Designed for a FS of 1mA, this circuit divides the input into two current paths. One path is through the 100Ω

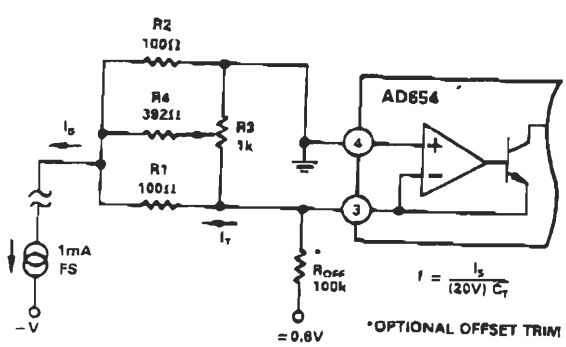


Figure 4. Current Source FS Trim

H-4

resistor R1, and flowing into pin 3; it constitutes the signal current I_T to be converted. The second path, through another 100Ω resistor R2, carries the same nominal current. Two equal valued resistors offer the best overall stability, and should be either 1% discrete film units, or a pair from a common array.

Since the 1mA FS input current is divided into two 500μA legs (one to ground and one to pin 3), the total input signal current (I_S) is divided by a factor of two in this network. To achieve the same conversion scale factor, C_T must be reduced by a factor of two. This results in a transfer unique to this hookup:

$$f = \frac{I_S}{(20V)\, C_T}$$

For calibration purposes, resistors R3 and R4 are added to the network, allowing a ±15% trim of scale factor with the values shown. By varying R4's value the trim range can be modified to accommodate wider tolerance components or perhaps the calibration tolerance on a current output transducer such as the AD592 temperature sensor. Although the values of R1 – R4 shown are valid for 1mA FS signals only, they can be scaled upward proportionately for lower FS currents. For instance, they should be increased by a factor of ten for a FS current of 100μA.

In addition to the offsets generated by the input amplifier's bias and offset currents, an offset voltage induced parasitic current arises from the current fork input network. These effects are minimized by using the bias current compensation resistor R_{OFF} and offset trim scheme shown in Figure 3e.

Although device warmup drifts are small, it is good practice to allow the devices operating environment to stabilize before trim, and insure the supply, source and load are appropriate. If provision is made to trim offset, begin by setting the input to 1/10,000 of full scale. Adjust the offset pot until the output is 1/10,000 of full scale (for example, 25Hz for a FS of 250kHz). This is most easily accomplished using a frequency meter connected to the output. The FS input should then be applied and the gain pot should be adjusted until the desired FS frequency is indicated.

INPUT PROTECTION

The AD654 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions. Thus $+V_{IN}$ and R_T pins should not be driven more than 300mV below $-V_S$. Likewise, Logic Common should not drop more than 500mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. In addition to the diode shown in Figures 1 and 2 protecting Logic Common, a second Schottky diode (MBD101) can protect the AD654's inputs from "below $-V_S$" inputs as shown in Figure 5. It is also desirable not to drive $+V_{IN}$ and R_T above $+V_S$. In operation, the converter will exhibit a zero output for inputs above ($+V_S - 3.5V$). Also, control currents above 2mA will increase nonlinearity.

The AD654's 80dB dynamic range guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to input. For example, when scaled to accept an FS input of 1V, the −80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes

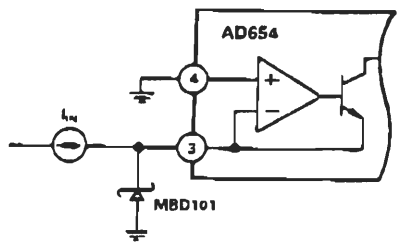


Figure 5. Input Protection

of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter or a guard ring around the R_T pin. The filter can be assembled using the bias current compensation resistor discussed in the previous section. For an FS of 10kHz, a single-pole filter with a time constant of 100ms will be suitable, but the optimum configuration will depend on the application and the type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA full integration of additive input noise occurs. Like the inputs, the capacitor terminals are sensitive to interference from other signals. The timing capacitor should be located as close as possible to the AD654 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in the system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD654. A proper ground scheme appears in Figure 6.

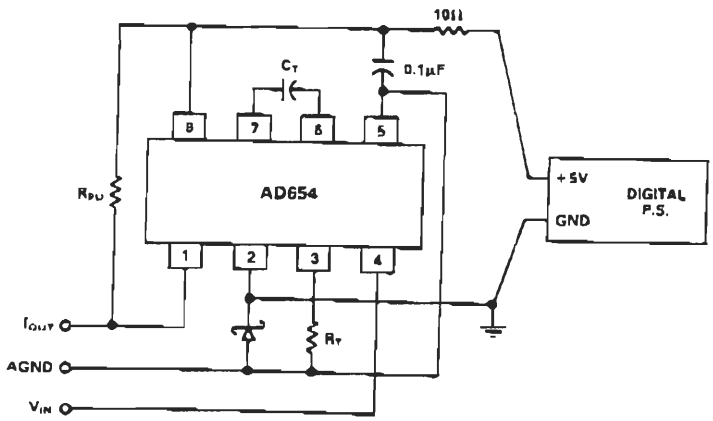


Figure 6. Proper Ground Scheme

OUTPUT INTERFACING CONSIDERATIONS

The output stage's design allows easy interfacing to all digital logic families. The output NPN transistor's emitter and collector are both uncommitted. The emitter can be tied to any voltage between $-V_S$ and 4 volts below $+V_S$, and the open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can sink over 10mA at a maximum saturation voltage of 0.4V. The stage limits the output current at 25mA and can handle this limit indefinitely without damaging the device.

The preferred method of specifying nonlinearity error is in terms of maximum deviation from the ideal relationship after calibrating the converter at full scale. This error will vary with the full scale frequency and the mode of operation. The AD654 operates best at a 150kHz full scale frequency with a negative voltage input; the linearity is typically within 0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicated in the Specifications Table. Typical linearity at various temperatures is shown in Figure 7.

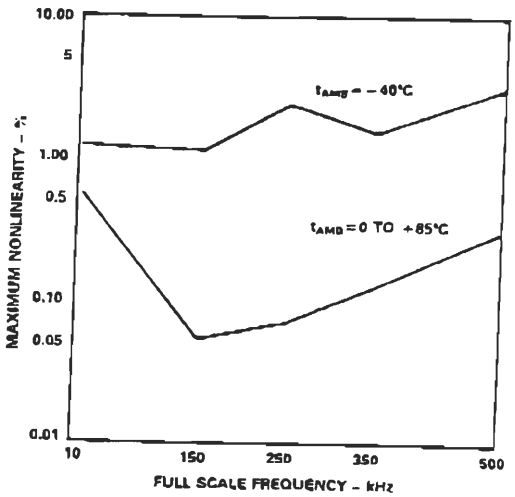


Figure 7. Typical Nonlinearities at Different Full-Scale Frequencies

TWO-WIRE TEMPERATURE-TO-FREQUENCY CONVERSION

Figure 8 shows the AD654 in a two-wire temperature-to-frequency conversion scheme. The twisted pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation.

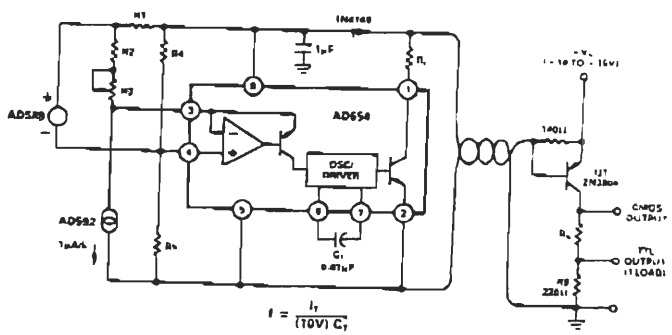


Figure 8. Two-Wire Temperature-to-Frequency Converter

The positive supply line is fed to the remote V/F through a 140Ω resistor. This resistor is selected such that the quiescent current of the AD654 will cause less than one V_{BE} to be dropped. As the V/F oscillates, additional switched current is drawn through R_L when pin 1 goes low. The peak level of this additional current causes Q1 to saturate, and thus regenerates the AD654's output square wave at the collector. The supply voltage to the AD654 then consists of a DC level, less the resistive line drop, plus a one V_{BE} p-p square wave at the output frequency of the AD654. This ripple is reduced by the diode/capacitor combination.

To set up the receiver circuit for a given voltage, the R_S and R_L resistances are selected as shown in Table I. CMOS logic stages can be driven directly from the collector of Q1, and a single TTL load can be driven from the junction of R_S and R6.

$+V_S$	R_S	R_L
10V	270Ω	1.8k
15V	680Ω	2.7k

Table I.

	$(+V_S)$	R1	R2	R3	R4	R5	
K	10V	–	–	–	100k	127k	F = 10Hz/K
	15V	–	–	–	100k	127k	
°C	10V	6.49k	4.02k	1k	95.3k	22.6k	F = 10Hz/°C
	15V	12.7k	4.02k	1k	78.7k	36.5k	
°F	10V	6.49k	4.42k	1k	154k	22.6k	F = 5.55Hz/°F
	15V	12.7k	4.42k	1k	105k	36.5k	

Table II.

At the V/F end, the AD592C temperature transducer is interfaced with the AD654 in such a manner that the AD654 output frequency is proportional to temperature. The output frequency can be scaled and offset from K to °C or °F using the resistor values shown in Table II. Since temperature is the parameter of interest, an NPO ceramic capacitor is used as the timing capacitor for low V/F TC.

When scaling per K, resistors R1 – R3 and the AD589 voltage reference are not used. The AD592 produces a 1μA/K current output which drives pin 3 of the AD654. With the timing capacitor of 0.01μF this produces an output frequency scaled to 10Hz/K. When scaling per °C and °F, the AD589 and resistors R1 – R3 offset the drive current at pin 3 by 273.2μA for scaling per °C and 255.42μA for scaling per °F. This will result in frequencies scaled at 10Hz/°C and 5.55Hz/°F, respectively.

OPTOISOLATOR COUPLING

A popular method of isolated signal coupling is via optoelectronic isolators, or optocouplers. In this type of device, the signal is coupled from an input LED to an output photo-transistor, with light as the connecting medium. This technique allows DC to be transmitted, is extremely useful in overcoming ground loop problems between equipment, and is applicable over a wide range of speeds and power.

Figure 9 shows a general purpose isolated V/F circuit using a low cost 4N37 optoisolator. A +5V power supply is assumed for both the isolated (+5V isolated) and local (+5V local) supplies. The input LED of the isolator is driven from the collector output of the AD654, with a 9mA current level established by R1 for high speed, as well as for a 100% current transfer ratio.

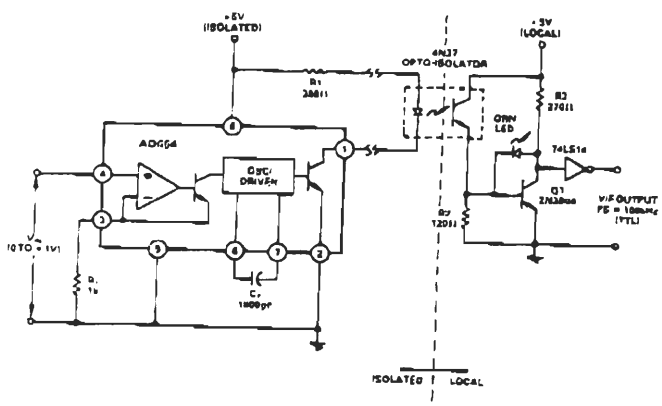


Figure 9. Optoisolator Interface

At the receiver side, the output transistor is operated in the photo-transistor mode; that is with the base lead (pin 6) open. This allows the highest possible output current. For reasonable speed in this mode, it is imperative that the load impedance be as low as possible. This is provided by the single transistor stage current-to-voltage converter, which has a dynamic load impedance of less than 10 ohms and interfaces with TTL at the output.

USING A STAND-ALONE FREQUENCY COUNTER/LED DISPLAY DRIVER FOR VOLTMETER APPLICATIONS

Figure 10 shows the AD654 used with a stand-alone frequency counter/LED display driver. With C_T = 1000pF and R_T = 1kΩ the AD654 produces an FS frequency of 100kHz when V_{IN} = +1V. This signal is fed into the ICM7226A, a universal counter system that drives common anode LED's. With the FUNCTION pin tied to D1 through a 10kΩ resistor the ICM7226A counts the frequency of the signal at A_{IN}. This count period is selected by the user and can be 10ms, 100ms, 1s, or 10 seconds, as shown on pin 21. The longer the period selected, the more resolution the count will have. The ICM7226A then displays the frequency on the LED's, driving them directly as shown. Refreshing of the LED's is handled automatically by the ICM7226. The entire circuit operates on a single +5V supply and gives a meter with 3, 4, or 5 digit resolution.

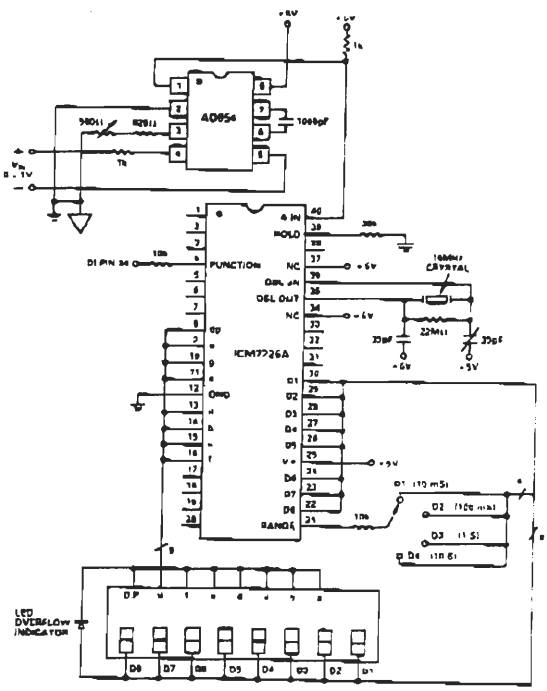


Figure 10. AD654 With Stand-Alone Frequency Counter/LED Display Driver

Longer count periods not only result in the count having more resolution, they also serve as an integration of noisy analog signals. For example, a normal-mode 60Hz sine wave riding on the input of the AD654 will result in the output frequency increasing on the positive half of the sine wave and decreasing on the negative half of the sine wave. This effect is cancelled by selecting a count period equal to an integral number of noise signal periods. A 100ms count period is effective because it not only has an integral number of 60Hz cycles (6), it also has an integral number of 50Hz cycles (5). This is also true of the 1 second and 10 second count period.

AD654-BASED ANALOG-TO-DIGITAL CONVERSION USING A SINGLE CHIP MICROCOMPUTER

The AD654 can serve as an analog-to-digital converter when used with a single component microcomputer that has an interval timer/event counter such as the 8048. Figure 11 shows the AD654, with a full scale input voltage of +1V and a full scale output frequency of 100kHz, connected to the timer/counter input pin T1 of the 8048. Such a system can also operate on a single +5V supply.

The 8748 counter is negative edge triggered; after the STRT CNT instruction is executed subsequent high to low transitions on T1 increment the counter. The maximum rate at which the counter may be incremented is once per three instruction cycles; using a 6MHz crystal, this corresponds to once every 7.5μs, or a maximum frequency of 133kHz. Because the counter overflows every 256 counts (8 bits), the timer interrupt is enabled. Each overflow then causes a jump to a subroutine where a register is incremented. After the STOP TCNT instruction is executed, the number of overflows that have occurred will be the number in this register. The number in this register multiplied by 256 plus the number in the counter will be the total number of negative edges counted during the count period. The count period is handled simply by decrementing a register the number of times necessary to correspond to the desired count time. After the register has been decremented the required number of times, the STOP TCNT instruction is executed.

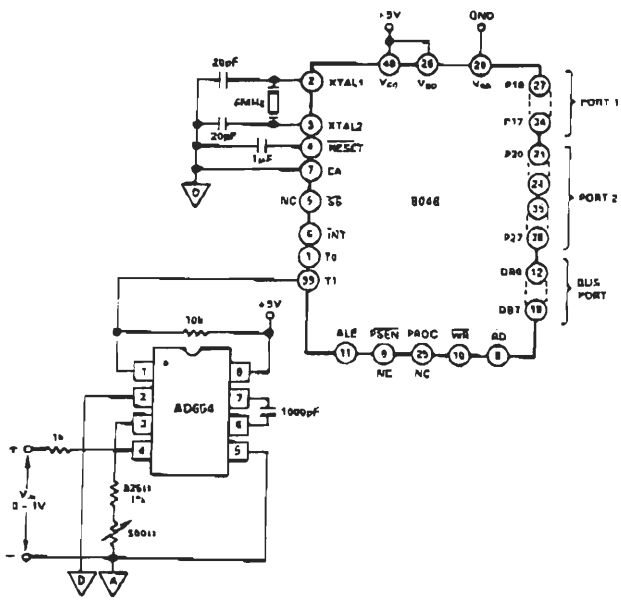


Figure 11. AD654 VFC as an ADC

The total number of negative edges counted during the count period is proportional to the input voltage. For example, if a 1V full-scale input voltage produces a 100kHz signal and the count period is 100ms, then the total count will be 10,000. Scaling from this maximum is then used to determine the input voltage, i.e., a count of 5000 corresponds to an input voltage of 0.5V. As with the ICM7226, longer count times result in counts having more resolution; and they result in the integration of noisy analog signals.

FREQUENCY DOUBLING

Since the AD654's output is a square-wave rather than a pulse train, information about the input signal is carried on both halves of the output waveform. The circuit in Figure 12 converts the output into a pulse train, effectively doubling the output frequency, while preserving the better low frequency linearity of the AD654. This circuit also accommodates an input voltage that is greater than the AD654 supply voltage.

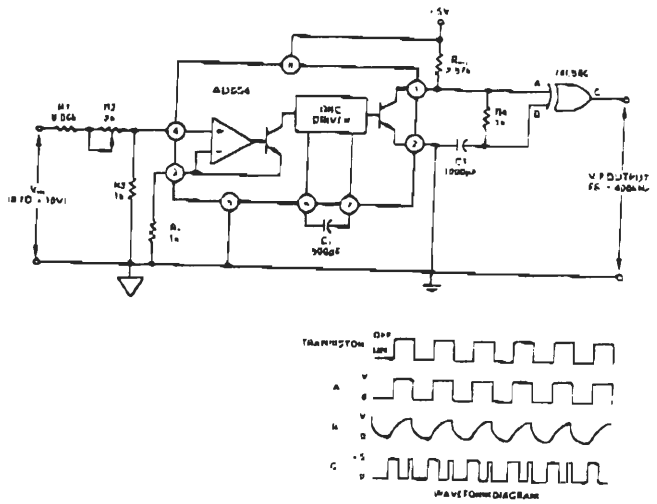


Figure 12. Frequency Doubler

Resistors R1 – R3 are used to scale the 0 to +10V input voltage down to 0 to +1V as seen at pin 4 of the AD654. Recall that V_{IN} must be less than V_{SUPPLY} −4V, or in this case less than 1V. The timing resistor and capacitor are selected such that this 0 to +1V signal seen at pin 4 results in a 0 to 200kHz output frequency.

The use of R4, C1 and the XOR gate doubles this 200kHz output frequency to 400kHz. The AD654 output transistor is basically used as a switch, switching capacitor C1 between a charging mode and a discharging mode of operation. The voltages seen at the input of the 74LS86 are shown in the waveform diagram. Due to the difference in the charge and discharge time constants, the output pulse widths of the 74LS86 are not equal. The output pulse is wider when the capacitor is charging due to its longer rise time than fall time. The pulses should therefore be counted on their rising, rather than falling, edges.

OPERATION AT HIGHER OUTPUT FREQUENCIES

Operation of the AD654 via the conventional output (pins 1 and 2) is speed limited to approximately 500kHz for reasons of TTL logic compatibility. Although the output stage may become speed limited, the multivibrator core itself is able to oscillate to 1MHz or more. The designer may take advantage of this feature in order to operate the device at frequencies in excess of 500kHz.

Figure 13 illustrates this with a circuit offering 2MHz full scale. In this circuit the AD654 is operated at a full scale (FS) of 1mA, with a C_T of 100pF. This achieves a basic device FS frequency of 1MHz across C_T. The P channel JFETs, Q1 and Q2, buffer the differential timing capacitor waveforms to a low impedance level where the push-pull signal is then AC coupled to the high speed comparator A2. Hysteresis is used, via R7, for non-ambiguous switching and to eliminate the oscillations which would otherwise occur at low frequencies.

The net result of this is a very high-speed circuit which does not compromise the AD654 dynamic range. This is a result of the FET buffers typically having only a few pA of bias current. The high end dynamic range is limited, however, by parasitic package and layout capacitances in shunt with C_T, as well as those from each node to AC ground. Minimizing the lead length between A2–6/A2–7 and Q1/Q2 in PC layout will help. A ground plane will also help stability. Figure 14 shows the waveforms V1 – V4 found at the respective points shown in Figure 13.

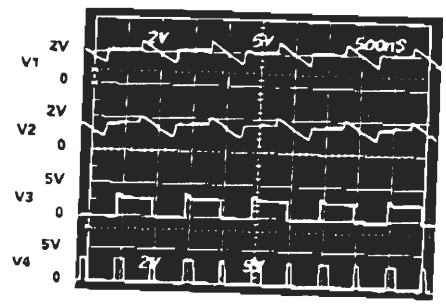


Figure 14. Waveforms of 2MHz Frequency Doubler

The output of the comparator is a complementary square wave at 1MHz FS. Unlike pulse train output V/F converters, each half-cycle of the AD654 output conveys information about the input. Thus it is possible to count edges, rather than full cycles of the output, and double the effective output frequency. The XOR gate following A2 acts as an edge detector producing a short pulse for each input state transition. This effectively doubles the V/F FS frequency to 2MHz. The final result is a 1V full scale input V/F with a 2MHz full-scale output capability; typical nonlinearity is 0.5%.

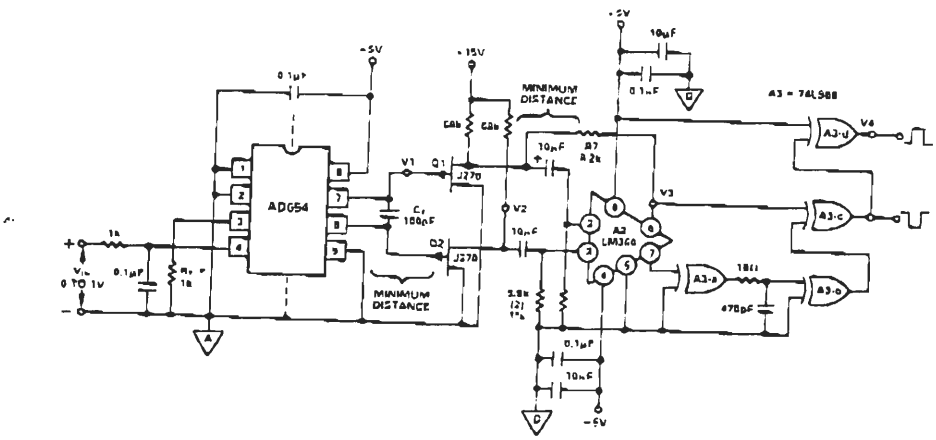


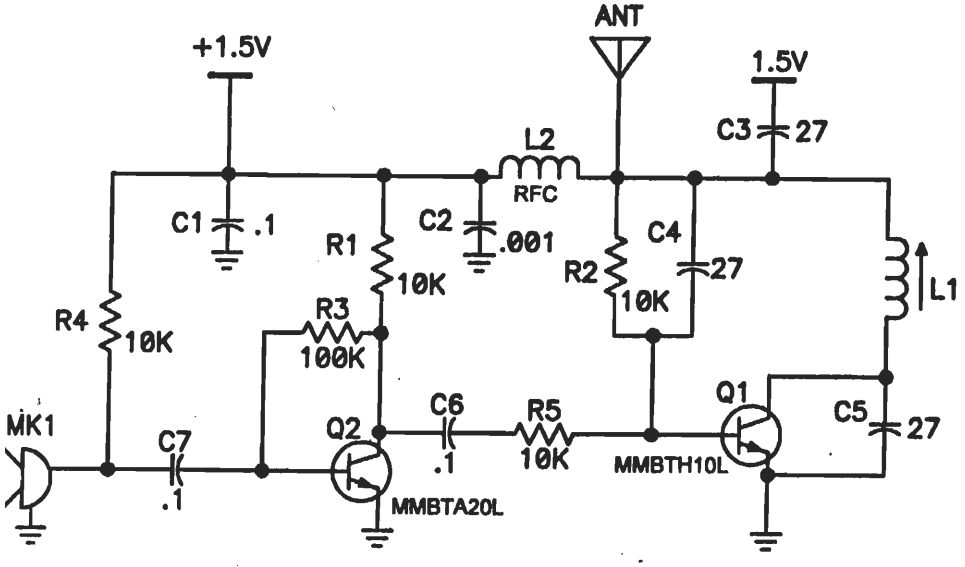
Figure 13. 2MHz, Frequency Doubling V/F

Appendix I – FM-5 FM Transmitter

Manufactured by Ramsey Electronics
793 Canning Parkway
Victor, NY 14564
(716) 924-4560

causing the oscillator frequency to vary accordingly, resulting in elementary frequency modulation, or FM.

FM-5 SCHEMATIC DIAGRAM



RAMSEY Learn-As-You-Build KIT ASSEMBLY

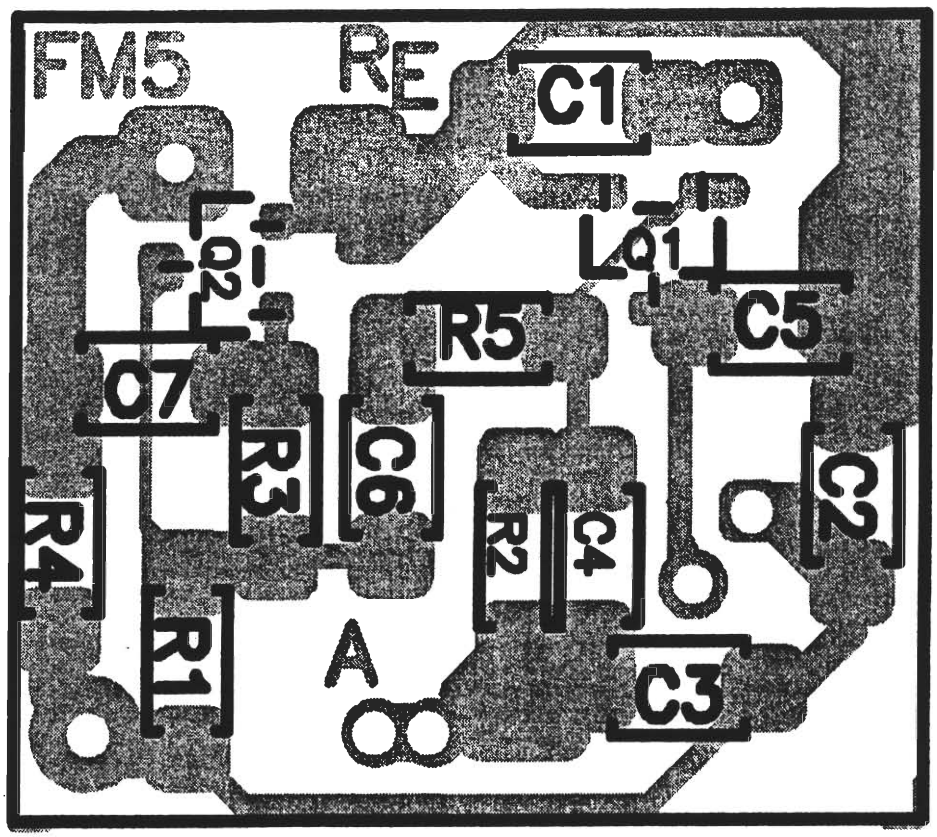
There are numerous solder connections on the FM-5 printed circuit board. Therefore, PLEASE take us seriously when we say that good soldering is essential to the proper operation of your transmitter!

- Use a 25-watt soldering pencil with a clean, sharp tip.
- Use only rosin-core solder intended for electronics use.
- Use bright lighting, a magnifying lamp or bench-style magnifier may be helpful.
- Do your work in stages, taking breaks to check your work. Carefully brush away wire cuttings so they don't lodge between solder connections.

We have a two-fold "strategy" for the order of the following kit assembly steps. First, we install parts in physical relationship to each other, so there's minimal chance of inserting wires into wrong holes. Second, whenever possible, we install in an order that fits our "Learn-As-You Build" Kit building philosophy.
For each part, our word "Install" always means these steps:

FM-5 FINDER DIAGRAM:

Note that all components mount to the "solder" side of the circuit board.



Shown slightly larger than actual size.

Appendix J – LM565 Phase Locked Loop

Manufactured by National Semiconductor
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052
(800) 272-9959

National Semiconductor

February 1995

LM565/LM565C Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CN is specified for operation over the 0°C to +70°C temperature range.

Features

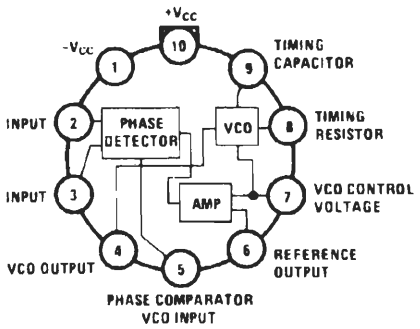
- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%

Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators

Connection Diagrams

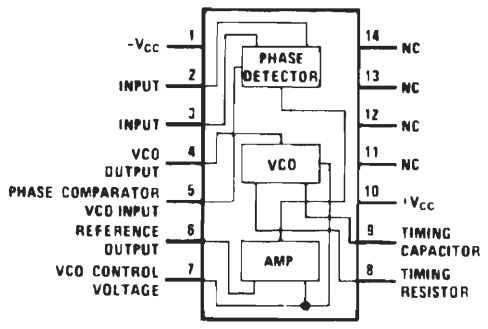
Metal Can Package



TL/H/7853–2

Order Number LM565H
See NS Package Number H10C

Dual-In-Line Package



TL/H/7853–3

Order Number LM565CN
See NS Package Number N14A

 TL/H/7853

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±12V
Power Dissipation (Note 1)	1400 mW
Differential Input Voltage	±1V
Operating Temperature Range	
LM565H	−55°C to +125°C
LM565CN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

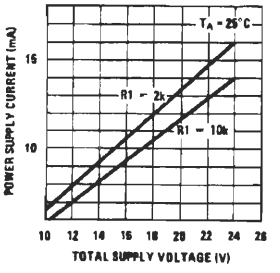
Electrical Characteristics AC Test Circuit, $T_A = 25°C$, $V_{CC} = \pm 6V$

Parameter	Conditions	LM565			LM565C			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	$-4V < V_2, V_3 < 0V$	7	10			5		kΩ
VCO Maximum Operating Frequency	$C_o = 2.7$ pF	300	500		250	500		kHz
VCO Free-Running Frequency	$C_o = 1.5$ nF $R_o = 20$ kΩ $f_o = 10$ kHz	−10	0	+10	−30	0	+30	%
Operating Frequency Temperature Coefficient			−100			−200		ppm/°C
Frequency Drift with Supply Voltage			0.1	1.0		0.2	1.5	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{p-p}
Triangle Wave Output Linearity			0.2			0.5		%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{p-p}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	$f_o = 10$ kHz		6600			6600		Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	400	200	300	450	mV_{p-p}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\lvert V_7 - V_6 \rvert$			30	100		50	200	mV
Temperature Drift of $\lvert V_7 - V_6 \rvert$			500			500		μV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D			.68			.68		V/radian

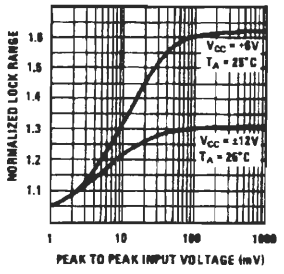
Note 1: The maximum junction temperature of the LM565 and LM565C is +150°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W junction to ambient or +45°C/W junction to case. Thermal resistance of the dual-in-line package is +85°C/W.

Typical Performance Characteristics

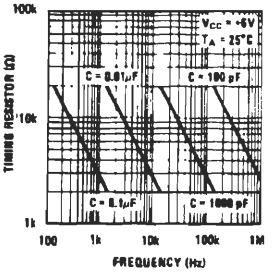
Power Supply Current as a Function of Supply Voltage



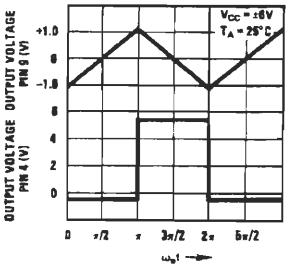
Lock Range as a Function of Input Voltage



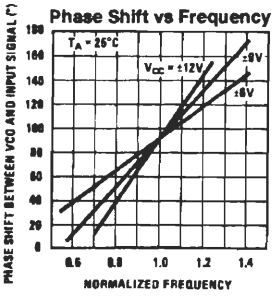
VCO Frequency



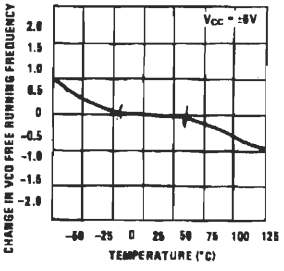
Oscillator Output Waveforms



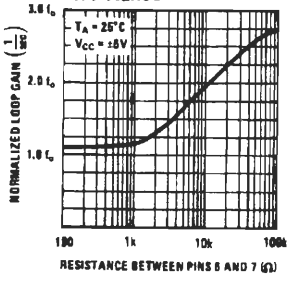
Phase Shift vs Frequency



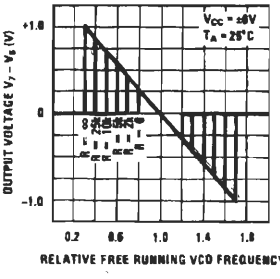
VCO Frequency as a Function of Temperature



Loop Gain vs Load Resistance

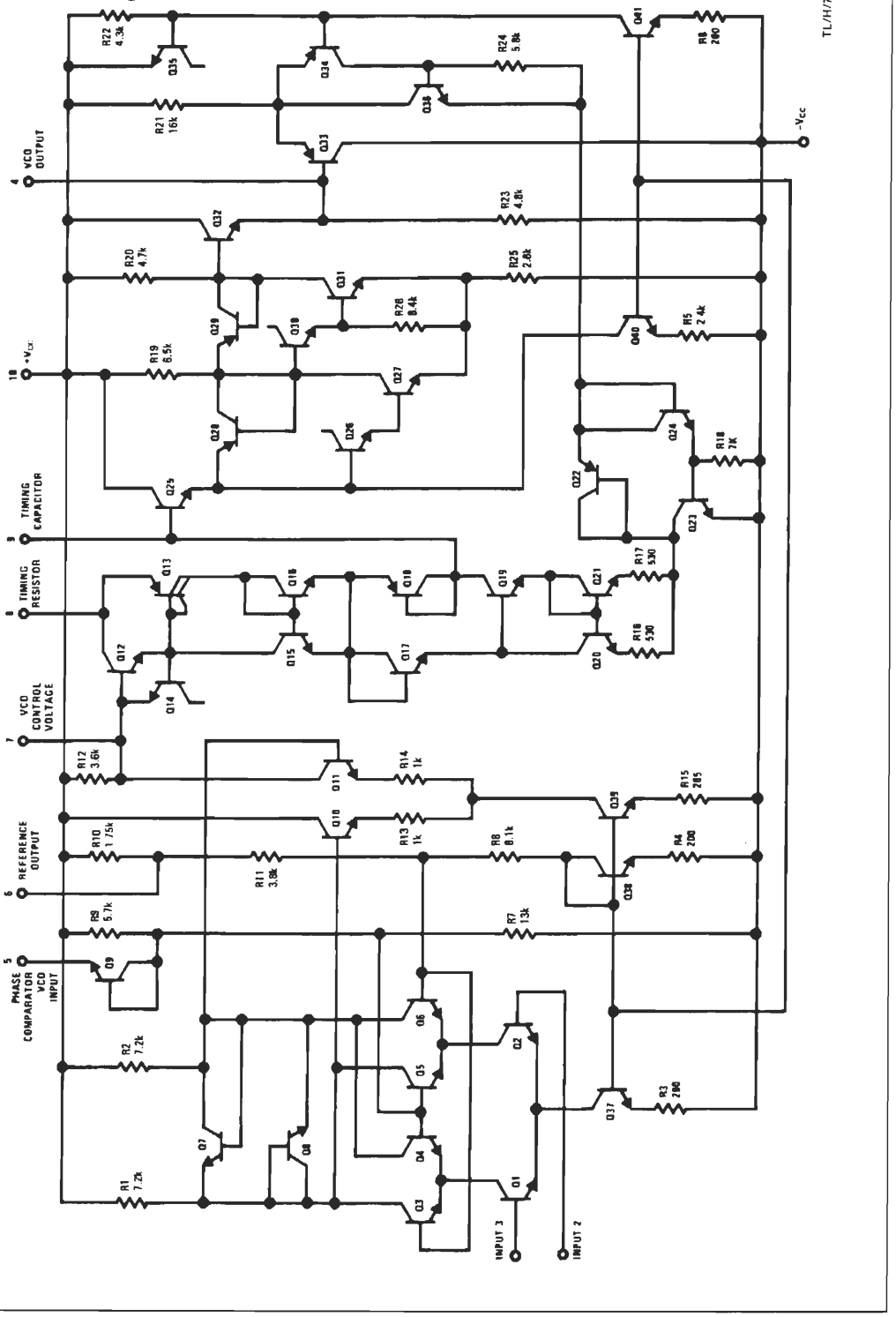


Hold in Range as a Function of R_{6-7}

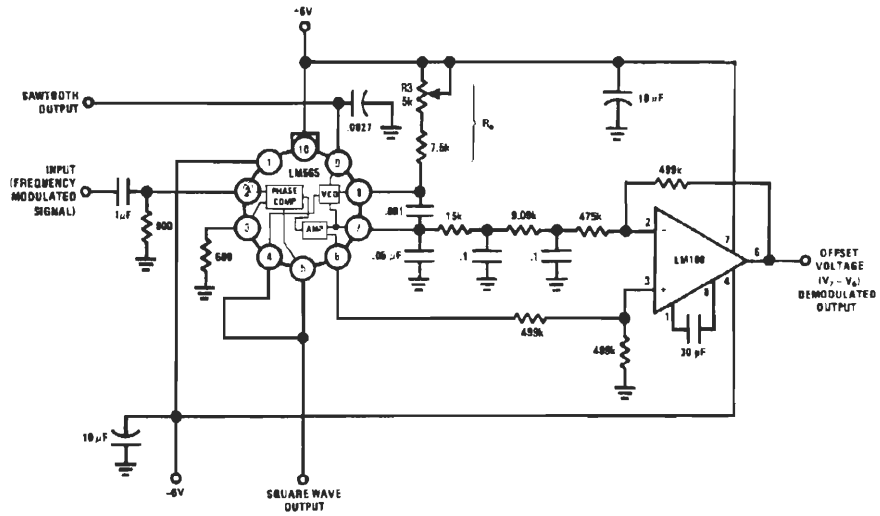


TL/H/7863–4

Schematic Diagram



AC Test Circuit

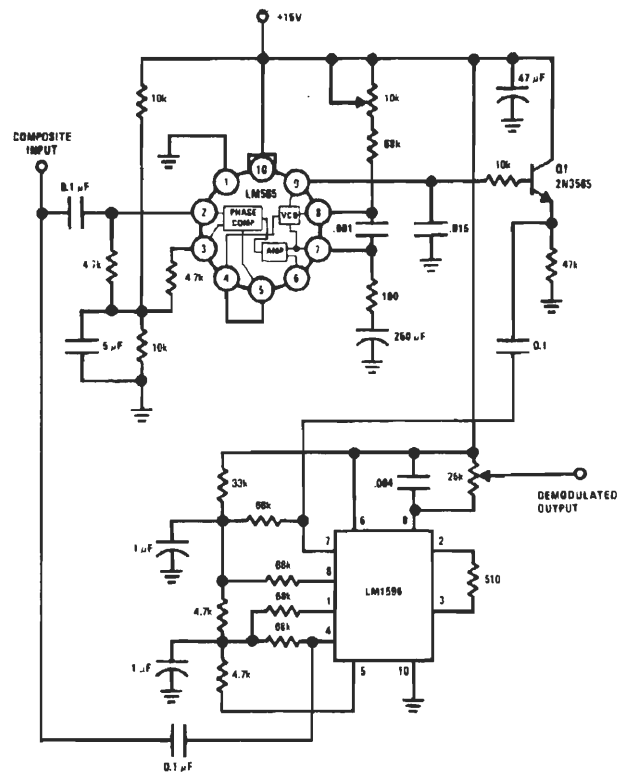


TL/H/7853–5

Note: S_1 open for output offset voltage ($V_7 - V_6$) measurement.

Typical Applications

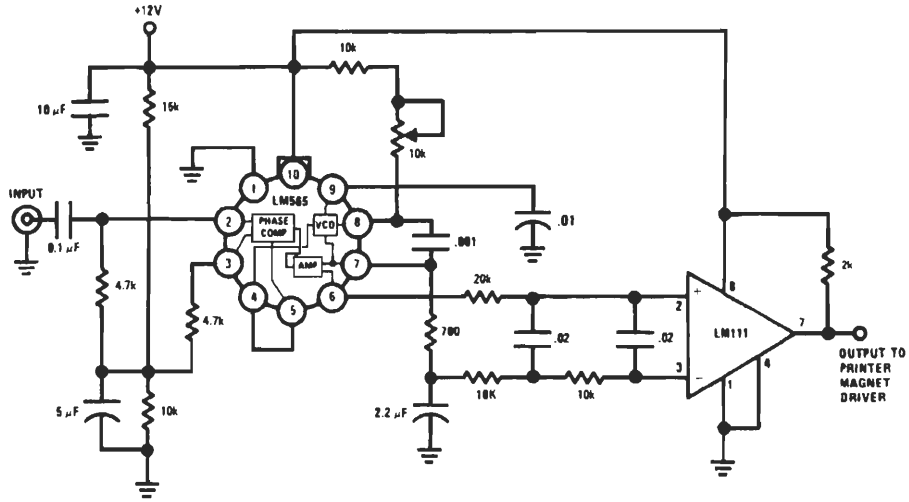
2400 Hz Synchronous AM Demodulator



TL/H/7853–6

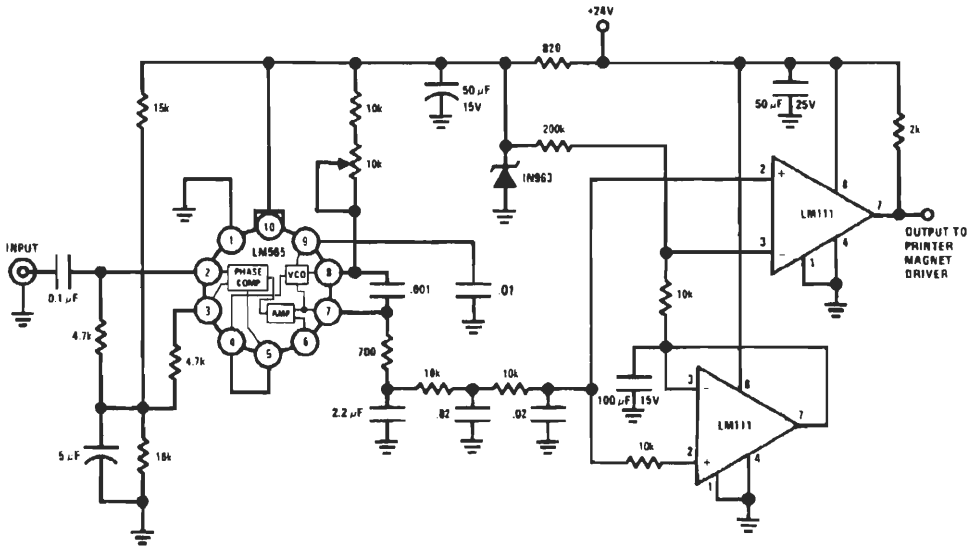
Typical Applications (Continued)

FSK Demodulator (2025–2225 cps)



TL/H/7853–7

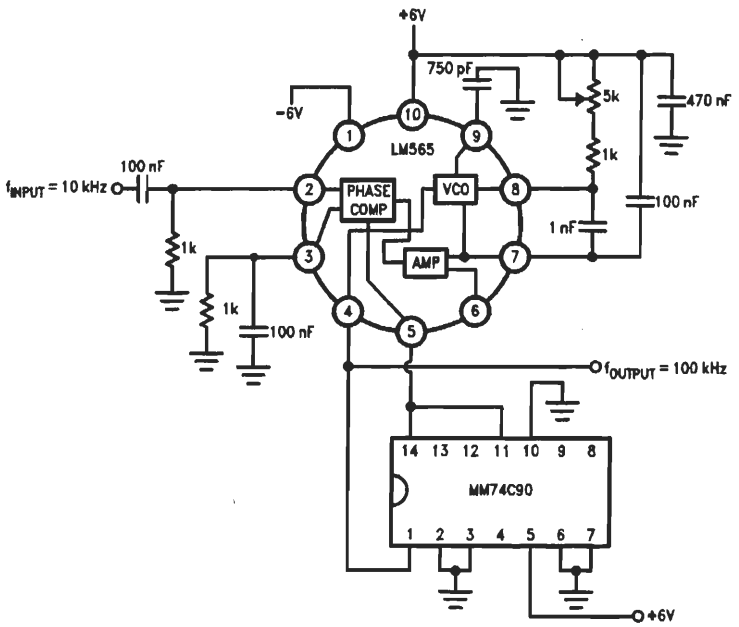
FSK Demodulator with DC Restoration



TL/H/7853–8

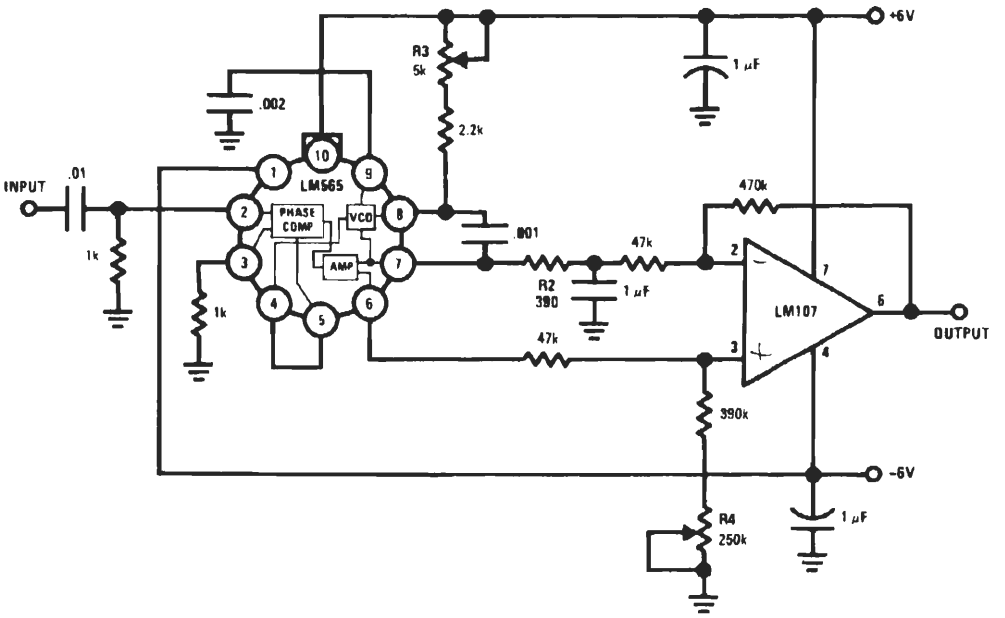
Typical Applications (Continued)

Frequency Multiplier (×10)



TL/H/7853–9

IRIG Channel 13 Demodulator



TL/H/7853–10

Applications Information

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o \cong \frac{0.3}{R_o C_o}$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo theory, this is called the "velocity error coefficient."

$$\text{Loop gain} = K_o K_D \left(\frac{1}{\text{sec}}\right)$$

$$K_o = \text{oscillator sensitivity} \left(\frac{\text{radians/sec}}{\text{volt}}\right)$$

$$K_D = \text{phase detector sensitivity} \left(\frac{\text{volts}}{\text{radian}}\right)$$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6\, f_o}{V_c}$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

$$f_H = \pm \frac{8\, f_o}{V_c}$$

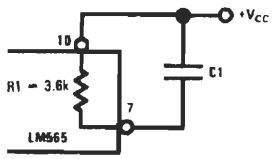
f_o = free running frequency of VCO

V_c = total supply voltage to the circuit

THE LOOP FILTER

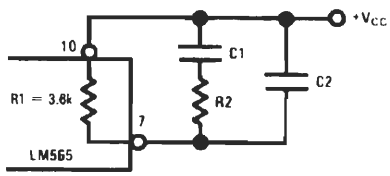
In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7); this filter may take one of two forms:

Simple Lag Filter



TL/H/7853–11

Lag-Lead Filter



TL/H/7853–12

A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi} \sqrt{\frac{K_o K_D}{R_1 C_1}}$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2} \sqrt{\frac{1}{R_1 C_1 K_o K_D}}$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1C_1 < K_o K_D$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

$$f_n = \frac{1}{2\pi} \sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

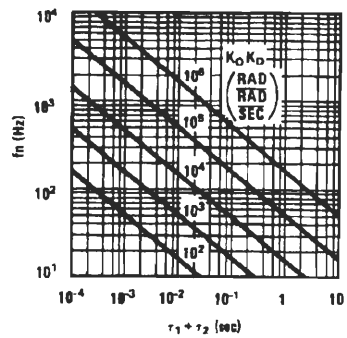
$$\tau_1 + \tau_2 = (R_1 + R_2)\, C_1$$

R_2 is selected to produce a desired damping factor δ, usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta \approx \pi\, \tau_2 f_n$$

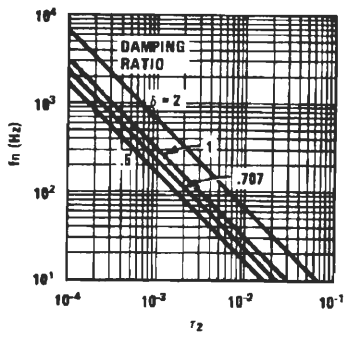
These two equations are plotted for convenience.

Filter Time Constant vs Natural Frequency



TL/H/7853–13

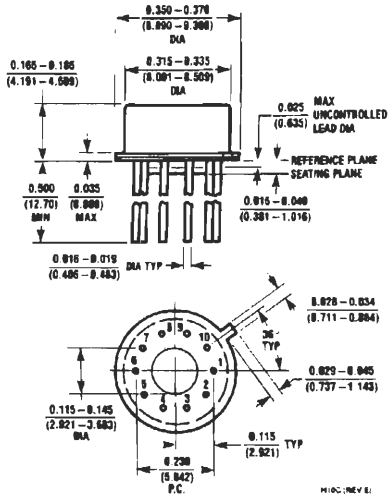
Damping Time Constant vs Natural Frequency



TL/H/7853–14

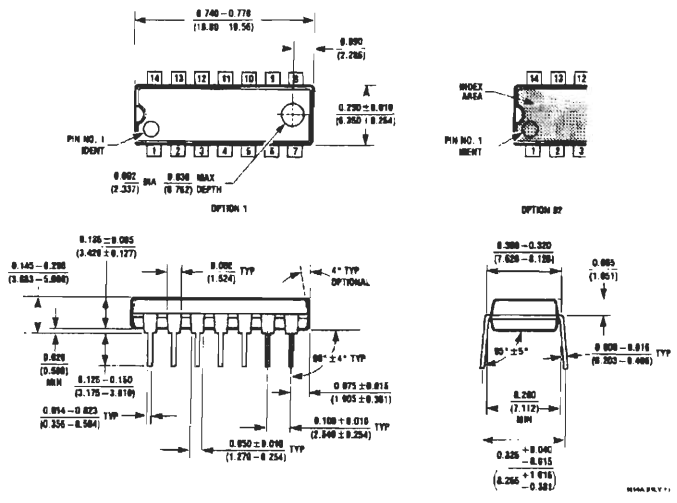
Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of carrier. In general $C_2 \leq 0.1\ C_1$.

Physical Dimensions inches (millimeters)



Metal Can Package (H)
Order Number LM565H
NS Package Number H10C

Physical Dimensions inches (millimeters) (Continued)



Dual-In-Line Package (N)
Order Number LM565CN
NS Package Number N14A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408