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Computer Aided Design for FET Circuits

Iyad Ahmad Natour

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COMPUTER AIDED DESIGN FOR FET CIRCUITS

by

Iyad Ahmad Natour

A Thesis
Submitted to the
Faculty of the Graduate College
in partial fulfillment
of the
Degree of Master of Arts
Department of Physics

Western Michigan University
Kalamazoo, Michigan
August, 1980

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COMPUTER-AIDED DESIGN FOR FET CIRCUITS.
WESTERN MICHIGAN UNIVERSITY, M.I., 1980
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MOS FIELD EFFECT TRANSISTOR

Metal oxide semiconductor field effect transistors (MOSFET) are semiconductor devices in which the conductivity of the channel is controlled by an external electric field. These devices gain their importance because of their higher operating speed, much lower power dissipation, and greatly increased packing density. These properties make them much used in logic gates and memories in computer technology.

Metal Oxide Semiconductors (MOS).

A basic background in order to understand the operation of a MOSFET is to understand the MOS structure and its operation.

Fig. 1.1 The MOS Structure
Figure 1.1 shows the structure of a MOS which consists of a lightly doped silicon P-type (or N-type) semiconductor. This layer is called the substrate, above it is an insulator layer, silicon dioxide, SiO\textsubscript{2}. The insulator thickness ranges between 200Å-1100Å. This insulator is connected with a metallic plate called the gate. In the following discussion, the applied gate voltage V\textsubscript{G} is with respect to the substrate, which is grounded. If V\textsubscript{G} is negative then the majority holes will be attracted to the surface of the semiconductor (i.e., the surface near the insulator) to terminate the electric field produced. This will form a charge layer called the accumulation charge layer. If the magnitude of V\textsubscript{G} is reduced this will reduce the concentration of the holes at the surface. Continuing this process will lead to a point where the concentration of the holes at the surface is zero and we are left with the non-mobile charge of the ionized acceptor. This process forms another kind of charge layer called the depletion charge layer.

Let us now consider the case for a positive gate voltage. Applying such a voltage to the gate will attract the minority electrons to the surface. For a sufficiently high positive gate voltage electrons will become majority carriers at the surface, forming an inversion charge layer.
The above discussion was for a P-type semiconductor MOS structure. The same argument can be made for the N-type semiconductor MOS structure, but the polarity of gate voltage must be inverted.

**MOSFET Structure.**

![Fig. 1.2 A Cross Section of N-channel MOSFET](image)

There are two kinds of MOSFETs, the first is an N-channel MOSFET which operates by means of electron conduction, and the second is P-channel MOSFET which operate by means of hole conduction. In this project the discussion will be based on an N-channel type MOSFET. The same discussion can be extended to the P-channel type by analogy.

Figure 1.2 shows a cross section of an N-channel type MOSFET. It consists of two regions on N-type semiconductor, heavily doped (denoted by $N^+$). These two regions are formed on a substrate, which is lightly doped P-type silicon.
semiconductor. The distance between the two heavily
doped regions is typically a few 10 μm. An insulator
layer of silicon dioxide is formed above the region
separating the two heavily doped regions. A metal contact
with that insulator layer, as shown in Figure 1.2, forms
what is called the gate. There are two metallic contacts
with the two heavily doped regions. The two regions are
called the source and the drain. Because of the symmetry
between these two regions there are no physical differences
between them. A convention is to call the N+ region with
the most negative potential the source, and the other
N-type region the drain.

There are two types of operation of a MOSFET. The
first type is called the enhancement type, in which there
will be no current flow from drain to source when a posi-
tive drain-source voltage is applied and the gate-source
voltage is set to zero, because the drain junction is
reverse biased. On the other hand if a sufficiently
positive gate-source voltage is applied, an inversion
charge layer will be formed in the region between source
and drain. This charge region is called the channel.
When this channel is formed a current will flow from drain
to source, when a positive drain-source voltage is applied.
The minimum gate-source voltage required to produce such
a channel is normally called the threshold voltage.
The second type of MOSFET is the depletion type. These devices can conduct current even if the gate to source voltage is zero. Because there is an inversion layer with gate voltage zero. Conduction can be stopped by applying a negative gate-source voltage. In these devices threshold voltage is a negative voltage. Normally, and in this project, the source and the substrate are grounded. Any gate or drain voltage will be applied with respect to ground.

**The \( V_d-I_d \) Characteristic of a MOSFET [2,7].**

This section summarizes the classical drain current (\( I_d \), current flowing from drain to source) characteristic and shows its dependence on the physical measurements of the MOSFET. The next chapter contains a discussion of some of the new approaches, with emphasis on a recent model which explains the behavior of the device over a wide range of dynamical operating conditions. Generally there are four charge components affecting the behavior of a MOSFET. As shown in Figure 1.3, these charges are

- \( Q_N \): is the total inversion charge layer (mobile),
- \( Q_B \): the total depletion charge layer (non-mobile),
- \( Q_G \): the total gate charge layer (non-mobile),
- \( Q_S \): the total equivalent charge layer.
Fig. 1.3 Charge Distribution of MOSFET

For charge neutrality one should have

\[ Q_N + Q_B + Q_G + Q_S. \]  \hspace{1cm} (1.1)

In deriving the classical characteristic of the drain current the following assumptions are normally made:

1) non degenerate condition,
2) the mobility of the carriers is independent of the field,
3) the substrate is thick and uniformly doped,
4) the diffusion current in the channel is negligible compared to the drift current,
5) electron-hole recombination is negligible,
6) also the electric field \( E_x \) (in the charge layer) is much larger than \( E_y \), this assumption is called the gradual channel approximation. The Poisson equation inside the channel is
\[ \frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho}{\varepsilon_s} \]  

(1.2)

where \( \phi \) is the potential inside the channel. It is assumed to be zero deep in the semiconductor and it is a function of \( x \).

\( -\varepsilon_s \) is the dielectric constant in the semiconductor.

\( \rho \) is the charge density.

\[ \rho = q[(p-n)-(p_0-n_0)] \]  

(1.3)

\( p_0 \) and \( n_0 \) are the equilibrium concentrations of the holes and electrons while \( p \) and \( n \) are hole and electron concentrations respectively. For a P-type semiconductor it is known that

\[ p_0 = n_i e^{\beta \phi_F} \]

\[ n_0 = n_i e^{-\beta \phi_F} \]

where \( n_i = 1.5 \times 10^{16}/m^3 \). The intrinsic density of the silicon. \( \phi_F \) is the fermi potential. Defined to be \( \phi_F = \frac{kT}{q} n(N_A/n_i) \). Also

\[ n = n_i e^{-\beta(\phi_p-\phi)} \text{ and } p = n_i e^\beta(\phi_p-\phi) \]  

(1.4)

where \( \beta \) is \( q/kT \) and where \( \phi_p \) and \( \phi_n \) are the quasi-fermi potential for electrons and holes respectively. \( \phi \) is the potential function. Deep in the semiconductor \( \phi = 0 \) and \( \rho = 0 \).
The solution to equation 1.2 is given in many textbooks and research papers. The results stated below are under the following assumptions: 1) before a strong inversion occurs \( Q_n = 0 \) (the charge density/unit area of the inversion charge layer), which means that the charge at the surface is due to the depletion charge layer only. 2) a strong inversion occurs when \( \phi_s = 2\phi_F \), where \( \phi_s = \phi(x=0) \). At this potential the depletion layer reaches its maximum. It was found that just when the strong inversion occurs

\[
Q_b = -\sqrt{2\varepsilon N_A q \varepsilon_s (V+2\phi_F)}
\]  

(1.5)

where \( N_A \) is the impurity concentration in the semiconductor, and \( V(Y) \) is the potential function along the channel such that \( V(Y=0) = C \) and \( V(Y=L) = V \).

\[
X_d = \left( \frac{2\varepsilon_s (V+2\phi)}{\varepsilon N_A q^2} \right)^{1/2}
\]

(1.6)

\( X_d \) is the effective depletion layer width. Recall equation 1.1 and rewrite it in terms of charge density

\[
Q_n + Q_b + Q_s + Q_g = 0
\]

or

\[
Q_n = -Q_s - Q_b - Q_g
\]

(1.7)

*Capital letter subscript denote total charge while lower case letters denote charge denisty.*
Now

$$Q_g = C_i (V_g - \phi_s - \phi_{ms}) \phi$$  \hspace{1cm} (1.8)

$$C_i = \frac{\varepsilon_i}{t_i}$$  where \(\varepsilon_i\) is the insulator dielectric constant, \(t_i\) is the insulator thickness and \(\phi_{ms}\) is the metal-semiconductor potential work function. Combining equation 1.5, equation 1.7 and equation 1.8 will give us \(Q_n\) at a strong inversion

$$Q_n = -Q_s + \sqrt{2N_A e \varepsilon_s (V+2\phi_f)} - C_i [V_G - V - 2\phi_f - \phi_{ms}]$$  \hspace{1cm} (1.9)

\(I'_D = z \int_0^{x_i} J(x,y) dx\). \(I'_D\) is the current flowing in the \(dy\) direction. \(z\) is the width of the device and \(x_i\) is the channel depth, i.e., \(\phi(x>x_i) = 0\). The current density \(J(x,y) = -q\mu_n \frac{dv(y)}{dy}\) where \(n\) and \(\mu_n\) are the electron density and mobility respectively

$$I'_D = - \frac{dv}{dy} \int_0^{x_i} q \mu_n (x) n(x) dx$$  \hspace{1cm} (1.10)

and define \(\mu_{eff}\) by \(\mu_{eff} = \frac{q \int_0^{x_i} \mu_n (x) n(x) dx}{|Q_n|}\) then equation 1.10 becomes

$$I'_D = -\mu_{eff} z Q_n(y) \frac{dv(y)}{dy}.$$  \hspace{1cm} (1.11)
Q_n is given in equation 1.9 and if equation 1.11 is integrated along the channel from Y = 0 where V(Y=0) = 0 to Y = L where V(Y=L) = V.

Integrating, one gets for drain current:

\[
I'_D = \frac{C_i v_{\text{eff}}}{L} \left[ V_D (V_G - V_T) - \frac{V'_D}{2} - \frac{2}{3} \left( \frac{N A q e_s}{C_i} \right)^{1/2} \right] 
\]

(1.12)

where \( V_T = 2 \phi_F + \phi_{ms} - \frac{Q_s}{C_i} \). Equation 1.12 predicts that for a given gate voltage \( V_G \) the drain current will first increase linearly with drain voltage. This region is called the non-saturated region. Then gradually the current will level off and is approaching a saturated value, this region is called the saturation region.

Figure 1.4 shows an ideal characteristic for a MOSFET. Before going into the details of these two regions, it is worthwhile to find a mathematical form for the threshold voltage. The threshold voltage was previously defined to be the minimum gate voltage needed to make the channel conduct. When \( V_D \) is small but finite, equate \( I_D \) to zero in equation 1.12 and solve for \( V_G \).
then

\[ V_T = V_T^* + 2 \left( \frac{N_A \varepsilon_s \phi_F}{C_i} \right)^{1/2} \]  \hspace{1cm} (1.13)

Now we return to the two regions mentioned above. Let us first consider the non-saturated region. This region can be approximated as

\[ I_D = \frac{C_i u_{eff}^Z}{L} \left[ V_D (V_G - V'_T) - \frac{V_D^2}{2} \right]. \]  \hspace{1cm} (1.14)

This expression is obtained from equation 1.12, for small \( V_D \) and by assuming that \( N_A \), the impurity concentration, is small. Equation 1.14 describes the non-saturation region. Equation 1.12, the drain current equation, is restricted to a range of \( V_D \) such that \( Q_m \) is always a finite negative quantity. As \( V_D \) increased there comes a point at which \( Q_n \) at the drain becomes zero. In reality \( Q_n \) will never be zero, but it will become very small but finite. This phenomena is called the pinch-off, after which the drain current becomes constant as a function of \( V_D \), as shown in Figure 1.4. The pinch-off voltage, \( V'_D \), is defined to be the drain voltage required to produce a pinch-off. \( V'_D \) can be found by finding a value of \( V_D \) which makes \( I_D \) maximum in equation 1.12. Following this approach one can get

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Fig. 1.4 The Ideal Characteristic of MOSFET
where \( V'_{DS} \) is the drain voltage at which saturation occurs. For a lightly substrate doping and thin insulator thickness \( \frac{N_A q_s}{C_i} \ll 1 \), we can approximate the saturation drain voltage as

\[
V_{DS} \approx V_G - V'_T
\]  

(1.16)

and under the same conditions the saturation current can be written with the aid of equation 1.12 and equation 1.15 as

\[
I_{DS} = \frac{C_i \text{eff} V_{G} - V'_T}{2L} \cdot (V_{G} - V'_T)^2.
\]  

(1.17)

Equations 1.14 and 1.17 are the classical drain current equations. Note that equation 1.14 can be applied if \( V_D < V_{DS} = V_G - V'_T \) and equation 1.17 can be applied if \( V_D \geq V_{DS} \).

**Circuit Representations of MOSFET [2]**

For the sake of circuit analysis, a MOSFET can be represented by primitive electrical components, i.e., resistance, capacitance and current sources. The representation can be done for two modes of operation, low frequency and high frequency. In the low frequency mode the MOSFET can be represented as shown in Figure 1.15.
where $g_m$, is the transconductance between input voltage and output voltage, and defined as

$$g_m = \frac{\partial I_D}{\partial V_G} \bigg|_{V_D = \text{cons.}}$$  \hfill (1.18)

and $r_d$ is the drain resistance, defined as

$$\frac{1}{r_d} = g_d = \frac{\partial I_D}{\partial V_D} \bigg|_{V_G = \text{cons.}}$$  \hfill (1.19)

It should be noted that there is a resistor between the gate and the source, which is not shown in the figure. This resistor has such a high value that for practical purposes it is considered to be open.

At a high frequency the capacitive effect should be taken into account. A high frequency representation
of a MOSFET is shown in Figure 1.6. $g_d$ and $g_m$ are the same as defined above. $C_{gd}$ is the gate to drain capacitance given by

$$C_{gd} = \frac{2}{3} C_i \left[ 1 - \frac{V_1^2}{(V_1 + V_2)^2} \right]$$

(1.20)

where $V_1 = V_G - V_T$, $V_T$ was defined in equation 1.13, and $V_2 = (V_G - V_D) - V_T (\frac{1}{C_i} (2q\epsilon_s N_A)(2\phi_f))^{1/2}$ where $V_T$ is as defined before, $V_T' = 2\phi_f + \phi_{ms} - \frac{Q_s}{C_i}$, $C_{gt} = C_{gs} + C_{gb}$ where $C_{gs}$ is the gate to source capacitance and given by

$$C_{gs} = \frac{2}{3} C_i \left[ 1 - \frac{V_2^2}{(V_1 + V_2)^2} \right], \quad V_1 \text{ and } V_2 \text{ defined above},$$

and $C_{gb} = C_i \left[ 1 + \frac{K}{(V_G - V_{FB})} \right]^{1/2}$ where $K = \frac{1}{C_i} (2q\epsilon_s N_A)^{1/2}$.

$V_{FB}$ is the flat band voltage defined by $V_{FB} = \phi_{ms} - \frac{Q_s}{C_i}$.
In this chapter we will present two more models, which try to describe the behavior of a MOSFET. Emphasis will be on the model proposed by El-Mansy, which will be the basic element of the project. The reasons for such a choice are: this new model shows that it is as applicable over a wide range of dynamical operating conditions. This model also predicts the behavior of the device which is very close with experiment, as shown in reference [3]. This model has a very easy expression to be implemented into a computer program.

1) The Charge Sheet Model [J.R. Brews][1]

This model in its final form was developed by J.R. Brews. The idea of this model is to compress the inversion charge layer into a conducting plane of zero thickness. This model was compared with the Pao-Sah model for long channel devices and there was close agreement. This model was found to have the following advantages over the Pao-Sah model: a) a single formula for the current, transconductance, and channel conductance, b) this model includes the diffusion current which is needed to give the correct current near the threshold, c) the possibility of extending the current model into two or three dimensions, which is required when dealing with small devices.

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Since this model uses a charge sheet of zero thickness this implies that i) the current is constrained to move along the oxide-silicon interface and ii) there is no voltage drop across the inversion layer.

The I-V characteristic presented in the paper mentioned is for a long channel device which means that Poisson's equation is one dimensional only because the potential variation along the channel is gradual compared to that normal to the channel. An equation for the current from the source to a point Y in the channel was found to be

\[ I = \frac{1}{\beta} \mu \left[ \frac{Z}{Y} \right] \left[ C_i (1 + \beta V_G) (\phi_s - \phi_{SO}) - \beta/2 C_i (\phi_s^2 - \phi_{SO}^2) \right] - \frac{qN_A \alpha [(\beta \phi_s - 1)^{3/2} - (\beta \phi_{SO} - 1)^{3/2} + qN_A \alpha [(\beta \phi_s - 1)^{1/2} - (\beta \phi_{SO} - 1)^{1/2}]} \]

where \( \alpha \) is the Debye length defined earlier, and \( C_i \) is the insulator capacitance, \( \phi_{SO} = \phi_s (Y=0) \) is the surface potential at the source, and \( \phi_s \) is the surface potential at \( Y \).

To be able to use the above equation one has to find the value of \( \phi_{SO} \) and \( \phi_{SL} = \phi_s (Y=L) \), the surface potential at the drain. Frequently \( \phi_{SO} \) is approximated by \( 2\phi_F \). Although such an approximation gives acceptable results as shown in many texts and research papers [5,7], the present model gave an algorithm to calculate \( \phi_{SO} \).
Once $\phi_{SO}$ is found then $\phi_{SL}$ can be expressed as:

$$\phi_{SL} = \phi_{SO} + V_D.$$ 

2) El-Mansy Model [2,3]

This model was chosen for the following reasons.
1) Most of the previous models were based on the Stronge inversion approximation, which considers the charge in the channel to be of zero thickness and therefore it will not contribute to the surface potential. 2) The old models failed to predict the behavior of a MOSFET at higher currents, that is, the present model provides analytical expressions for the current and the other parameters over a wide range of dynamical operation, which makes this model suitable for computer aided design (CAD).

This new model is based on the following assumptions:

i) The space charge layer of the mobile carriers and the substrate depletion charge can be modeled by a single charge layer, which is uniform normal to the surface.
ii) The mobile part of this layer is transported by drift and diffusion.

Figure 2.1 shows a cross section of a typical MOSFET, with potential applied at its terminals, $U_S$ (source potential), $U_D$ (drain potential), $U_G$ (gate potential), and $U_B$ (substrate potential), all the potentials are normalized.
by $q/kT$ (i.e., $U = \frac{q}{kT} \cdot V$). Note that in the coming discussion there is a potential applied at the source and the substrate. It should be noted also that the capital letter subscript will be used in connection with the external potential, while the lower case subscript will be used with internal analysis of the device. $\phi_S$ in the figure denotes the surface potential of the channel. $Q_n$ denotes the charge density/unit area of the mobile charge of the inversion charge layer, while $Q_d$ denotes the non-mobile charge density of the depletion layer. $\phi_S$ is normalized by $\frac{q}{kT}$.

The analysis is based on defining a quantity which is called a measure of the channel strength $M$, which shows the relation between potential and charge density in the
channel. \( M \) is defined as

\[
M = \int_0^{\phi_s} \text{ndu} = \int_{\text{channel}} \text{ndu}
\]  

(2.1)

\( n \) is the carrier concentration and it is defined by any point \( x \) and \( y \).

An expression for \( M \) was found by solving Poisson's equation inside the channel

\[
M = \int_{U_b}^{\phi_s} \text{ndu} = \frac{Q_s^2}{2q\epsilon_s} \cdot \frac{q}{kT} - N_A (\phi_s - U_b)
\]  

(2.2)

where

\[
Q_s = -(Q_d + Q_n) = \frac{-kT}{q} (U - \phi_s) C_i
\]  

(2.3)

At the source or drain boundary it is required to satisfy relationship 2.2 together with the Boltzman relationship between electron density on either side of the P-N junction. It is required as a boundary condition that \( M \) must have the same value for the channel distribution of \( N \) deduced from the junction Boltzman relation. Let \( U \) be quasi-fermi potential at the \( n^+ \) region (either the source or the drain), the concentration of the electrons is then given by

\[
n = n_0 e^{(U-U_0)}.
\]
$n_0$ is the equilibrium concentration of electron. It is known that $n_0^2 = n_i^2$ and $P_0 = N_A$ for N-type semiconductors

$$n = \frac{n_i^2}{N_A} e^{(U-U_0)}$$

$$M = \int_{U_b}^{\phi_s} n_i^2 \frac{e^{(U-U_0)}}{N_A} du = \frac{n_i^2}{N_A} e^{(\phi_s'-\phi)}$$

(2.4)

Applying the boundary conditions mentioned above, that are required to have equal $M$ in both sides of the $n^+$-region, gives

$$\frac{n_i^2}{N_A} e^{(\phi_s'-\phi_0)} = \frac{[kT(U_g' - \phi_s')C_i]}{2kT\varepsilon_S} - N_A(\phi_s'-U_b).$$

(2.5)

This equation can be simplified by defining the following:

$$a = \left[ \frac{kT}{2n_i q^2} \right]^{1/2} \frac{C_i}{\varepsilon_S} e^{-U_F/2}.$$

$U_F$ is the fermi-potential normalized by $\frac{q}{kT}$ and it is given by $U_F = \ln \frac{N_A}{n_i}$.

Define also $\zeta = a(U_g' - \phi_s')$ and let $\xi = U_0$. Then equation 2.5 takes this form
A numerical solution for this equation is required for \( \zeta \) at the source and drain boundaries with \( \xi \) equal to the source and drain potential respectively. This was done by a computer program, listed in the appendix.

An expression for \( Q_n \) was found by subtracting \( Q_d \) from \( Q_s \)

\[
Q_n = \frac{kT}{q} \frac{C_i}{a} \cdot \frac{\zeta^2 + \xi/a - U_g + U_b}{\zeta} \quad (2.7)
\]

from which an expression for the drain current can be evaluated

\[
I = \mu_{\text{eff}} \frac{L}{W} C_i \left( \frac{kT}{a} \right) \zeta_s \cdot \left[ \frac{\zeta^2}{\zeta} + \left( 2a + \frac{1}{a} \right) \zeta + \left( 1 - U_g + U_b \right) \ln \zeta \right] \zeta_D \quad (2.8)
\]

where \( \zeta_s \) and \( \zeta_D \) are the solution of equation 2.6 at the source and the drain respectively. This expression for the current is valid over a wide range of dynamical operation.

**MOSFET Parameters**

This model also provides an equivalent circuit like the one discussed in the first chapter. The parameters are the same as for the model discussed earlier.
The conductance of the channel is defined and given by:

\[
g_m = \frac{kT}{q} \frac{\partial I_D}{\partial U_G} \bigg|_{U_D, U_S, U_B} = \frac{kT}{q} \frac{\mu C_i Z}{L_a} \left[ \zeta + \frac{1-U_g+U_b}{\zeta} - \frac{1}{a} \ln \frac{\zeta_D}{\zeta_s} \right] \tag{2.9}
\]

The transconductance \( g_d \).

\[
g_d = \frac{q}{kT} \frac{\partial I_D}{U_B} \bigg|_{U_g, U_S, U_B} = \frac{kT}{q} \frac{\mu C_i Z}{L_a} \left[ \zeta_D + \frac{1}{a} - \frac{U_g-U_b}{\zeta_D} \right] \tag{2.10}
\]

The other parameters namely the capacitances were found to be:

\[
C_{gs} = ZL C_i \left\{ \frac{\zeta_s^2 + \zeta_s/a - U_g}{(I_D')^2} \right\} I_D' F/\zeta_s \tag{2.11}
\]

\[
C_{gd} = ZL C_i \left\{ \frac{\zeta_s^2 + \zeta_s/a - U_g}{(I_D')^2} \right\} -I_D' F/\zeta_D \tag{2.12}
\]

\[
C_{gb} = ZL C_i \left\{ \frac{I_D' \left[ 1 - \zeta/a \right] \zeta_s - F \left[ 1/\zeta - \ln \zeta/a \right]}{(I_D')^2} \right\} \zeta_s \tag{2.13}
\]

where

\[
I'_b = I_d \left( \frac{kT}{q} \right)^2 \frac{\mu C_i Z}{L_a^2} \tag{2.14}
\]
In the Ph.D. thesis [3] of El-Mansy he made intensive comparisons between his model and experiment, and he proved close agreement.

Here I present a comparison of the drain current based on the El-Mansy model and the drain current on the classical model. Figure 2.2 shows the characteristic of a MOSFET with the following parameters: \( \text{VG} = 10 \text{V}, \; L = 100 \text{M}, \; Z = 97.5 \text{M}, \; T = 1500 \text{A}, \; \text{NI} = 1 \times 10^7, \) and \( J = 340 \times 10^7. \) Figure 2.3 shows the characteristics of a MOSFET for \( \text{VG} = 8 \text{V}, \) the other parameters are the same.
Fig. 2.1 Characteristic of the old model Compared to the new model

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Fig. 2.2 Characteristic of the old model Compared to the new model
Computer aided design (CAD) is becoming an important tool in designing electronic circuits, especially integrated circuits. This importance comes from the fact that the designer can get the characteristic of the device he or she is designing without having it manufactured. This saves time and money.

In order to have an efficient program for CAD, one should have in hand a theory which describes the characteristic of the basic element of the circuit under consideration. A good program for CAD is one which permits the designer to interact directly with the program. In other words, the designer can specify the physical parameters of the basic element of the device, run the program and get the results. The designer can keep doing this process until he or she gets a desired characteristic.

In this project, two CAD programs for an inverter were developed. The first deals with the transfer characteristic of the inverter, while the second deals with the transient response of the device. In both programs the model of FET developed by Al-Mansey is implemented. The reasons for this choice are: this model has a simple analytical expression for the characteristic of a MOSFET, easy to implement in computer programs, and the formulas provided are applicable over a wider range of dynamical
operation, than other models. Finally this model shows close agreement with the experimental characteristic.

**Invertor [5]**

The inverter, or not gate, is a basic circuit in digital electronics. Ideally we could think of the inverter as a circuit with a single input and a single output and performs the operation of logic negation, i.e., output is high if and only if the input is low and vice versa. High and low are relative terms, and it is the duty of the designer to specify voltage ranges for high and low.

![Circuit Diagram of An Invertor](image)

*Fig. 3.1 Circuit Diagram of An Invertor*
The circuit diagram of an inverter is shown in Figure 3.1. As shown in the figure the inverter consists of two MOSFETs, Q₁ and Q₂. The first transistor Q₁ is called the driving transistor and the second transistor, Q₂, is called the load transistor. An ideal inverter should have a transfer characteristic (a relation between the input \( V_i \) and the output \( V_o \)) as shown in Figure 3.2.

![Fig. 3.2 Ideal and Actual Characteristic of An Inverter](image)

Fig. 3.2 Ideal and Actual Characteristic of An Inverter

Any voltage \( V_i < V_{i1} \) is to be considered logic 0 and therefore the output should be logic 1, i.e., \( V_o = V_{o2} \). From the circuit presented in Figure 3.1 one can see the following conditions:

\[
V_{GS2} = V_{DS2} = V_2
\]

and

\[
I_{D1} = I_{D2}.
\]
The input voltage \( V_i \) is, \( V_i = V_{GS1} \) and the output voltage \( V_o = V_{DS1} \). It should be noted also that \( V_o = V_{DS1} = V_{DD} - V_L \).

![Graphs](image)

**Fig. 3.3 Load and Driving Transistor Characteristic**

Figure 3.3(a) shows the characteristic of \( Q_2 \). The dotted line is the graph of \( I_{D2} \) versus \( V_L \). The slope of this graph is the incremental load conductance \( g_L \) of \( Q_2 \). Figure 3.3(b) shows the characteristic of \( Q_1 \), the dotted graph is the plot of \( I_D = I_{D1} \) versus \( V_{DS1} = V_o = V_{DD} - V_L \).

To get the transfer characteristic of the inverter the above conditions should be satisfied. The process of constructing the transfer characteristic is as follows: for an input voltage \( I_i = V_{GS1} \) an output voltage \( V_o = V_{DS1} \) is found by reading the intercept of the load curve with current characteristic as shown in Figure 3.3(b).
Figure 2.3 shows, as mentioned earlier, the ideal transfer characteristic of an inverter. Figure 3.2 also shows the actual transfer characteristic of an inverter. The problem facing the designer when designing such a circuit is to get the actual transfer characteristic as close as possible to the ideal one. The real transfer characteristic depends on the dimensions of the two transistors used, i.e., length, width, the impurity concentration and the insulator thickness. As mentioned earlier there are many models which describe the behavior of MOSFETs. The model used here is the model proposed by El-Mansey [3]. A program was developed to simulate the behavior of an inverter. (A listing of the program is given in the appendix. A sample run of the program is found at the end of this chapter.) This program starts by asking the user to provide length, width mobility and the insulator thickness for both the driving and load transistor. Also the program asks for \( V_{DD} \) (refer to Figure 3.1).

**Transient Response of an Invertor**

In the actual use of an inverter the input is a pulse of duration around 25 n-sec. The output of the inverter should be an inverted pulse. Figure 3.3(a) shows a typical input pulse and Figure 3.3(b) shows the output of the
Fig. 3.4 Time Response of An Inverter

Output Voltage vs. Time

Actual Response

Ideal Response
invertor for such an input. The reason for such an exponential rising is due to the capacitors inside the MOSFET as it was discussed earlier in Chapter 1. Using the high frequency model of MOSFET for the driving transistor and replacing the load transistor by its equivalent resistor, the circuit shown in Figure 3.1 will look like the circuit shown in Figure 3.5.

![Fig. 3.5 Low Frequency Representation of An Invertor](image)

The problem now is to find the output voltage $V_o$ for such $V_i$. The solution of the above problem goes as follows. Calculate the input capacitance which, in electronic books is called the Miller capacitance. Part of the circuit shown in Figure 3.5 can be drawn as shown in Figure 3.6 with current and potential defined as shown in the diagram. Using Kirchhoff's Current Law for node 1
Let \( A_v = \frac{V_o}{V_i} \) (voltage gain). Then equation 3 becomes

\[
I_2 = \frac{(A_v - 1)}{1/C_{gs}S} = (A_v - 1)V_i C_{gd}S
\]
Back to Kirchhoff's Current Law.

\[ I_t = I_1 - I_2 \]

\[ = V_i C_{gs} S - (A_v - 1)V_i C_{gs} S \]

\[ = V_i [C_{gs} + (1-A_v)C_{gd} S] \]

Define \( \frac{I_t}{V_i} = \) input admittance

\[ = C_{gs} S + (1-A_v)C_{gd} S \]

\[ \frac{1}{V_i/V_t} = \frac{1}{Z_i} = \frac{1}{C_{gs} S} + \frac{1}{1/(1-A_v)C_{gd} S} . \]

Drawing the capacitive circuit for the above equation

\[ \begin{array}{c}
\hline
\hline
\end{array}
\]

\[ Z_i \quad C_{gs} \quad (1-A_v)C_{gd} \]

this can be made into

\[ C_{in} = C_{gs} + (1-A_v)C_{gd} \ldots \quad \text{(Miller Capacitance)} \quad \text{(3.5)} \]

\[ A_v = -g_m R_t \quad \text{(3.6)} \]
where

\[ R_t = \frac{R_L r_d}{R_L + r_d} \]

which gives

\[ C_{in} = C_{gs} + (1 + g_m r_t) C_{gd}. \]

The simplified equivalent circuit will now be

\[ V_o = -g_m V_i R_t. \]

Calculation for \( V_i \).

The above figure shows the connection of the inverter to a source, with \( R_s \), the source impedance, while \( E_s \) is the source. We could write \( V_i \) in terms of \( C_{in}, R_s \), and \( E_s \).
\[ V_i = \left( \frac{E_s}{R_s + 1/C_i S} \right) \cdot \frac{1}{C_i S} \]

\[ V_i = \left( \frac{E_s}{1 + C_i R_S S} \right) \]

(3.8)

Using equation 3.7, the output voltage becomes

\[ V_i = -g_m \frac{E_s}{1 + C_i R_S S} \cdot R_L \]

or

\[ \frac{V_O}{E_s} = \frac{-g_m R_L}{1 + C_i R_S S} \cdot \frac{1}{S} \]

(3.9)

In the application of the invertor, the source voltage \( E_s \) is a pulse, which can be written as a difference of two step functions

\[ E_s(t) = a [U(t) - U(T-\delta)] \]

where

\[ a \] : is the amplitude of the pulse

\[ \delta \] : is the duration of the pulse.

The LaPlace transformation of the above source is

\[ E_s(S) = a \left( \frac{1 - e^{-\delta S}}{S} \right) = a \left( \frac{1 - e^{-\delta S}}{S} \right) \]
Modifying equation 3.9 we obtain
\[ V_o(S) = -g_m R_t a \left( \frac{1}{1+R_s C_{in} S} \right) \cdot \frac{1-e^{-\delta S}}{S}. \]

Recall that \( A = -g_m R_t \) and define \( K = R_s C_{in}. \) Then we get
\[ V_o(S) = aA_v \left( \frac{1}{1+KS} \right) \cdot \frac{1-e^{-\delta S}}{S} \]
or
\[ V_o(S) = \frac{aA_v}{(1+KS)S} - \frac{aA_v e^{-\delta S}}{(1+KS)S}. \] (3.10)

Consider the first term of the above equation.
\[ \frac{aA_v}{(1+KS)S} = \frac{\beta_1}{S} - \frac{\beta_2}{1+KS} \]

Solving for \( \beta_1 \) and \( \beta_2 \) one obtains
\[ \frac{aA_v}{(1+KS)S} = \frac{aA_v}{S} - \frac{aA_v k}{1+KS}. \]

Similarly we will obtain terms for the second term of equation 3.10
\[ \frac{aA_v e^{-\delta S}}{(1+KS)S} = aA_v e^{-\delta S} \left( \frac{1}{S} - \frac{1}{1/k+S} \right). \]
Then equation 3.10 becomes

\[ V_o(s) = aA \left[ \frac{1}{s} - \frac{1}{1/k+s} - \frac{e^{-\delta s}}{s} + \frac{e^{-\delta s}}{1/k+s} \right] \]

The inverse Laplace transformation gives us the solution for the output voltage. Taking the inverse we get as an output voltage

\[ V_o(t) = aA \left[ 1 - e^{-t/k} \right] u(t) - aA \left[ 1 - e^{-1/k(t-\delta)} \right] u(t-\delta) \]

(3.11)

It should be noted at this point that equation 3.11 does not give the actual output voltage because in the above analysis we did not consider \( V_{DD} \). Therefore to obtain the actual output voltage we should add \( V_{DD} \) to equation 3.11.

Results

Program 3.1 shows an actual run of the program which simulates the transient response of an inverter. The transfer characteristic simulator has the same dialog. Several runs for the transfer characteristic were done. Figure 3.7 - 3.11 show the results. All runs were done for the following parameters for both load and driving transistor. \( N_A = 1.5E21 \), \( t_i = 1500 \mu m \) and \( u = 370 \times 10^{-21} \). Figure 3.7 shows results for \( L_L = 100 \mu m \), \( Z_L = 100 \mu m \).
EX FET2.F4, CGS.F4, CDG.F4, FM.F4, GD.F4, CURENT.F4, ETA.F4, TRAN.F4
FORTRAN: FET 2
MAIN.
FORTRAN: CGS
CGS
FORTRAN: CGD
CGS
FORTRAN: GM
GM
FORTRAN: GD
GD
FORTRAN: CURENT
CURENT
FORTRAN: ETA
ETA
FORTRAN: TRAN
TRAN
LINK: LOADING
[LNKXCT FET2 EXECUTION]

PARAMETERS OF LOAD TRANSISTOR IN (MKS) UNITS
INPUT LENGTH, WIDTH, MOBILITY IMPURITY CONCENTRATION AND
THE INSULATOR THICKNESS SEPARATED BY SPACES
100E-6  100E-6  370E-4  1.5E21  1500E-10

PARAMETERS OF DRIVING TRANSISTOR
INPUT LENGTH, WIDTH, MOBILITY IMPURITY CONCENTRATION AND
THE INSULATOR THICKNESS SEPARATED BY SPACES
10E-6  100E-6  370E-4  1.5E21  1500E-10

INPUT VDD (VOLT), DURATION OF IMPULSE (SEC), MAGNITUDE OF
IMPULSE (VOLT), AND INPUT INPEDANCE (OHM)
10.0  0.001  9.99  500.0
STOP

END OF EXECUTION
CPU TIME: 2.7  ELAPSED TIME: 2:5.92

Program 3.1
\[ Z_d = 100\mu m, \ L_d = 100\mu m. \] Figure 3.8 shows a result for 
\[ Z_L = 100\mu m, \ L_L = 50\mu m, \ Z_d = 100\mu m, \ L_d = 10\mu m. \] Figure 
3.10 shows a result for 
\[ Z_L = 100\mu m, \ L_L = 100\mu m, \ Z_d = 100\mu m, \ L_d = 10\mu m. \] Figure 
3.11 shows results for 
\[ Z_L = 10\mu m, \ L_L = 100\mu m, \ Z_d = 25\mu m, \ L_d = 10\mu m. \] Figure 
3.11 shows results for 
\[ Z_L = 10\mu m, \ L_L = 100\mu m, \ Z_d = 50\mu m, \ L_d = 10\mu m. \] 

As it can be seen from Figures 3.7 - 3.11 the transfer characteristic becomes closer to the ideal one as the 
\( \frac{Z_d}{L_d} \) increases. Results for the run of the 
transient response are shown in Figures 3.12 - 3.14.

Figure 3.12 shows the transient response of an 
inverter with the following parameters. Driving and load 
transistor both have \( \mu = 370 \times 10^{-21}, \ NA = 7 \times 10^{21}/m^3, \) 
\( t_i = 1100\mu A, \ Z = 97.5\mu m, \ L = 100\mu m. \) The duration of the 
pulse is 0.2 n-sec., while the magnitude of the pulse is 7.0 volts.

Figure 3.13 shows the transient response of an 
inverter with the following parameters. Driving and load 
transistor both have \( \mu = 370 \times 10^{-21}, \ NA = 1 \times 10^{21}/m^3, \) 
\( t_i = 1055 \mu A, \ Z_L = 10\mu m, \ L_L = 100\mu m, \ Z_d = 25\mu m, \) 
\( L_d = 10\mu m. \) 

Figure 3.14 shows results for the run with the 
following parameters for both load and driving transistor. 
\( \mu = 370 \times 10^{-21}, \ NA = 1.5 \times 10^{21}, \ t_i = 1055 \mu A, \)
$Z_L = 100\mu m$, $L_L = 100\mu m$, $Z_d = 100\mu m$, $L_d = 10\mu m$. The duration of the pulse is 0.2 n-sec., while the magnitude is 9.99 volts.
Fig. 3.7 Transfer Characteristic, for $\beta = 1$
Fig. 3.8 Transfer Characteristic, for $\beta = 5$
Fig. 3.9 Transfer Characteristic, for $\beta = 10$
Fig. 3.10 Transfer Characteristic, for \( \beta = 25 \)
Fig. 3.11 Transfer Characteristic, for $\beta = 50$

TIME <FEL.>

OUTPUT VOLTAGE (VOLT)
Fig. 3.12 Transient Response, for $\beta = 10$
Fig. 3.14 Transient Response, for $\beta = 50$
BIBLIOGRAPHY


APPENDIX I

This appendix gives a listing of the two computer programs which calculates the transfer characteristic of an inverter, and the transient response of an inverter.
THIS APPENDIX SHOWS A LIST OF THE PROGRAM WHICH SIMULATES THE TRANSFER CHARACTERISTIC OF AN INVERTOR. DATA NEEDED TO RUN THIS PROGRAM ARE: LENGTH, WIDTH, MOBILITY, IMPURITY CONCENTRATION AND INSULATOR THICKNESS FOR BOTH THE LOAD AND DRIVING TRANSISTOR. ALSO THE USER SHOULD PROVIDE VDD. AFTER A SUCCESSFUL EXECUTION OF THIS PROGRAM, THE RESULT WILL BE FOUND IN A DISK FILE 'FOR20.DAT'.

EXTERNAL SUBROUTINE USED

CURREN A FUNCTION SUBPROGRAM TO CALCULATE THE DRAIN CURRENT.

ETA A FUNCTION SUBPROGRAM TO CALCULATE

REAL K,NI,K1,K2,ID1,ID2
REAL L1,MU1,NA1
REAL L2,MU2,NA2

DATA EPSI,EPSS/3.53677E-11,1.0613295E-10/
DATA K,T,NI,Q,VS/1.38E-23,300.0,1.5E16,1.6E-19,0.0/
CALL ERRSET(0)

WRITE(5,1)
1 FORMAT(IX,'PARAMETERS OF LOAD TRANSISTOR (MKs) UNITS')

WRITE(5,2)
2 FORMAT(IX,'INPUT LENGTH WIDTH MOBILITY IMPURITY CONCENTRATION AND THE THICKNESS OF INSULATOR SEPERATED BY SPACES.')
READ(5,3)L2,Z2,MU2,NA2,TI2

3 FORMAT(5G)

WRITE(5,4)
4 FORMAT(IX,'INPUT PARAMETERS OF DRIVING TRANSISTOR IN MKS')
WRITE(5,2)
READ(5,3)L1,Z1,MU1,NA1,TI1

C=SQR((K*T*EPSS)/(2*NI*Q**2))

A1=C*SQR((NI/NA1)*(EPSI/(TI1*EPSS)))
A2=C*SQR((NI/NA2)*(EPSI/(TI2*EPSS)))
K1=MU1*(Z1/L1)*(EPSI/TI1)*((K*T)/(Q*NA1))**2
K2=MU2*(Z2/L2)*(EPSI/TI2)*((K*T)/(Q*NA2))**2

WRITE(5,5)
5 FORMAT(IX,'INPUT THE VALUE OF VDD')
READ(5,3)VDD

DO 9 II=1,22
VG1=II/2.0-0.5

9 DO 10 J=10,1000
VD1=J/100.0 - 0.01
ID1=CURREN(VG1,VD1,K1,A1,VS1)
VD2=VDD-VD1

DO 10 J=10,1000
VD1=J/100.0 - 0.01
ID1=CURREN(VG1,VD1,K1,A1,VS1)
VD2=VDD-VD1

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VS2=VD1
ID2=CURENT(VG2,VD2,K2,A2,VG2)
IF(ID1 .EQ. 0.0 .AND. ID2 .EQ. 0.0) GO TO 13
IF(ID1 .EQ. 0.0) GO TO 10
IF(ABS((ID1-ID2)/ID1) .LT. 1E-1) GO TO 13
10 CONTINUE
13 WRITE(20,14) VD1, VG1
14 FORMAT(2G)
9 CONTINUE
STOP
END

EXTERNAL PROGRAMS USED

C
C CURENT A FUNCTION SUBPROGRAM TO CALCULATE THE DRAIN CURENT
C ETA A FUNCTION SUBPROGRAM TO FIND THE SOLUTION OF
C \[ \frac{1}{\eta} \left( u_d - \frac{2a}{\eta} - \frac{1}{2} v_b \right) = \frac{1}{\eta} + \frac{2a}{\eta} + u_d + u_b \]
C CGS A FUNCTION SUBPROGRAM TO CALCULATE \( C_{GS} \)
C CGD A FUNCTION SUBPROGRAM TO CALCULATE \( C_{GD} \)
C GM A FUNCTION SUBPROGRAM TO CALCULATE \( \gamma M \)
C GD A FUNCTION SUBPROGRAM TO CALCULATE \( \alpha D \)
C TRAN A SUBROUTINE TO FIND THE TRANSIENT RESPONSE OF THE INVERTER UNDER CONSIDERATION.

REAL K,N1,K1,K2
REAL L1,MU1,NA1,ID1
REAL L2,MU2,NA2,ID2
COMMON /AREA1/ VG1,UF,UB,VS1
COMMON /AREA2/ K,T,N1,Q,A1
COMMON /AREA3/ MU1,L1,Z1,T1,ID1
DATA EPSI,EPSS/3.53677E-11,1.0613295E-10/
DATA K,T,N1,Q,1.38E-23,300.0,1.5E16,1.6E-19/
DATA VS1,UF,UB,0.0,13.0533,0.0/
WRITE(5,2)
2 FORMAT(IX,'PARAMETERS OF LOAD TRANSISTOR IN (MKS) UNITS')
WRITE(5,3)
3 FORMAT(IX,'INPUT LENGTH, WIDTH, MOBILITY IMPURITY COCENTRATION',1,X,'AND THE INSULATOR THICKNESS SEPERATED BY SPACES')
READ(5,4)L2,Z2,MU2,NA2,T1
WRITE(5,7)
7 FORMAT(IX,'INPUT VDD (VOLT), DURATION OF IMPULSE (SEC), MAGNITUDE 2',1X,'OF IMPULSE (VOLT), AND INPUT IMPEDANCE (OHM)')
READ(5,8)VDD,D,VS1,R
8 FORMAT(4G)
C=SQRT((K*T*EPSS)/(2*NI*Q**2))

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A1=C*SQRT(NI/NA1)*(EPSI/(TI1*EPSS))
A2=C*SQRT(NI/NA2)*(EPSI/(TI2*EPSS))
K1=MU1*(Z1/L1)*(EPSI/TI1)*(K*T)/(Q*A1)**2
K2=MU2*(Z2/L2)*(EPSI/TI2)*(K*T)/(Q*A2)**2

DO 9 I=10,1001
VD1=I/100.0 - 0.01
ID1=CURRENT(VG1,VD1,K1,A1,VS1)
102 VD2=VDD-VD1
VG2=VD2
VS2=VD1
ID2=CURRENT(VG2,VD2,K2,A2,VS2)
101 IF(ID1 .EQ. 0.0 .AND. ID2 .EQ. 0.0) GO TO 13
IF(ID1 .EQ. 0.0) GO TO 9
IF(ABS((ID1-ID2)/ID1) .LT. 0.1) GO TO 13
9 CONTINUE
WRITE(5,11)
11 FORMAT(1X,'ERROR')
STOP
13 CGS1=CGS(VD1)
CGD1=CGD(VD1)
CGM1=((K*T)/Q)*(MU1*EPSI*Z1)/(L1*A1*TI1)
CGM2=((K*T)/Q)*(MU2*EPSI*Z2)/(L2*A2*TI2)
GM1=GM(VD1,VS1,VG1,CGM1,A1)
GM2=GM(VD2,VS2,VG2,CGM2,A2)
GD1=GD(VD1,VS1,VG1,CGM1,A1)

RL=1/GM2
RD=1/GD1
100 CALL TRAN(CGS1,CGD1,RL,RD,GM1,R,VD1,VG1)
STOP
END
A LIST OF CGS FUNCTION SUBPROGRAM, WHICH CALCULATES C_SD OF MOSFET, BASED ON THE FORMULA GIVEN IN THE TEXT.

DIRECT PARAMETERS.

---

**VD** DRainer VOLTAGE

**INDIRECT PARAMETERS**

**VG** GATE VOLTAGE
**UF** FERMI POTENTIAL
**UB** SUBSTRATE POTENTIAL NORMALIZED
**VS** SOURCE VOLTAGE
**K*,T*,Q** BOLTZMAN CONSTANT, TEMPERATURE, AND ELECTRON CHARGE
**MU** MOBILITY OF THE ELECTRONS
**L*,Z** LENGTH AND WIDTH
**TI** THICKNESS OF INSULATOR
**ID** DRAIN CURRENT

FUNCTION CGS(VD)

REAL K, ID, L, MU, IDP

COMMON /AREA1/ VG, UF, UB, VS
COMMON /AREA2/ K, T, Q, A
COMMON /AREA3/ MU, L, Z, TI, ID

COMMON UG, UFF, AA, U, US

FF(ET) = (ET**3) / 3 + (2*A + 1/A) * (ET**2 / 2) + (1 - UG + UB) * ET

UFF = UF
AA = A
B = 38.647343
UG = (VG - 0.5) * B
UD = VD * B
US = VS * B

CI = 3.53677E-11 / TI

IDP = ID / (((K * T / Q)**2) * (MU * CI * Z) / (L * A**2))
ETA = ETA(UD)
ETAS = ETA(US)
F = FF(ETAS) - FF(ETA)

CGS = (Z * L * CI) * (((ETAS**2 + ETAS / A - UG) * (IDP - F / ETAS)) / IDP**2)

RETURN
END
A LIST OF CGD FUNCTION SUBPROGRAM WHICH CALCULATES 
MOSFET, BASED ON THE FORMULA PROVIDED IN THE TEXT.

THE PARAMETERS ARE THE SAME AS THE PARAMETERS OF CGS.

FUNCTION CGD(VD)

REAL K, IDP, L, MU, ID

COMMON /AREA1/ VG, UF, UB, VS
COMMON /AREA2/ K, T, Q, A
COMMON /AREA3/ MU, L, Z, TI, ID
COMMON UG, UFF, AA, U, US

FF(ET) = (ET**3) / 3 + (2*A + 1/A) * (ET**2 / 2) + (1 - UG + UB) * ET

UFF=UF
AA=A
B=38.647343
UD=VD*B
UG=VG*B
US=VS*B
UF=13.0533

Cl=3.53677E-11/TI

IDP=ID / (((K*T/Q)**2) * ((MU*Cl*Z)/(L*A**2)))

ETAD=ETA(UD)
ETAS=ETA(US)

F=FF(ETAS) - FF(ETAD)

CGD=(Z*L*Cl)*((ETAD**2 + ETAD/A - UG)*(-IDP + F/ETAD)) / IDP**2
RETURN
END
THIS SHOWS A LIST OF GM FUNCTION SUBPROGRAM, WHICH CALCULATES \( g_m \) BASED ON THE FORMULA GIVEN IN THE TEXT.

DIRECT PARAMETERS
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\[ \text{FUNCTION } \text{GM}(V_D, V_S, V_G, CGM, A) \]

\[ \text{COMMON } U_G, U_F, A_A, U_B, U_S \]

\[ G(T) = CGM \times (T + (1 - U_G - U_B)/T - (1/A) \times \text{ALOG}(T)) \]

\[ A_A = A \]
\[ B = 38.647343 \]
\[ U_B = V_D \times B \]
\[ U_G = V_G \times B \]
\[ U_S = V_S \times B \]
\[ U_F = 13.0533 \]

\[ \text{ETAS} = \text{ETA}(U_S) \]
\[ \text{ETAD} = \text{ETA}(U_D) \]

\[ \text{GM} = G(\text{ETAS}) - G(\text{ETAD}) \]

RETURN
END
THIS SHOWS A LIST OF GD FUNCTION SUBPROGRAM WHICH CALCULATES $J_d$ BASED ON THE FORMULA GIVEN IN THE TEXT.

DIRECT PARAMETERS

$V_D, V_S, V_G$ DRAIN, SOURCE, GATE VOLTAGES

$CGM$ IS EQUAL TO $\left(\frac{k T}{q}\right) \left(\frac{\mu e s Z}{L^0.t_i}\right)$

INDIRECT PARAMETERS

$U_F$ FERMI POTENTIAL

$A$

FUNCTION GD($V_D$, $V_S$, $V_G$, $CGM$, $A$)

COMMON $U_G$, $U_F$, $A$, $U_B$, $U_S$

$AA = A$
$U_F = 13.0533$
$B = 38.647343$
$UD = V_D*B$
$UG = V_G*B$
$US = V_S*B$

$TD = ETA(U_D)$
$GD = CGM*(TD+1/A-(U_G-U_B)/TD)$
RETURN
END
A LIST OF ETA FUNCTION SUBPROGRAM WHICH FINDS A SOLUTION FOR
\[ \left( U_g - \frac{\varepsilon}{\alpha} - \varepsilon - 2U_F \right) = \varepsilon^2 + \frac{\varepsilon}{\alpha} + U_g + U_b \]

THE METHOD USED IS NEWTON-RAPHSON METHOD

DIRECT PARAMETERS

SI CORESPONDS TO IN THE TEXT.

INDIRECT PARAMETERS (VIA COMMON STATEMENT.)

UG, UF, A, UB, US AS DEFINED IN THE TEXT.

FUNCTION ETA(SI)
COMMON UG,UF,A,UB,US
F(ET)=ET**2+ET/A-UG+UB-EXP(UG-ET/A-SI-2*UF)
FP(ET)=2*ET+1/A+(1/A)*EXP(UG-ET/A-SI-2*UF)
ETI=-1/(2*A)+SORT(1/(4*A**2)+UG-UB)
C=A*(UG-SI-2*UF)
IF(ETI.LT.C)ETI=(C-A*ALOG(C**2+C/A-UG+UB))
DO 9 I=1,100
FF=F(ETI)
FFP=FP(ETI)
ETA1=ETI-FF/FFP
FF=F(ETA1)
IF(ABS(FF).LT.1E-5)GO TO 7
ETI=ETA1
9 CONTINUE
7 ETA=ETA1
RETURN
4 ETA=C-A*ALOG(C**2+C/A-UG+UB)
RETURN
END
THIS SUBROUTINE CALCULATES THE TRANSIENT RESPONSE OF AN INVERTOR, THE RESULTS CAN BE FOUND AFTER THE EXECUTION ON A DISK FILE 'FOR20.DAT'

PARAMETERS NEEDED

SUBROUTINE TRAN(CGS,CGD,RL,RD,GM,R,VDS1,VG1)
REAL K
F(T)=VG1*A*(1-EXP(-T/K))
FF(T)=F(T)-VG1*A*(1-EXP((-1/K)*(T-1E-8)))
RT=(RD*RL)/(RD+RL)
CIN=CGS+(1+GM*RT)*CGD
K=R*CIN
A=-GM*RT

DO 9 I=1,200
T=I/1E10 - 1E-10
IF(T .GT. 1E-8)GO TO 4
Y=F(T)+VDS1
GO TO 5
4 Y=FF(T)+VDS1
5 WRITE(20,6)Y,T
6 FORMAT(1X,2G)
9 CONTINUE
7 RETURN
END
THIS IS THE LIST OF CURRENT FUNCTION SUBPROGRAM. THE PROGRAM IS BASED ON THE FORMULA PROVIDED IN THE TEXT.

DIRECT PARAMETERS

VD, VS, VG ARE DRAIN, SOURCE, AND GATE VOLTAGES RESPECTIVELY

K IS EQUAL TO $\mu \left( \frac{E_D}{I} \right)^2 \left( \frac{k \cdot T}{q \cdot A} \right)$

FUNCTION CURRENT(VG, VD, K, A, VS)

REAL K, I

COMMON UG, UF, AA, UB, US

DATA UF, UB, B/13.0533, 0.0, 38.647343/

I(ET) = K*(ET**2/2 + (2*A + 1/A)*ET + (1 - UG + UB)*ALOG(ET))

AA = A
UG = (VG - 0.5)*B
UD = VD*B
US = VS*B
ETAS = ETA(US)
ETAD = ETA(UD)

CURRENT = I(ETAS) - I(ETAD)

RETURN
END