A State Architecture Notation Specification of the Electronic Industries Association RS-232-C Generic Interchange Circuit

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Nelson E. Hastings
The Electronic Industries Association (EIA) RS-232-C recommendation is an interface specification which was introduced in August 1969 and presents a natural language specification of a 25 pin binary serial data interface between a Data Communication Equipment (DCE) and a Data Terminal Equipment (DTE). The exchange of data signals between a DCE and a DTE ultimately provides the means for DTEs to communicate on networks of DCEs interconnected by different transmission mediums possibly over great distances. The exchange of data signals between a DCE and a DTE occurs at an interface via interchange circuits.

In this thesis we will create a new specification of a generic EIA RS-232-C interchange circuit using micro State Architecture Notation (μSAN), a formal general system specification language. The μSAN specification developed will provide a formal basis by which to understand, evaluate, and analyze the natural language EIA RS-232-C generic interchange circuit specification. In addition, the merits of μSAN as a specification tool will be tested and evaluated.
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ABBREVIATIONS, NOTATIONS, AND SYMBOLS

The abbreviations, notations, and symbols used throughout this thesis and a brief explanation of each are presented in the following list. The reserved words of State Architecture Notation (µSAN) are bolded. The reader can find a detailed explanation of the µSAN notation in [10].

- **cont**: continuous type
- **Real**: the set of real numbers
- **static**: static type
- **pulsed**: pulsed type
- **and**: logical AND operation
- **or**: logical OR operation
- **MIN**: minimum operation on a set of numerical values
- **Xn**: n-th input signal range
- **Zn**: n-th output signal range
- **alias**: indicates another name for an input or output signal will follow
- **Integer**: the set of integers
- **cs**: the current state of a system
- **ns**: the next state of a system
- **FNS**: the next state function of a system
Abbreviations, Notations, and Symbols—Continued

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FOUT</td>
<td>the output function in a system</td>
</tr>
<tr>
<td>$S$</td>
<td>the state set of a system</td>
</tr>
<tr>
<td>$\exists$</td>
<td>there exists</td>
</tr>
<tr>
<td>$\therefore$</td>
<td>such that</td>
</tr>
<tr>
<td>$\in$</td>
<td>is an element of</td>
</tr>
<tr>
<td>$\star$</td>
<td>star operator of a set</td>
</tr>
<tr>
<td>$&amp;$</td>
<td>concatenation of</td>
</tr>
<tr>
<td>$\Rightarrow$</td>
<td>results in, implies</td>
</tr>
<tr>
<td>$\text{iff}$</td>
<td>if and only if</td>
</tr>
<tr>
<td>$\forall$</td>
<td>for all</td>
</tr>
<tr>
<td>$\Delta$</td>
<td>is defined as</td>
</tr>
<tr>
<td>$\sim$</td>
<td>don't care</td>
</tr>
<tr>
<td>$\mathcal{H}$</td>
<td>represents a discontinuity in the germ $\alpha$ - function</td>
</tr>
<tr>
<td>$\mathcal{V}^{(0)}, \mathcal{V}^{(1)}, \mathcal{V}^{(2)}, \ldots }$</td>
<td>Taylor series germ representation of the function $\mathcal{V}$ at an $\alpha$ - point</td>
</tr>
<tr>
<td>$\mathcal{V}^{(n)}$</td>
<td>the n-th derivative of the function $\mathcal{V}$</td>
</tr>
<tr>
<td>$\text{Dir}(\mathcal{V})$</td>
<td>direction of simple germ function $\mathcal{V}$ (positive, negative, or zero)</td>
</tr>
<tr>
<td>$\text{GT}(T, t)$</td>
<td>set of all elements in $T$ greater than $t$</td>
</tr>
<tr>
<td>$\langle H \rangle$</td>
<td>the generic abstract value of logical high</td>
</tr>
<tr>
<td>$\langle L \rangle$</td>
<td>the generic abstract value of logical low</td>
</tr>
<tr>
<td>$B$</td>
<td>busy</td>
</tr>
</tbody>
</table>
Abbreviations, Notations, and Symbols—Continued

NB  not busy

null  represents the abstract value of no germ

FSM  Finite State Machine

DSM  Discrete State Machine

$V_{Xdriver}$  driver interface voltage

$V_{Xsensor}$  sensor interface voltage

$t_{penter}$  positive driver enter time

$T_{penter}$  set of all positive driver enter times

$t_{pexit}$  positive driver exit time

$T_{pexit}$  set of all positive driver exit times

$[t_{penter}, t_{pexit}]$  positive driver transition domain

$t_{nenter}$  negative driver enter time

$T_{nenter}$  set of all negative driver enter times

$t_{nexit}$  negative driver exit time

$T_{nexit}$  set of all negative driver exit times

$[t_{nenter}, t_{nexit}]$  negative driver transition domain

$t_{senter}$  positive sensor enter time

$T_{senter}$  set of all positive sensor enter times

$t_{sexit}$  positive sensor exit time

$T_{sexit}$  set of all positive sensor exit times
Abbreviations, Notations, and Symbols—Continued

[t\textsubscript{enter} , t\textsubscript{exit}] positive sensor transition domain

\(t\textsubscript{enter}\) negative sensor enter time

\(T\textsubscript{enter}\) set of all negative sensor enter times

\(t\textsubscript{exit}\) negative sensor exit time

\(T\textsubscript{exit}\) set of all negative sensor exit times

\([t\textsubscript{enter} , t\textsubscript{exit}]\) negative sensor transition domain

\(R_L\) load resistance

\(R_O\) source resistance

\(C_O\) source capacitance

\(C_L\) load capacitance

\(C_T\) total capacitance

\(E_L\) load voltage

\(v_O\) driver voltage

\(v_{\text{noise}}\) noise voltage at the driver interface

\(v_{\text{noise}}\) noise voltage at the sensor interface

\(v_{\text{spec}}\) germ of the driver voltage \((V_O)\)

\(v_{\text{Xspec}}\) germ of the driver interface voltage \((V_{\text{Xdriver}})\)

\(v_{\text{Xspec}}\) germ of the sensor interface voltage \((V_{\text{Xsensor}})\)

\(T\) period of a signal

\(T\textsubscript{domain}(v)\) set of all driver transition domains in \(v\).
Abbreviations, Notations and Symbols--Continued

T_{\text{domain}}(v) \quad \text{set of all sensor transition domains in } v.

length \quad \text{length domain operation}

In\_Data \quad \text{static binary input signal of } \langle \text{Interchange\_Circuit} \rangle

Out\_Data \quad \text{static binary output signal of } \langle \text{Interchange\_Circuit} \rangle

Busy \quad \text{static binary output signal of } \langle \text{Interchange\_Circuit} \rangle

Error \quad \text{pulsed output signal of } \langle \text{Interchange\_Circuit} \rangle

t_{\text{now}} \quad \text{current time}

t_{\text{init}} \quad \text{initial value of a time domain}

t_{\text{final}} \quad \text{final value of a time domain}

[t_{\text{init}}, t_{\text{final}}] \quad \text{a time domain}

v_{\text{meas}} \quad \text{measured value of the driver voltage}

v_{\text{Xmeas}} \quad \text{measured value of the driver interface voltage}

V_{\text{spec Set}} \quad \text{set of valid driver voltage time functions}

V_{\text{Xspec Set}} \quad \text{set of valid driver interface voltage time functions}

V_{\text{spec Non}A} \quad \text{set of valid non-adaptive driver voltage time functions}

V_{\text{spec Ad}} \quad \text{set of valid adaptive driver voltage time functions}

P_{\text{Electrical Model Set}} \quad \text{set of valid parameter arrays}

P_{\text{Electrical Model SetAD}} \quad \text{set of valid adaptive parameter arrays}

P_{\text{Electrical Model}} \quad \text{parameter array}

V_{\text{nspec}} \quad \text{germ of the noise for the driver interface voltage } (V_{\text{noise}})
Abbreviations, Notations and Symbols—Continued

$v_{\text{naspoc}}$  germ of the noise for the sensor interface voltage ($V_{\text{noise}}$)

$B^{\cdot}$  behavior set

$B_{\text{Ad}^{\cdot}}$  behavior set for the adaptive case

$B_{\text{NonAd}^{\cdot}}$  behavior set for the non-adaptive case
A network user shares information and resources with other network users by connecting to the network. A network user connects to the network at an interface between a Data Terminal Equipment (DTE) and a Data Communication Equipment (DCE). DTEs and DCEs made by different manufacturers of communication equipment are not generally able to successfully interface with each other unless they are compatible both physically and logically. To facilitate the design and fabrication of compatible DTEs and DCEs, often a formal standard is developed. One of the first DTE/DCE interface standards to be developed was RS-232 because of the telephone companies need for communication equipment from different manufacturers to connect to the telephone network without compromising telephone service [5]. In 1969, RS-232 was developed cooperatively by Electronic Industries Association (EIA), Bell Laboratories, and manufacturers of communication equipment to solve the interfacing problems between a DTE and a DCE.

An example of a single hop network consisting of two DTEs and DCEs is shown in Figure 1 (all Figures appear in Appendix B). In the example, the network has two users with the DTE to DCE interfaces specified as RS-232. At each interface, the DTE and DCE interact with each other via data and control signals. The control signals coordinate the interaction between the DTE and DCE at an
interface. The data signals from the DTE to DCE contains the information which one user of the network is willing to share with the other network user. The data signals from the DCE to DTE contains information which is received over the network connection from one network user to the other.

The exchange of data and control signals across the DTE and DCE interface occurs using interchange circuits [15]. In general when defining an interface, a specification must cover the following four basic areas:

1. The mechanical specification must clarify how the DTE and DCE will physically be connected.

2. The electrical specification describes the voltage and timing requirements for the interface.

3. The functional specification defines the role each of the interchange circuit will play (data, timing, control, etc.).

4. The procedural specification defines the protocol which will be used by the interface.

The specification of the four basic areas can be done using various specification languages. Some of the common specification languages are natural language, Format and Protocol Language (FAPL) [8], and Very High Speed Integrated Circuit Hardware Description Language (VHDL) [9].

The Electronic Industries Association (EIA) RS-232 series of recommendations is the most common interfacing used in the United State [15]. The EIA RS-232 recommended standards provides for the capabilities of several different
types communication services. Some examples might be asynchronous or synchronous transmission, primary and secondary channels, and full or half duplex communication over the channels. The EIA RS-232-C recommendation specifies a 25 pin binary serial interface between the DTE and DCE. The EIA RS-232-C specification uses natural language plus a circuit schematic to specify the mechanical, electrical, functional, and procedural areas of an interface.

An objective of this thesis is to develop a specification of the EIA RS-232-C generic interchange circuit using micro State Architecture Notation (µSAN) [10]. µSAN is a formal general specification language used to specify system behavior and was developed to address the problem of ambiguities which arise in natural language specifications. The specifications described by µSAN are at an abstract level leaving specific implementation decisions to the implementer. The mathematical rigor of µSAN leads to sounder specifications and allows for analysis resulting in properties (theorems) which can be mathematically proven.

In this thesis, we will introduce some µSAN notation and conventions which will be used in the formal µSAN specification. A complete reference and tutorial on µSAN can be found in [10]. In addition to the new µSAN specification of the RS-232-C generic interchange circuit, we will identify inadequacies and ambiguities of the original natural language specification. The new specification will be more straight forward than the original natural language specification and will lead to the easier understanding of the RS-232-C generic interchange circuit specification. The merits of µSAN as a specification tool will be demonstrated and evaluated by
comparing the resulting µSAN specification with the original natural language specification. The remaining chapters and appendices in the thesis are as follows:

Chapter II. An Overview of the EIA RS-232-C Recommended Standard. The chapter presents a general overview of the EIA RS-232-C recommended standard and the area of the recommendation to be specified in the thesis.


Chapter IV. Ambiguities, Incompleteness, and Inadequacies Found in the EIA RS-232-C Natural Language Generic Interchange Circuit Specification. The chapter highlights the ambiguities, incompleteness and inadequacies in the EIA RS-232-C natural language generic interchange circuit as revealed by the formal µSAN specification given in Chapter III.

Appendix A. Electronic Industries Association Standard RS-232-C: Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange. This appendix contains a copy of the original EIA RS-232-C natural language specification for the reader’s cross-reference use.

Appendix B. Figures.
AN OVERVIEW OF EIA RS-232-C RECOMMENDED STANDARD

The version of the EIA RS-232 series of recommendations that will be used as a reference throughout this thesis is the EIA RS-232-C which was released in August 1969, hereafter referred to simply as RS-232-C. RS-232-C was selected to be used in this thesis because the recommended standard is an accepted and well known interface in the United States. In addition, the recommendation is not under development so it will not be changing during the development of the \textit{µSAN} specification presented in this thesis. The fact that RS-232-C addresses both analog (electrical) and digital (logical) areas in its specification makes it a good test of a specification language’s abilities. A specification language should be able to handle both analog and digital areas equally well.

RS-232-C describes a 25 pin binary serial interface between a DTE and a DCE. The 25 pins of the interface operate in parallel to enable the DTE and DCE to interact with each other. The logical signal on each of the pins is binary. RS-232-C specifies the electrical, mechanical, functional, and procedural characteristics of the interface using natural language and a circuit schematic. Since RS-232-C was released in 1969 two more versions of EIA RS-232 have been presented, EIA RS-232-D and EIA RS-232-E which were released in 1987 and 1991, respectively. The approach of the thesis will be from the point of view that only RS-232-C exists and
no other refinement of this recommendation is available. However, as part of the exercise, newer versions of RS-232 will be referenced to clear up any ambiguities or inconsistencies found in RS-232-C. For example, one of the main differences between the EIA RS-232-D and RS-232-C is that a physical connector has been fully specified in EIA RS-232-D. In RS-232-C, the only things mentioned about the physical connector is that the female connector will be associated with the DCE, the male connector will be associated with the DTE, and the length of the cable between the two connectors is unspecified except that the resulting capacitance of the load capacitor and the cable capacitance should be less than 2500 pf (see RS-232-C, p. 8, ln. 3). The configuration of the pins in the connector or the shape of the connector are two issues not mentioned in RS-232-C. Therefore, no μSAN specification of the physical adapter will be given except to say there is a 25 pin adapter with each pin associated with an interchange circuit or ground.

Figure 2 shows a general configuration of the 25 pin interface of RS-232-C including the function and interchange circuit type associated with each pin. Two of the pins are classified as ground pins which provide a common and protective ground for the DTE and DCE. The remaining 23 pins carry voltage values that convey the data, control, and timing information between the DTE and DCE. A full listing of the pin number assignments for the 25 interchange circuits and grounds in addition to the interchange circuit’s name, function, and type is given in Table 1. The function, acronym, and a brief description of the interchange circuits and grounds can be found in Table 2.
Table 1
Relationship Between Pin Number, Circuit Name, Function, and Interchange Circuit Type for an RS-232-C Interface

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Circuit Name</th>
<th>Function</th>
<th>Interchange Circuit Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AA</td>
<td>Protective Ground</td>
<td>Ground</td>
</tr>
<tr>
<td>2</td>
<td>BA</td>
<td>Transmitted Data</td>
<td>Data</td>
</tr>
<tr>
<td>3</td>
<td>BB</td>
<td>Received Data</td>
<td>Data</td>
</tr>
<tr>
<td>4</td>
<td>CA</td>
<td>Request to Send</td>
<td>Control</td>
</tr>
<tr>
<td>5</td>
<td>CB</td>
<td>Clear to Send</td>
<td>Control</td>
</tr>
<tr>
<td>6</td>
<td>CC</td>
<td>Data Set Ready</td>
<td>Control</td>
</tr>
<tr>
<td>7</td>
<td>AB</td>
<td>Signal Ground</td>
<td>Ground</td>
</tr>
<tr>
<td>8</td>
<td>CF</td>
<td>Received Line Signal Detector</td>
<td>Control</td>
</tr>
<tr>
<td>9</td>
<td>-</td>
<td>Reserved for Data Set Testing</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>-</td>
<td>Reserved for Data Set Testing</td>
<td>-</td>
</tr>
<tr>
<td>11</td>
<td>-</td>
<td>Unassigned</td>
<td>-</td>
</tr>
<tr>
<td>12</td>
<td>SCF</td>
<td>Secondary Received Line Signal Detector</td>
<td>Control</td>
</tr>
<tr>
<td>Pin Number</td>
<td>Circuit Name</td>
<td>Function</td>
<td>Interchange Circuit Type</td>
</tr>
<tr>
<td>------------</td>
<td>--------------</td>
<td>----------</td>
<td>-------------------------</td>
</tr>
<tr>
<td>13</td>
<td>SCB</td>
<td>Secondary Clear to Send</td>
<td>Control</td>
</tr>
<tr>
<td>14</td>
<td>SBA</td>
<td>Secondary Transmitted Data</td>
<td>Data</td>
</tr>
<tr>
<td>15</td>
<td>DB</td>
<td>Transmitter Signal Element Timing DCE Source</td>
<td>Timing</td>
</tr>
<tr>
<td>16</td>
<td>SBB</td>
<td>Secondary Received Data</td>
<td>Data</td>
</tr>
<tr>
<td>17</td>
<td>DD</td>
<td>Receiver Signal Element Timing DCE Source</td>
<td>Timing</td>
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<td>18</td>
<td>-</td>
<td>Unassigned</td>
<td>-</td>
</tr>
<tr>
<td>19</td>
<td>SCA</td>
<td>Secondary Request to Send</td>
<td>Control</td>
</tr>
<tr>
<td>20</td>
<td>CD</td>
<td>Data Terminal Ready</td>
<td>Control</td>
</tr>
<tr>
<td>21</td>
<td>CG</td>
<td>Signal Quality Detector</td>
<td>Control</td>
</tr>
<tr>
<td>22</td>
<td>CE</td>
<td>Ring Indicator</td>
<td>Control</td>
</tr>
<tr>
<td>23</td>
<td>CH/CI</td>
<td>Data Signal Rate Selector DTE/DCE Source</td>
<td>Control</td>
</tr>
<tr>
<td>24</td>
<td>DA</td>
<td>Transmitter Signal Element Timing DTE Source</td>
<td>Timing</td>
</tr>
<tr>
<td>25</td>
<td>-</td>
<td>Unassigned</td>
<td>-</td>
</tr>
<tr>
<td>Function</td>
<td>Acronym</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>-------------------</td>
<td>---------</td>
<td>-----------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Protective Ground</td>
<td>PG</td>
<td>Grounds the equipment to earth ground.</td>
<td></td>
</tr>
<tr>
<td>Transmitted Data</td>
<td>TD</td>
<td>Transfers data for transmission from the DTE to the DCE.</td>
<td></td>
</tr>
<tr>
<td>Received Data</td>
<td>RD</td>
<td>Transfers received data from the DCE to the DTE.</td>
<td></td>
</tr>
<tr>
<td>Request to Send</td>
<td>RTS</td>
<td>Signals the DCE that the DTE has data ready to transmit.</td>
<td></td>
</tr>
<tr>
<td>Clear to Send</td>
<td>CTS</td>
<td>Indicates to the DTE that the DCE is ready to transmit data.</td>
<td></td>
</tr>
<tr>
<td>Data Set Ready</td>
<td>DSR</td>
<td>Indicates to the DTE that the DCE is connected to a communication channel, not in a test, talk or dial mode, and any timing or answer functions have been completed.</td>
<td></td>
</tr>
<tr>
<td>Function</td>
<td>Acronym</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>-----------------------------------------------</td>
<td>---------</td>
<td>-----------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Signal Ground</td>
<td>SG</td>
<td>Provides the reference ground for all the interchange circuits.</td>
<td></td>
</tr>
<tr>
<td>Received Line Signal Detector</td>
<td>RLSD</td>
<td>Indicates to the DTE that the DCE is receiving a signal within the predefined criteria.</td>
<td></td>
</tr>
<tr>
<td>Secondary Received Line Signal Detector</td>
<td>SRLSD</td>
<td>Same as Received Line Signal except for secondary channel.</td>
<td></td>
</tr>
<tr>
<td>Secondary Clear to Send</td>
<td>SCTS</td>
<td>Same as Clear to Send except for secondary channel.</td>
<td></td>
</tr>
<tr>
<td>Secondary Transmitted Data</td>
<td>STD</td>
<td>Same as Transmitted Data except for secondary channel.</td>
<td></td>
</tr>
<tr>
<td>Transmitter Signal Element Timing (Source DTE/DCE)</td>
<td>TSET</td>
<td>Provides the DCE/DTE with the timing information from DTE/DCE for the signal on Transmitted Data.</td>
<td></td>
</tr>
<tr>
<td>Secondary Received Data</td>
<td>SRD</td>
<td>Same as Received Data except for secondary channel.</td>
<td></td>
</tr>
<tr>
<td>Function</td>
<td>Acronym</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>-----------------------------------------------</td>
<td>---------</td>
<td>-----------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Receiver Signal Element Timing (Source DCE)</td>
<td>RSET</td>
<td>Provides the DTE with the timing information from DCE for the signal on Received Data.</td>
<td></td>
</tr>
<tr>
<td>Secondary Request to Send</td>
<td>SRTS</td>
<td>Same as Request to Send except for secondary channel.</td>
<td></td>
</tr>
<tr>
<td>Data Terminal Ready</td>
<td>DTR</td>
<td>The DTE signal used to indicate that the DCE should connect to the communication channel.</td>
<td></td>
</tr>
<tr>
<td>Signal Quality Detector</td>
<td>SQD</td>
<td>Indicates the probability of error in the received data to the DTE from DCE.</td>
<td></td>
</tr>
<tr>
<td>Ring Indicator</td>
<td>RI</td>
<td>Signals the DTE that the DCE detects a ringing signal on the communication channel.</td>
<td></td>
</tr>
<tr>
<td>Data Signal Rate Selector (DTE/DCE Source)</td>
<td>DSRS</td>
<td>Indicates the data signaling rate to be used.</td>
<td></td>
</tr>
</tbody>
</table>
RS-232-C actually describes only 22 of the 25 pins in the specification. The undefined pins have been left unspecified so that they could be used in later revisions of the specification. Two pins (9 and 10) are used for testing operation of the DTE and DCE. A full complement of the remaining 20 pins may not be required at the interface depending on the type of communication services being used or available.

The different types of communication services supported by RS-232-C are transmit only, receive only, half duplex, and duplex service on a single channel or using primary and secondary channels. Both asynchronous and synchronous transmission is supported. RS-232-C incorporates data signal rates between zero and 20,000 bits per second (see RS-232-C, p. 3, ln. -4). The RS-232-C specification includes thirteen configurations for the different types of common communication services and one configuration reserved for services not covered by the other configurations. The different configurations are designated by a letter between A and M with Z being given to the uncovered configurations (see RS-232-C, p. 21). The required interchange circuits for the different specified configurations are given on page 22 of RS-232-C.

All of the interchange circuits used by an RS-232-C interface must follow specified electrical characteristics which are found in section 2 of the recommendation. The notion of specifying a generic interchange circuit can be used because all of the interchange circuits must follow the same electrical specifications defined by RS-232-C. Each of the 23 specific interchange circuits are specific
instantiations of the specified generic interchange circuits. The thesis will now proceed to develop a \( \mu \)SAN specification of the RS-232-C generic interchange circuit based on the electrical characteristics specified in RS-232-C. We will not be concerned about the mechanical, functional, or procedural aspects of RS-232-C except when they have some influence on the generic interchange circuit. The next chapter will define the scope of the RS-232-C generic interchange circuit to be covered by this thesis and give its complete \( \mu \)SAN specification.
CHAPTER III

A FORMAL SPECIFICATION OF EIA RS-232-C
GENERIC INTERCHANGE CIRCUIT

Overview of the Generic Interchange Circuit

A generic interchange circuit is the means by which an interface uses an electrical signal to exchange data, control, or timing signal between a DTE and a DCE. A RS-232-C interface utilizes a maximum of 19 out of the 20 defined interchange circuits at an interface (see Figure 3). An interchange circuit conveys information in one direction from the DTE to DCE or vice versa. The higher level components (the DTE_Mgr in a DTE and the DCE_Mgr in a DCE) use the information from the interchange circuits to allow the DTE and DCE interact at an interface and the DTE user to communicate on the network of DCEs. The specific operation of the higher level components (DTE_Mgr/DCE_Mgr) is outside the scope of this thesis.

Each of the specific interchange circuits shown in Figure 3 is specified in RS-232-C by one general (generic) interchange circuit. Each of the interchange circuits of an interface is a specific instance (instantiation) of the general interchange circuit specification.

The μSAN generic interchange circuit presented in this chapter is based on the general interchange circuit specification in Section 2 of [2]. A block diagram of the
µSAN generic interchange circuit, \( \langle \text{Interchange Circuit} \rangle \), is shown in Figure 4. RS-232-C has left the interface of the generic interchange circuit unspecified in the natural language specification. The interface described for the \( \langle \text{Interchange Circuit} \rangle \) was created by the thesis to capture the purpose of the generic interchange circuit which is to transfer user data signals. The interface of \( \langle \text{Interchange Circuit} \rangle \) has one input signal (In_Data) and three output signals (Out_Data, Busy, and Error).

In_Data and Out_Data convey user information entering and leaving \( \langle \text{Interchange Circuit} \rangle \), respectively. In_Data and Out_Data can have the static values of \( \langle H \rangle \) (generic high) or \( \langle L \rangle \) (generic low). A mapping of the generic signal values to RS-232-C signal values is based on the type of interchange circuit that is referenced (see Table 3).

<table>
<thead>
<tr>
<th>Generic Signal Value</th>
<th>Data Interchange Circuit (Binary State)</th>
<th>Timing Interchange Circuit</th>
<th>Control Interchange Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \langle L \rangle )</td>
<td>Marking (1)</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>( \langle H \rangle )</td>
<td>Spacing (0)</td>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

Busy and Error convey information from \( \langle \text{Interchange Circuit} \rangle \) to the source of In_Data to help prevent information loss. Information may be lost due to the time required by \( \langle \text{Interchange Circuit} \rangle \) to change the value of Out_Data when the value
of In_Data changes. Busy has static values to indicate that a value change of In_Data might cause information to be lost (B) or not (NB). Error is used to indicate that information has been lost by giving a pulsed output error signal. Information will be lost if the value of In_Data changes faster than Interchange_Circuit can change the value of Out_Data. By providing the Busy and Error signals, the generic interchange circuit provides information the higher level components (DTE_Mgr and DCE_Mgr) can use to help prevent information loss.

Interchange_Circuit can be refined into the following subsystems: Vo_Controller, Electrical_Model, and VX_Sensor (see Figure 5). A detailed specification of each subsystem in Interchange_Circuit will be presented in the remaining portion of this chapter. The thesis will introduce the Electrical_Model subsystem followed by an electrical analysis of the model. The results of the electrical analysis will be used to give a detailed specification of Vo_Controller and VX_Sensor.

Electrical_Model describes the equivalent electrical circuit to be used by Interchange_Circuit. Electrical_Model takes an abstract real input germ value \( V_{opp} \) from the input signal \( V_{opp} \) and converts it into a voltage source \( V_o(t) \) with the same germ magnitude characteristics. \( V_o(t) \) is applied to the specified electrical circuit resulting in two electrical output signals from specific nodes of the electronic circuitry, \( V_{x\_sensor}(t) \) and \( V_{x\_driver}(t) \). The two electrical output signals are a result of the
circuit behavior and noise inducted by the electromagnetic fields in the environment of the electrical circuit. The noise components, $V_{\text{noise}}(t)$ and $V_{\text{noise}}(t)$, will generally be different depending on where in the electrical circuit the electromagnetic fields induce currents. The electrical output signals from the circuit are presented as the abstract real output germ values $V_{X_{\text{spec}}}(t)$ and $V_{X_{\text{spec}}}(t)$ on the output signals $V_{X_{\text{spec}}}$ and $V_{X_{\text{spec}}}$ from $\langle\text{Electrical\_Model}\rangle$, respectively. A detailed description of $\langle\text{Electrical\_Model}\rangle$ is presented in Figure 6 and is derived from Figure 2.1 on page 5 of [2].

A combination of the source resistance ($R_0$), source capacitance ($C_0$), load resistance ($R_L$), load capacitance ($C_L$), and load voltage ($E_L$) will specify a specific instantiation of $\langle\text{Electrical\_Model}\rangle$. A parameter array, $p_{\text{Electrical\_Model}} = (R_0, C_0, R_L, C_L, E_L)$, is introduced to represent a specific combination of the above electrical parameters. RS-232-C specifies rules which restricts the ranges of the parameters in the array. A full listing of each parameter rule, RS-232-C rule reference, a brief rule description, and the figure containing the formalized of the natural language rule is given in table 4. $P_{\text{Electrical\_Model\_Set}}$, the set of valid parameter arrays, for $\langle\text{Electrical\_Model}\rangle$ can be derived using the RS-232-C parameter rules (see Figure 12). The parameter array and valid set of possible parameter arrays will be used in this thesis to help develop the behavior set of $\langle V_0\_\text{Controller}\rangle$. 
Table 4

The RS-232-C Rules for the Parameter Array of \langle Electrical\_Model \rangle

<table>
<thead>
<tr>
<th>Parameter Rule</th>
<th>Page and Line Reference in RS-232-C</th>
<th>Figure Number of Formal Representation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Source Resistance</td>
<td>Page 7, Line + 1</td>
<td>Figure 7</td>
<td>Source resistance ($R_o$) shall not be less than 300 $\Omega$ when the driver voltage ($V_o$) is zero.</td>
</tr>
<tr>
<td>Minimum Load Resistance</td>
<td>Page 6, Line -14</td>
<td>Figure 8</td>
<td>Load resistance ($R_L$) shall not be less than 3000 $\Omega$ when the driver voltage is between -25V and 25 V</td>
</tr>
<tr>
<td>Maximum Load Resistance</td>
<td>Page 6, Line -12</td>
<td>Figure 9</td>
<td>Load resistance ($R_L$) shall not be more than 7000 $\Omega$ when the driver voltage has a magnitude between 3 V and 25 V</td>
</tr>
<tr>
<td>Maximum Load Capacitance</td>
<td>Page 6, Line -11</td>
<td>Figure 10</td>
<td>Load capacitance ($C_L$) shall not be more than 2500 pf.</td>
</tr>
<tr>
<td>Load Voltage Range</td>
<td>Page 6, Line -9</td>
<td>Figure 11</td>
<td>Load voltage ($E_L$) shall not be more than 2V in magnitude.</td>
</tr>
</tbody>
</table>
Analysis of 〈Electrical_Model〉

An electrical analysis of the electrical circuit in 〈Electrical_Model〉 is presented. The result of the electrical analysis will yield the relationship between the driver voltage \( V_0(t) \) and the driver interface voltage \( V_{xdriver}(t) \). The relationship developed in this section will be used to help specify the behavior of 〈V_o_Controller〉. A reduced circuit diagram of 〈Electrical_Model〉 is shown in Figure 13 and will be used as the basis for the analysis of 〈Electrical_Model〉.

The interface voltage \( V_I(t) \) across the total capacitance of the electrical circuit can be written in terms of \( V_{xdriver}(t) \) and \( V_{dnoise}(t) \) or \( V_{xsensor}(t) \) and \( V_{noise}(t) \) resulting in (1) and (2), respectively.

\[
V_I(t) = V_{xdriver}(t) - V_{dnoise}(t) \quad (1)
\]

\[
V_I(t) = V_{xsensor}(t) - V_{noise}(t) \quad (2)
\]

Using Kirchhoff's Current Law,

\[
I_T(t) = I_1(t) + I_2(t) \quad (3)
\]

Component equations determine the currents in terms of \( V_O(t) \), \( V_I(t) \), \( E_L(t) \), \( R_O \), \( R_L \), and \( C_T \), (4), (5), and (6).
\[ I_T(t) = \frac{V_o(t) - V_i(t)}{R_o} \] (4)

\[ I_1(t) = C_T \frac{d}{dt} V_i(t) \] (5)

\[ I_2(t) = \frac{V_i(t) - (-E_L)}{R_L} = \frac{V_i(t) + E_L}{R_L} \] (6)

Substituting (4), (5), and (6) into (3) yields

\[ \frac{V_o(t) - V_i(t)}{R_o} = C_T \frac{d}{dt} V_i(t) + \frac{V_i(t) + E_L}{R_L} \] (7)

Now (7) will be simplified to get \( V_o(t) \) in terms of \( R_o, R_L, C_T \), and \( V_i(t) \).

\[ V_o(t) - V_i(t) = R_o C_T \frac{d}{dt} V_i(t) + \frac{R_o (V_i(t) - E_L)}{R_L} \] (8)

\[ V_o(t) = R_o C_T \frac{d}{dt} V_i(t) + \frac{R_o V_i(t)}{R_L} + V_i(t) - \frac{R_o E_L}{R_L} \] (9)
Finally, the relationship between the driver voltage $V_o(t)$ and the driver interface voltage $V_{X_{driver}}(t)$ can be derived by substituting (1) into (11) resulting in (12).

$$V_o(t) = R_0 C_T \frac{d}{dt} V_i(t) + \left( \frac{R_0}{R_L} + 1 \right) V_i(t) - \frac{R_0 E_L}{R_L}$$  \hspace{1cm} (10)

$$V_o(t) = R_0 C_T \frac{d}{dt} V_i(t) + \frac{R_L + R_0}{R_L} V_i(t) + \frac{R_0 E_L}{R_L}$$  \hspace{1cm} (11)

$$V_o(t) = R_0 C_T \frac{d}{dt} (V_{X_{driver}}(t) - V_{noise}(t)) +$$

$$\frac{R_L + R_0}{R_L} (V_{X_{driver}}(t) - V_{noise}(t)) + \frac{R_0 E_L}{R_L}$$  \hspace{1cm} (12)

The driver voltage $V_o(t)$ can be seen to be a time function of the previously defined parameter array, $P_{Electrical\_Model}$, driver interface voltage $V_{X_{driver}}(t)$, and the noise associated with the driver interface voltage $V_{noise}(t)$.

The germ representation of a time function will be introduced and applied to the derived relationship between the driver voltage and driver interface voltage. $\mu$SAN represents a time function by what is known as the germ of a function. The germ uses the Fourier, Taylor, or polynomial information of a time function at a given point in time to represent the function. In this thesis, the germ value of a time
function is the array of all time derivatives of the function. A detailed treatment of
germ concepts and notation is outside the scope of this thesis however a tutorial on
can be found in [10].

The general germs in Taylor form of the driver voltage, driver interface
voltage, sensor interface voltage, load voltage, noise voltages associated with the
driver and sensor interface voltages are given in (13), (14), (15), (16), (17), and (18),
respectively. The superscripts of the elements in the Taylor germ indicate the n-th
derivative of the specific function.

\[ V_{O_{spec}}(t) = \{V_{O_{spec}}^{(0)}(t), V_{O_{spec}}^{(1)}(t), V_{O_{spec}}^{(2)}(t), \ldots \} \] \hspace{1cm} (13)

\[ V_{X_{dspec}}(t) = \{V_{X_{dspec}}^{(0)}(t), V_{X_{dspec}}^{(1)}(t), V_{X_{dspec}}^{(2)}(t), \ldots \} \] \hspace{1cm} (14)

\[ V_{X_{spec}}(t) = \{V_{X_{spec}}^{(0)}(t), V_{X_{spec}}^{(1)}(t), V_{X_{spec}}^{(2)}(t), \ldots \} \] \hspace{1cm} (15)

\[ E_{L_{spec}}(t) = \{E_{L_{spec}}^{(0)}(t), 0, 0, 0, \ldots \} \] \hspace{1cm} (16)

\[ V_{d_{spec}}(t) = \{V_{d_{spec}}^{(0)}(t), V_{d_{spec}}^{(1)}(t), V_{d_{spec}}^{(2)}(t), \ldots \} \] \hspace{1cm} (17)

\[ V_{a_{spec}}(t) = \{V_{a_{spec}}^{(0)}(t), V_{a_{spec}}^{(1)}(t), V_{a_{spec}}^{(2)}(t), \ldots \} \] \hspace{1cm} (18)
The germs $V_{Ospec}(t)$, $V_{Xdasec}(t)$, $E_{Lspec}(t)$, and $V_{dnoise}(t)$ can be substituted into (12) for $V_0(t)$, $V_{Xdriver}(t)$, $E_L(t)$, and $V_{dnoise}(t)$ respectively, yielding the result shown in (19).

$$[V_{Ospec}^{(0)}(t), V_{Ospec}^{(1)}(t), V_{Ospec}^{(2)}(t), \ldots \ldots] =$$

$$+ R_0 C_T[V_{Xdasec}^{(1)}(t), V_{Xdasec}^{(2)}(t), V_{Xdasec}^{(3)}(t), \ldots \ldots]$$

$$- R_0 C_T[V_{dasec}^{(1)}(t), V_{dasec}^{(2)}(t), V_{dasec}^{(3)}(t), \ldots \ldots] \quad (19)$$

$$+(1+\frac{R_o}{R_L})[V_{Xdasec}^{(0)}(t), V_{Xdasec}^{(1)}(t), V_{Xdasec}^{(2)}(t), \ldots \ldots]$$

$$-(1+\frac{R_o}{R_L})[V_{dasec}^{(0)}(t), V_{dasec}^{(1)}(t), V_{dasec}^{(2)}(t), \ldots \ldots]$$

$$+ \frac{R_o}{R_L}[E_{Lspec}^{(0)}(t), 0, 0, \ldots \ldots]$$

The germ $V_{Ospec}(t)$ can be reduced to the equations specified by (20) and (21) where $n$ represents the n-th derivative of the germ.
When \( n = 0 \),

\[
V^{(0)}_{O,spec}(t) = R_0 C_T V^{(1)}_{X,spec}(t) - R_0 C_T V^{(1)}_{\text{duspec}}(t)
\]

\[
+ (1 + \frac{R_0}{R_L}) V^{(0)}_{X,spec} - (1 + \frac{R_0}{R_L}) V^{(0)}_{\text{duspec}} + \frac{R_0}{R_L} E^{(0)}_{L,spec}(t) \tag{20}
\]

\( \forall n > 0, \)

\[
V^{(n)}_{O,spec}(t) = R_0 C_T V^{(n+1)}_{X,spec}(t) - R_0 C_T V^{(n+1)}_{\text{duspec}}(t)
\]

\[
+ (1 + \frac{R_0}{R_L}) V^{(n)}_{X,spec} - (1 + \frac{R_0}{R_L}) V^{(n)}_{\text{duspec}} \tag{21}
\]

The germ of the driver voltage \( V^{(n)}_{O,spec}(t) \) can be seen to be a time function of the previously defined parameter array, \( P_{\text{Electrical Model}} \), the germ of driver interface voltage \( V^{(n)}_{X,spec}(t) \), and the germ of the noise associated with the driver interface voltage \( V^{(n)}_{\text{duspec}}(t) \).

The derived relationship between the driver voltage and driver interface voltage presented in (12), (20), and (21) will be used to help specify the behavior of \( \langle V_{O,\text{Controller}} \rangle \). A discussion of the RS-232-C definitions and constraints about the driver voltage \( V^{(n)}_{O,spec}(t) \) and driver interface voltage \( V^{(n)}_{X,spec}(t) \) will be required before the derived relationship can be used in the specification of \( \langle V_{O,\text{Controller}} \rangle \).
and its behavior.

RS-232-C Definitions and Rules for the Driver Voltage, Driver Interface Voltage, and Sensor Interface Voltage

RS-232-C specifies constraints and rules for the driver voltage, driver interface voltage, and sensor interface voltage. This section will formalize the RS-232-C natural language definitions and rules of the driver voltage, driver interface voltage, and sensor interface voltage. The application of the formalized constraints and rules combined with the constraints on the parameter array, \( \mathbf{p}_{\text{Electrical Model}} \), will restrict the behavior of \( \langle V \rangle_{\text{Controller}} \).

The only direct RS-232-C rule for the driver voltage \( V_{\text{spec}}(t) \) is its magnitude not exceed 25V (see Figure 14) (RS-232-C p. 7, ln. +5). However, the direct RS-232-C rules for the driver and sensor interface voltages will indirectly apply to the driver voltage via the relationship derived between the driver voltage, driver interface voltage and sensor interface voltage. An example of a direct RS-232-C driver and sensor interface voltage rule is that the slope of driver and sensor interface voltages shall not exceed 30 V/\( \mu \)s in magnitude (see Figure 15 and 16, respectively) (RS-232-C p. 7, ln. -8). More direct RS-232-C rules for the driver and sensor interface voltages are defined based on a mapping of the values of the driver and sensor interface voltages to an associated RS-232-C interchange circuit values. The mapping of the driver and sensor interface voltage values to RS-232-C interchange circuit values are contained in Table 5. Table 5 shows the RS-232-C interchange circuit
value, the RS-232-C reference for the mapping, the figure number of the formal representation, and a brief natural language description of mapping.

**Table 5**

Mapping of the Interface Voltage Values to RS-232-C Interchange Circuit Signal Values

<table>
<thead>
<tr>
<th>RS-232-C Interchange Circuit Signal Value</th>
<th>Page and Line Reference in RS-232-C</th>
<th>Figure Number of Formal Representation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensor marking</td>
<td>Page 5, Line - 6</td>
<td>Figure 17</td>
<td>Sensor interface voltages less than -3V are considered as marking for control interchange circuits.</td>
</tr>
<tr>
<td>Sensor OFF</td>
<td>Page 6, Line +5</td>
<td>Figure 18</td>
<td>Sensor interface voltages less than -3V are considered as OFF for data and timing interchange circuits.</td>
</tr>
<tr>
<td>Sensor spacing</td>
<td>Page 5, Line - 6</td>
<td>Figure 19</td>
<td>Sensor interface voltages greater than -3V are considered as spacing for control interchange circuits.</td>
</tr>
<tr>
<td>Sensor ON</td>
<td>Page 6, Line +5</td>
<td>Figure 20</td>
<td>Sensor interface voltages greater than -3V are considered as ON for data and timing interchange circuits.</td>
</tr>
<tr>
<td>RS-232-C Interchange Circuit Signal Value</td>
<td>Page and Line Reference in RS-232-C</td>
<td>Figure Number of Formal Representation</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------------------------------</td>
<td>------------------------------------</td>
<td>----------------------------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>Sensor Transition Region</td>
<td>Page 5, Line -2</td>
<td>Figure 21</td>
<td>Sensor interface voltages between -3V and 3V are considered in the transition region.</td>
</tr>
<tr>
<td>Driver marking</td>
<td>Page 5, Line - 6 and Page 23, Line +12</td>
<td>Figure 22</td>
<td>Driver interface voltages less than -5V are considered as marking for control interchange circuits.</td>
</tr>
<tr>
<td>Driver OFF</td>
<td>Page 6, Line +5 and Page 23, Line +12</td>
<td>Figure 23</td>
<td>Driver interface voltages less than -5V are considered as OFF for data and timing interchange circuits.</td>
</tr>
<tr>
<td>Driver spacing</td>
<td>Page 5, Line - 6 and Page 23, Line +12</td>
<td>Figure 24</td>
<td>Driver interface voltages greater than -5V are considered as spacing for control interchange circuits.</td>
</tr>
<tr>
<td>Driver ON</td>
<td>Page 6, Line +5 and Page 23, Line +12</td>
<td>Figure 25</td>
<td>Driver interface voltages greater than -5V are considered as ON for data and timing interchange circuits.</td>
</tr>
<tr>
<td>Driver Transition Region</td>
<td>Page 5, Line -2 and Page 23, Line +12</td>
<td>Figure 26</td>
<td>Driver interface voltages between -5V and 5V are considered in the transition region.</td>
</tr>
</tbody>
</table>
From the above RS-232-C definitions, RS-232-C specifies rules directly concerning the driver and sensor interface voltages when their values are in the transition region. In order to formalize the RS-232-C natural language transition region rules, the thesis will define the set function GT(\(t,T\)) and following sets: positive driver enter and exit times, positive sensor enter and exit times, positive driver transition domains, positive sensor transition domains, negative driver enter and exit times, negative sensor enter and exit times, negative driver transition domains, negative sensor transition domains, all driver transition domains, and all sensor transition domains (see Figures 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, and 37, respectively). Finally, the germ operator \(\text{DIR}(x(t))\) which gives the direction of a germ is defined (see Figure 38). The direct RS-232-C transition region rules for the driver and sensor interface voltages are listed in Table 6. Table 6 shows the transition region rule, the RS-232-C reference of the rule, the figure number of the formal representation, and a brief natural language description of the rule.
## Table 6

List of RS-232-C Transition Region Rules for Driver and Sensor Interface Voltages

<table>
<thead>
<tr>
<th>Transition Region Rule</th>
<th>Page and Line Reference in RS-232-C</th>
<th>Figure Number of Formal Representation</th>
<th>Description</th>
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<td>Driver Transition Domain Slew Rate Rule for Control Interchange Circuit</td>
<td>Page 7, Line - 13</td>
<td>Figure 39</td>
<td>For control interchange circuits, the driver interface voltage shall pass through the transition region within 1 millisecond.</td>
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<td>Sensor Transition Domain Slew Rate Rule for Control Interchange Circuit</td>
<td>Page 7, Line - 13</td>
<td>Figure 40</td>
<td>For control interchange circuits, the sensor interface voltage shall pass through the transition region within 1 millisecond.</td>
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<td>Driver Transition Domain Slew Rate Rule for Data and Timing Interchange Circuit</td>
<td>Page 7, Line - 11</td>
<td>Figure 41</td>
<td>For data and timing interchange circuits, the driver interface voltage shall pass through the transition region within 1 millisecond or 4 percent of the period of the signal which ever is less.</td>
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Table 6--Continued

<table>
<thead>
<tr>
<th>Transition Region Rule</th>
<th>Page and Line Reference in RS-232-C</th>
<th>Figure Number of Formal Representation</th>
<th>Description</th>
</tr>
</thead>
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<td>Sensor Transition</td>
<td>Page 7, Line - 11</td>
<td>Figure 42</td>
<td>For data and timing interchange circuits, the sensor interface voltage shall pass through the transition region within 1 millisecond or 4 percent of the period of the signal which ever is less.</td>
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<td>Domain Slew Rate Rule for Data and Timing Interchange Circuit</td>
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<td>Driver Transition</td>
<td>Page 7, Line - 15</td>
<td>Figure 43</td>
<td>The direction of the driver interface voltage shall not change while in the transition region.</td>
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<tr>
<td>Domain Direction Rule</td>
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<tr>
<td>Sensor Transition</td>
<td>Page 7, Line - 15</td>
<td>Figure 44</td>
<td>The direction of the sensor interface voltage shall not change while in the transition region.</td>
</tr>
<tr>
<td>Domain Direction Rule</td>
<td></td>
<td></td>
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\(\langle V_{o\_Controller} \rangle\)

The specification of \(\langle V_{o\_Controller} \rangle\) will be presented in this section. RS-232-C does not give a mapping of the input signal In_Data to the output signal \(V_{Ospec}\); this means \(\langle V_{o\_Controller} \rangle\) is an undefined system. This thesis captures the undefinedness in formal terms by specifying the valid behavior of the system; i.e., the valid behavior of \(\langle V_{o\_Controller} \rangle\) is the set of all possible time functions for
output signal $V_{O_{spec}}$ that satisfies the constrains on $V_{O_{spec}}$ and which produce only valid driver interface voltage time functions $V_{X_{driver}}$. The thesis will make the assumptions that no noise will be associated with the driver interface voltage $V_{X_{driver}}$ and the parameter array of the $\langle$Electrical_Model$\rangle$ is constant over time. These assumptions are required in order to specify the set of valid behaviors for $\langle V_{o\_Controller} \rangle$. The valid set of driver interface voltage time functions $V_{X_{driver}Set}$ is defined Figures 45 and 46. A valid driver interface voltage time function must follow all the constraints and rules specified by RS-232-C (see Table 6 and Figure 15). An example of a valid driver interface voltage time function is shown in Figure 47.

Many implementation strategies for generating the output signal $V_{O_{spec}}$ of $\langle V_{o\_Controller} \rangle$ can be selected. This thesis will focus on a non-adaptive implementation strategy and an adaptive implementation strategy. The non-adaptive implementation strategy will cause $\langle V_{o\_Controller} \rangle$ to act in a conservative manor when generating $V_{O_{spec}}$. Under the non-adaptive strategy, $\langle V_{o\_Controller} \rangle$ does not observe or use the driver interface voltage information provided by $\langle$Electrical_Model$\rangle$. $\langle V_{o\_Controller} \rangle$ will not know anything about the parameter array of $\langle$Electrical_Model$\rangle$ and must assume any of the possible parameter arrays maybe present. $\langle V_{o\_Controller} \rangle$ must generate a driver voltage $V_{O_{spec}}$ which will produce a valid driver interface voltage regardless of the parameter array present in $\langle$Electrical_Model$\rangle$. The set of preliminary driver interface voltage time functions $V_{O_{spec} Set}$ is shown in Figure 48. The only direct RS-232-C constraint on the driver
voltage $V_{\text{spec}}$ is its value must not be greater than 25 V in magnitude (see Figure 14). Using $V_{\text{spec}} \text{Set}$, the set of non-adaptive driver voltage time functions $V_{\text{spec NonAd}}$ is defined in Figure 49.

The adaptive implementation strategy allows $\langle V_\alpha \text{-Controller} \rangle$ to generate the driver voltage $V_{\text{spec}}$ based on a restricted set of parameter arrays in $\langle \text{Electrical Model} \rangle$. $\langle V_\alpha \text{-Controller} \rangle$ uses the information about the driver interface voltage which the $\langle \text{Electrical Model} \rangle$ provides. Under the adaptive strategy, $\langle V_\alpha \text{-Controller} \rangle$ will measure the driver voltage $V_{\text{spec meas}}$ and the driver interface voltage $V_{\text{Xdmeas}}$. Using the derived relationship between $V_{\text{spec}}$ and $V_{\text{Xdmeas}}$ and the measured values, $\langle V_\alpha \text{-Controller} \rangle$ can determine a restrictive set of possible parameter arrays for $\langle \text{Electrical Model} \rangle$ (see Figure 50).

A detailed specification of the non-adaptive and adaptive $\langle V_\alpha \text{-Controller} \rangle$ is given in Figures 51 and 52. The state of $\langle V_\alpha \text{-Controller} \rangle$ is the current value of the output signal, $V_{\text{spec}}$. The behavior of Busy and Error is not specified by RS-232-C hence they are not specified in Figures 51 and 52. An example of a behavior time function of $\langle V_\alpha \text{-Controller} \rangle$ is shown in Figure 53.

$\langle V_{X \text{-Sensor}} \rangle$

$\langle V_{X \text{-Sensor}} \rangle$ is a finite state machine that converts the sensor interface germ voltage input signal $V_{\text{Xspec}}$ into a binary static output signal Out_Data. A detailed description of $\langle V_{X \text{-Sensor}} \rangle$ is presented in Figure 54. The next state of $\langle V_{X \text{-Sensor}} \rangle$ is determined by its current state and the current value of $V_{\text{Xspec}}$. The
next state function (1) derives from a page 3, line + 18 of [3] which states a change in the state from \( \langle L \rangle \) to \( \langle H \rangle \) occurs at the instant the sensor interface voltage crosses + 3V in the positive direction. The next state function (2) derives from a page 3, line + 20 of [3] which states a change in the state from \( \langle H \rangle \) to \( \langle L \rangle \) occurs at the instant the sensor interface voltage crosses - 3V in the negative direction. An example behavior of \( \langle V_{x \_Sensor} \rangle \) is shown in Figure 55.
CHAPTER IV

AMBIGUITIES, INCOMPLETENESS, AND INADEQUACIES FOUND IN THE EIA RS-232-C NATURAL LANGUAGE GENERIC INTERCHANGE CIRCUIT SPECIFICATION

Introduction

This section will focus on the ambiguities, incompleteness, and inadequacies found in the EIA RS-232-C natural language generic interchange circuit specification. The ability of μSAN to reveal the shortcomings of the natural language specification of EIA RS-232-C demonstrates its usefulness as a specification tool.

Short Circuit Rule Ambiguity

μSAN helped us see that the short circuit condition rule (see RS-232-C, p. 7, In. +8) is not clear on whether it should be applied to steady state or dynamic interface voltage conditions. The short circuit condition rule states no current greater than half an ampere should be generate by the generic interchange circuit. The short circuit condition rule can be violated if a short circuit occurs across a capacitor (C_L or C_0) in the generic interchange circuit. The instantaneous current generated by the short circuit would result in an infinite current (due to dV_c / dt = ∞ and i_c = C dV_c / dt = ∞).
Interface Voltage Rule Ambiguity

An interface voltage rule (see RS-232-C, p. 7, ln. +10) is also not clear on whether it should be applied to steady state or dynamic interface voltage conditions. The ambiguous interface voltage rule states that when the load resistance ($R_o$) is between 3000 Ω and 7000 Ω and the load voltage ($E_L$) is zero then the interface voltage should be between 5 and 15 volts. The interface voltage rule cannot be true when a transition is occurring in the interface voltage signal. The interface voltage must pass between ± 5 volts during a transition of the voltage signal condition.

A steady state interpretation for the rules in question was acquired from an interview with Mr. Fred Lucus of General Data Communication, an expert on RS-232. Any statement in RS-232-C which relies on a steady state interface voltage signal definition is ambiguous because no definition of a steady state condition exists in the RS-232-C specification.

Transition Region Reversal Redundancy

A redundancy was found in the RS-232-C statements of p. 7, ln. -15 and p. 7, ln. -18. The first statement states that no reversal of the direction of the rate of voltage change will occur while the interface voltage signals $V_{x_{sensor}}$ and $V_{x_{driver}}$ is in the transition region. The next statement states that interface voltage signals $V_{x_{sensor}}$ and $V_{x_{driver}}$ entering the transition region will proceed through to the opposite signal condition. If a voltage signal enters the transition region at one side and may not
change direction, then the voltage signal must exit at the opposite signal condition.

For the voltage signal to leave the side of the transition region which it entered, the voltage signal would have to change its direction which would violate the first statement. The two statements have the same effect on the specification resulting in one of the statements not being required.

Sensor Interface Voltage Incompleteness

\( \mu \text{SAN} \) revealed incompleteness in the definition of the sensor interface voltage values. RS-232-C clearly maps the sensor interface voltage values into the following RS-232-C generic interchange circuit values: sensor interface voltage values above 3V are considered marking or ON, sensor interface voltage values below -3V are considered spacing or OFF, and sensor interface voltage values between -3V and 3V are considered in the sensor transition region. The sensor interface voltage values of ±3V are not mapped into a RS-232-C generic interchange circuit value. The mapping of the sensor interface voltage values to RS-232-C generic interchange values is shown to be incomplete.

Interface Voltage Definition Ambiguity

RS-232-C gives a mapping of the interface voltage values to \( H \) / \( L \) data values and defines a noise margin. RS-232-C does not address how the electromagnetic noise of the environment will affect the interface voltages of the generic interchange circuit. The thesis introduces a driver interface voltage \( V_{X\text{driver}} \).
and sensor interface voltage $V_{x_{\text{Sensor}}}$ relative to the general interface voltage $V_1$ defined by RS-232-C because of the noise in the environment of the generic interchange circuit. The RS-232-C mapping is based on the general interface voltage which results in the ambiguity of how the driver and sensor interface voltage values with noise should be mapped to $\langle H \rangle / \langle L \rangle$ data values.

**Data Transfer Incompleteness**

The $\mu$SAN specification demonstrated the total incompleteness of RS-232-C to specify the transfer of the user $\langle H \rangle / \langle L \rangle$ data values from the driver, $\langle V_{o_{\text{Controller}}} \rangle$, to the sensor, $\langle V_{x_{\text{Sensor}}} \rangle$. The fundamental purpose of the generic interchange circuit, the transfer of user data, is essentially left unaddressed in the natural language specification. RS-232-C does not define the user interface of the generic interchange circuit. The interface specification is left to be specified by the users and designers of the generic interchange circuit. The result will be different interface specification by different users and designers. The interface presented for $\langle \text{Interchange\_Circuit} \rangle$ was created to cover this inadequacy of the natural language specification.

RS-232-C gives a mapping of the interface voltage values to $\langle H \rangle / \langle L \rangle$ data values, but fails to completely specify the behavior of the generic interchange circuit when a change in the data value occurs. RS-232-C specifies the dynamic behavior of the interface voltages in the transition region but not outside the transition region. The result is the specification of the non-deterministic system $\langle V_{o_{\text{Controller}}} \rangle$. A
complete specification of the transfer of user data would have resulted in a
deterministic $V_{\alpha\text{-Controller}}$.

The RS-232-C specification was shown to be incomplete by this thesis. A
revised formal specification of RS-232-C would help address the items highlighted
above to have a more complete, sound, and clear specification.
Appendix A

Electronics Industries Association Standard RS-232-C: Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange

1 Copied here with permission from the Electronic Industries Association.
EIA STANDARD

Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange

RS-232-C

August 1969

Engineering Department

ELECTRONIC INDUSTRIES ASSOCIATION
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INTERFACE BETWEEN DATA TERMINAL EQUIPMENT
AND DATA COMMUNICATION EQUIPMENT EMPLOYING
SERIAL BINARY DATA INTERCHANGE

(From EIA Standard RS-232-B and Standards Proposal No. 1012 formulated under
the cognizance of EIA Subcommittee TR-30.2 on Interface.)

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SECTION ONE

1. SCOPE

1.1 This standard is applicable to the interconnection of data terminal equipment (DTE) and data communication equipment (DCE) employing serial binary* data interchange. It defines:

Section 2 — Electrical Signal Characteristics:—

Electrical characteristics of the interchange signals and associated circuitry.

Section 3 — Interface Mechanical Characteristics:—

Definition of the mechanical characteristics of the interface between the data terminal equipment and the data communication equipment.

Section 4 — Functional Description of Interchange Circuits:—

Functional description of a set of data, timing and control interchange circuits for use at a digital interface between data terminal equipment and data communication equipment.

Section 5 — Standard Interfaces for Selected Communication System Configurations:—

Standard subsets of specific interchange circuits are defined for a specific group of data communication system applications.

In addition, the standard includes:

Section 6 — Recommendations and Explanatory Notes
Section 7 — Glossary of New Terms

1.2 This standard includes thirteen specific interface configurations intended to meet the needs of fifteen defined system applications. These configurations are identified by type, using alphabetic characters A through M. In addition, type Z has been reserved for applications not covered by types A through M, and where the configuration of interchange circuits is to be specified, in each case, by the supplier.

1.3 This standard is applicable for use at data signalling rates in the range from zero to a nominal upper limit of 20,000 bits per second.

1.4 This standard is applicable for the interchange of data, timing and control signals when used in conjunction with electronic equipment, each of which has a single common return (signal ground).

*See section 6.1.
that can be interconnected at the interface point. It does not apply where electrical isolation between equipment on opposite sides of the interface point is required.

1.5 This standard applies to both synchronous and nonsynchronous serial binary data communication systems.

1.6 This standard applies to all classes of data communication service, including:

1.6.1 Dedicated leased or private line service, either two wire or four wire. Consideration is given to both point-to-point and multipoint operation.

1.6.2 Switched network service, either two-wire or four-wire. Consideration is given to automatic answering of calls; however, this standard does not include all of the interchange circuits required for automatically originating a connection. (See EIA Standard RS-366 "Interface Between Data Terminal Equipment and Automatic Calling Equipment for Data Communication").

1.7 The data set may include transmitting and receiving signal converters as well as control functions. Other functions, such as pulse regeneration, error control, etc., may or may not be provided. Equipment to provide these additional functions may be included in the data terminal equipment or in the data communication equipment, or it may be implemented as a separate unit interposed between the two.

1.7.1 When such additional functions are provided within the data terminal equipment or the data communication equipment, this interface standard shall apply only to the interchange circuits between the two classes of equipment.

1.7.2 When additional functions are provided in a separate unit inserted between the data terminal equipment and the data communication equipment, this standard shall apply to both sides (the interface with the data terminal equipment and the interface with the data communication equipment — See Section 3.1.1) of such separate unit.

1.8 This standard applies to all of the modes of operation afforded under the system configurations indicated in Section 5, Standard Interfaces for Selected Communication System Configurations.

SECTION TWO

2. ELECTRICAL SIGNAL CHARACTERISTICS

2.1 Figure 2.1, Interchange Equivalent Circuit, shows the electrical parameters which are specified in the subsequent paragraphs of this section. The equivalent circuit shown in Figure 2.1 is applicable to all interchange circuits regardless of the category (data, timing, or control) to which they belong. The equivalent circuit is independent of whether the driver is located in the data communication equipment and the terminator in the data terminal equipment or vice versa.
FIGURE 2.1 - INTERCHANGE EQUIVALENT CIRCUIT

\( V_O \) is the open-circuit driver voltage.

\( R_O \) is the driver internal dc resistance.

\( C_O \) is the total effective capacitance associated with the driver, measured at the interface point and including any cable to the interface point.

\( V_1 \) is the voltage at the interface point.

\( C_L \) is the total effective capacitance associated with the terminator, measured at the interface point and including any cable to the interface point.

\( R_L \) is the terminator load dc resistance.

\( E_L \) is the open circuit terminator voltage (bias).

2.2 The driver on an interchange circuit shall be designed to withstand an open circuit, a short circuit between the conductor carrying that interchange circuit in the interconnecting cable and any other conductor in that cable, or any passive non-inductive load connected between that interchange circuit and any other interchange circuit including Circuit AB (Signal Ground), without sustaining damage to itself or its associated equipment. The terminator on an interchange circuit shall be designed to withstand any input signal within the 25 volt limit specified in section 2.6. (see Section 6.6).

2.3 For data interchange circuits, the signal shall be considered in the marking condition when the voltage \( (V_1) \) on the interchange circuit, measured at the interface point, is more negative than minus three volts with respect to Circuit AB (Signal Ground). The signal shall be considered in the spacing condition when the voltage \( (V_1) \) is more positive than plus three volts with respect to circuit AB (see 6.3). The region between plus three volts and minus three volts is defined as the transition region. The signal state is not uniquely defined when the voltage \( (V_1) \) is in this transition region.
During the transmission of data, the marking condition shall be used to denote the binary state ONE and the spacing condition shall be used to denote the binary state ZERO.

For timing and control interchange circuits, the function shall be considered ON when the voltage \(V_J\) on the interchange circuit is more positive than plus three volts with respect to circuit AB, and shall be considered OFF when the voltage \(V_J\) is more negative than minus three volts with respect to Circuit AB. The function is not uniquely defined for voltages in the transition region between plus three volts and minus three volts.

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This specification neither implies nor precludes the use of terminator circuits which utilize hysteresis techniques to enhance their noise immunity; however, the requirements of section 2.5 must also be satisfied.

2.4 The load impedance \(R_L\) and \(C_L\) of the terminator side of an interchange circuit shall have a dc resistance \(R_L\) of not less than 3000 Ohms, measured with an applied voltage not greater than 25 volts in magnitude, nor more than 7000 Ohms, measured with an applied voltage of 3 to 25 volts in magnitude. The effective shunt capacitance \(C_L\) of the terminator side of an interchange circuit, measured at the interface point, shall not exceed 2500 picofarads. The reactive component of the load impedance shall not be inductive. The open circuit terminator voltage \(E_L\) shall not exceed 2 volts in magnitude. (See sections 6.4, 6.5, and 6.6).

2.5 The following interchange circuits, where implemented, shall be used to detect either a power-off condition in the equipment connected across the interface, or the disconnection of the interconnecting cable:

- Circuit CA (Request to Send)
- Circuit CC (Data Set Ready)
- Circuit CD (Data Terminal Ready)
- Circuit SCA (Secondary Request to Send)
The power-off source impedance of the driver side of these circuits shall not be less than 300 Ohms, measured with an applied voltage not greater than 2 volts in magnitude referenced to Circuit AB (Signal Ground). The terminator for these circuits shall interpret the power-off condition or the disconnection of the interconnecting cable as an OFF condition.

2.6 The open-circuit driver voltage \( V_D \) with respect to Circuit AB (Signal Ground) on any interchange circuit shall not exceed 25 volts in magnitude. The source impedance \( R_D \text{ and } C_D \) of the driver side of an interchange circuit including any cable to the interface point is not specified; however, the combination of \( V_D \) and \( R_D \) shall be selected such that a short circuit between any two conductors (including ground) in the interconnecting cable shall not result in a current in excess of one-half ampere. Additionally, the driver design shall be such that, when the terminator load resistance \( R_L \) is in the range between 3000 Ohms and 7000 Ohms and the terminator open circuit voltage \( E_L \) is zero, the potential \( V_I \) at the interface point shall not be less than 5 volts nor more than 15 volts in magnitude (see section 6.5).

2.7 The characteristics of the interchange signals transmitted across the interface point, exclusive of external interference, shall conform to the limitations specified in this section. These limitations shall be satisfied at the interface point when the interchange circuit is terminated with any receiving circuit which meets the requirements given in Section 2.4. These limitations apply to all interchange signals (Data, Control and Timing) unless otherwise specified.

(1) All interchange signals entering into the transition region shall proceed through the transition region to the opposite signal state and shall not reenter the transition region until the next significant change of signal condition.

(2) There shall be no reversal of the direction of voltage change while the signal is in the transition region.

(3) For Control Interchange Circuits, the time required for the signal to pass through the transition region during a change in state shall not exceed one millisecond.

(4) For Data and Timing interchange Circuits, the time required for the signal to pass through the transition region shall not exceed one millisecond or four percent of the nominal duration of a signal element on that interchange circuit, whichever is the lesser.

(5) The maximum instantaneous rate of voltage change shall not exceed 30 volts per microsecond.

SECTION THREE

3. INTERFACE MECHANICAL CHARACTERISTICS

3.1 The interface between the data terminal equipment and data communication equipment is located at a pluggable connector signal interface point between the two equipments. The female connector shall be associated with, but not necessarily physically attached to the data communication equipment and should be mounted in a fixed position near the data terminal equipment. The use of an
extension cable on the data communication equipment is permitted. An extension cable with a male connector shall be provided with the data terminal equipment. The use of short cables (each less than approximately 50 feet or 15 meters) is recommended; however, longer cables are permissible, provided that the resulting load capacitance (C_L of Fig. 2.1), measured at the interface point and including the signal terminator, does not exceed 2500 picofarads. (See section 2.4 and 6.5.)

3.1.1 When additional functions are provided in a separate unit inserted between the data terminal equipment and the data communication equipment (See section 1.7), the female connector, as indicated above shall be associated with the side of this unit which interfaces with the data terminal equipment while the extension cable with the male connector shall be provided on the side which interfaces with the data communication equipment.

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Circuit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AA</td>
<td>Protective Ground</td>
</tr>
<tr>
<td>2</td>
<td>BA</td>
<td>Transmitted Data</td>
</tr>
<tr>
<td>3</td>
<td>BB</td>
<td>Received Data</td>
</tr>
<tr>
<td>4</td>
<td>CA</td>
<td>Request to Send</td>
</tr>
<tr>
<td>5</td>
<td>CB</td>
<td>Clear to Send</td>
</tr>
<tr>
<td>6</td>
<td>CC</td>
<td>Data Set Ready</td>
</tr>
<tr>
<td>7</td>
<td>AB</td>
<td>Signal Ground (Common Return)</td>
</tr>
<tr>
<td>8</td>
<td>CF</td>
<td>Received Line Signal Detector</td>
</tr>
<tr>
<td>9</td>
<td>-</td>
<td>(Reserved for Data Set Testing)</td>
</tr>
<tr>
<td>10</td>
<td>-</td>
<td>(Reserved for Data Set Testing)</td>
</tr>
<tr>
<td>11</td>
<td>SCF</td>
<td>Unassigned (See Section 3.2.2)</td>
</tr>
<tr>
<td>12</td>
<td>SCB</td>
<td>Sec. Rec'd. Line Sig. Detector</td>
</tr>
<tr>
<td>13</td>
<td>SCA</td>
<td>Sec. Clear to Send</td>
</tr>
<tr>
<td>14</td>
<td>SBA</td>
<td>Secondary Transmitted Data</td>
</tr>
<tr>
<td>15</td>
<td>DB</td>
<td>Transmission Signal Element Timing (DCE Source)</td>
</tr>
<tr>
<td>16</td>
<td>SBB</td>
<td>Secondary Received Data</td>
</tr>
<tr>
<td>17</td>
<td>DD</td>
<td>Receiver Signal Element Timing (DCE Source)</td>
</tr>
<tr>
<td>18</td>
<td>-</td>
<td>Unassigned</td>
</tr>
<tr>
<td>19</td>
<td>SCA</td>
<td>Secondary Request to Send</td>
</tr>
<tr>
<td>20</td>
<td>CD</td>
<td>Data Terminal Ready</td>
</tr>
<tr>
<td>21</td>
<td>CG</td>
<td>Signal Quality Detector</td>
</tr>
<tr>
<td>22</td>
<td>CE</td>
<td>Ring Indicator</td>
</tr>
<tr>
<td>23</td>
<td>CH/CI</td>
<td>Data Signal Rate Selector (DTE/DCE Source)</td>
</tr>
<tr>
<td>24</td>
<td>DA</td>
<td>Transmit Signal Element Timing (DTE Source)</td>
</tr>
<tr>
<td>25</td>
<td></td>
<td>Unassigned</td>
</tr>
</tbody>
</table>

Figure 3.1
Interface Connector Pin Assignments
3.2 Pin Identification

3.2.1 Pin assignments listed in Figure 3.1 shall be used.

3.2.2 Pin assignments for circuits not specifically defined in section 4 (See section 4.1.1.) are to be made by mutual agreement. Preference should be given to the use of unassigned pins, but in the event that additional pins are required extreme caution should be taken in their selection.

SECTION FOUR

4. FUNCTIONAL DESCRIPTION OF INTERCHANGE CIRCUITS

4.1 General

This section defines the basic interchange circuits which apply, collectively, to all systems.

4.1.1 Additional interchange circuits not defined herein, or variations in the functions of the defined interchange circuits may be provided by mutual agreement. See sections 3.2.2. and 5.2.

4.2 Categories

Interchange circuits between data terminal equipment and data communication equipment fall into four general categories.

Ground or Common Return
Data Circuits
Control Circuits
Tuning Circuits

4.2.1 A list or circuits showing category as well as equivalent C.C.L.T.T. identification in accordance with Recommendation V.24 is presented in Figure 4.1.

4.3 Signal Characteristics, General

4.3.1 Interchange circuits transferring data signals across the interface point shall hold marking (binary ONE) or spacing (binary ZERO) conditions for the total nominal duration of each signal element.

In synchronous systems using synchronous data communication equipment, distortion tolerances as specified in RS-3341 shall apply. Acceptable distortion tolerances for data terminal equipment in synchronous and start-stop (i.e. asynchronous) systems using non-synchronous

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data communication equipment are under consideration for a future companion standard to RS-334.

4.3.2 Interchange circuits transferring timing signals across the interface point shall hold ON and OFF conditions for nominally equal periods of time, consistent with acceptable tolerances as specified in RS-334. During periods when timing information is not provided on a timing interchange circuit, this interchange circuit shall be clamped in the OFF condition.

4.3.3 Tolerances on the relationship between data and associated timing signals shall be in accordance with RS-334.

<table>
<thead>
<tr>
<th>Interchange Circuit</th>
<th>CCITT Equivalent</th>
<th>Description</th>
<th>Gnd From DCE</th>
<th>Data From DCE</th>
<th>Control From DCE</th>
<th>Timing From DCE</th>
<th>Timing To DCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>AA 101</td>
<td></td>
<td>Protective Ground</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AB 102</td>
<td></td>
<td>Signal Ground/Common Return</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BA 103</td>
<td></td>
<td>Transmitted Data</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BB 104</td>
<td></td>
<td>Received Data</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CA 105</td>
<td></td>
<td>Request to Send</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CB 106</td>
<td></td>
<td>Clear to Send</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CC 107</td>
<td></td>
<td>Data Set Ready</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CD 108.2</td>
<td></td>
<td>Data Terminal Ready</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CE 125</td>
<td></td>
<td>Ring Indicator</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CF 109</td>
<td></td>
<td>Received Line Signal Detector</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CG 110</td>
<td></td>
<td>Signal Quality Detector</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH 111</td>
<td></td>
<td>Data Signal Rate Selector (DTE)</td>
<td>X</td>
<td>X</td>
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<td></td>
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<tr>
<td>CI 112</td>
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<td>Data Signal Rate Selector (DCE)</td>
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<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DA 113</td>
<td></td>
<td>Transmitter Signal Element Timing (DTE)</td>
<td>X</td>
<td>X</td>
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<td>DB 114</td>
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<td>Transmitter Signal Element Timing (DCE)</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DD 115</td>
<td></td>
<td>Receiver Signal Element Timing (DCE)</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
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<tr>
<td>SBA 118</td>
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<td>Secondary Transmitted Data</td>
<td>X</td>
<td></td>
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<td></td>
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<tr>
<td>SBB 119</td>
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<td>Secondary Received Data</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>SCA 120</td>
<td></td>
<td>Secondary Request to Send</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>SCB 121</td>
<td></td>
<td>Secondary Clear to Send</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCF 122</td>
<td></td>
<td>Secondary Rec’d Line Signal Detector</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 4.1
Interchange Circuits by Category
4.4 Interchange Circuits

Circuit AA — Protective Ground (C.C.I.T.T: 101)
Direction: Not applicable

This conductor shall be electrically bonded to the machine or equipment frame. It may be further connected to external grounds as required by applicable regulations.

Circuit AB — Signal Ground or Common Return (C.C.I.T.T. 102)
Direction: Not applicable

This conductor establishes the common ground reference potential for all interchange circuits except Circuit AA (Protective Ground). Within the data communication equipment, this circuit shall be brought to one point, and it shall be possible to connect this point to Circuit AA by means of a wire strap inside the equipment. This wire strap can be connected or removed at installation, as may be required to meet applicable regulations or to minimize the introduction of noise into electronic circuitry.

Circuit BA — Transmitted Data (C.C.I.T.T. 103)
Direction: TO data communication equipment

Signals on this circuit are generated by the data terminal equipment and are transferred to the local transmitting signal converter for transmission of data to remote data terminal equipment.

The data terminal equipment shall hold Circuit BA (Transmitted Data) in marking condition during intervals between characters or words, and at all times when no data are being transmitted.

In all systems, the data terminal equipment shall not transmit data unless an ON condition is present on all of the following four circuits, where implemented.

1. Circuit CA (Request to Send)
2. Circuit CB (Clear to Send)
3. Circuit CC (Data Set Ready)
4. Circuit CD (Data Terminal Ready)

All data signals that are transmitted across the interface on interchange circuit BA (Transmitted Data) during the time an ON condition is maintained on all of the above four circuits, where implemented, shall be transmitted to the communication channel.

See Section 4.3, for signal characteristics.

Circuit BB — Received Data (C.C.I.T.T. 104)
Direction: FROM data communication equipment

Signals on this circuit are generated by the receiving signal converter in response to data signals received from remote data terminal equipment via the remote transmitting signal converter. Circuit BB
(Received Data) shall be held in the binary ONE (Marking) condition at all times when Circuit CF (Received Line Signal Detector) is in the OFF condition.

On a half duplex channel, Circuit BB shall be held in the Binary ONE (Marking) condition when Circuit CA (Request to Send) is in the ON condition and for a brief interval following the ON to OFF transition of Circuit CA to allow for the completion of transmission (See Circuit BA – Transmitted Data) and the decay of line reflections. See section 4.3 for signal characteristics.

**Circuit CA – Request to Send (C.C.I.T.T. 105)**

**Direction:** TO data communication equipment

This circuit is used to condition the local data communication equipment for data transmission and, on a half duplex channel, to control the direction of data transmission of the local data communication equipment.

On one way only channels or duplex channels, the ON condition maintains the data communication equipment in the transmit mode. The OFF condition maintains the data communication equipment in a non-transmit mode.

On a half duplex channel, the ON condition maintains the data communication equipment in the transmit mode and inhibits the receive mode. The OFF condition maintains the data communication equipment in the receive mode.

A transition from OFF to ON instructs the data communication equipment to enter the transmit code (see Section 6.8). The data communication equipment responds by taking such action as may be necessary and indicates completion of such actions by turning ON Circuit CB (Clear to Send), thereby indicating to the data terminal equipment that data may be transferred across the interface point on interchange Circuit BA (Transmitted Data).

A transition from ON to OFF instructs the data communication equipment to complete the transmission of all data which was previously transferred across the interface point on interchange Circuit BA and then assume a non-transmit mode or a receive mode as appropriate. The data communication equipment responds to this instruction by turning OFF Circuit CB (Clear to Send) when it is prepared to again respond to a subsequent ON condition of Circuit CA.

**NOTE:** A non-transmit mode does not imply that all line signals have been removed from the communication channel. See section 6.8.

When Circuit CA is turned OFF, it shall not be turned ON again until Circuit CB has been turned OFF by the data communication equipment.

An ON condition is required on Circuit CA as well as on Circuit CB, Circuit CC (Data Set Ready) and, where implemented, Circuit CD (Data Terminal Ready) whenever the data terminal equipment transfers data across the interface on interchange Circuit BA.

It is permissible to turn Circuit CA ON at any time when Circuit CB is OFF regardless of the condition of any other interchange circuit.
Circuit CB — Clear to Send (C.C.I.T.T. 106)
Direction: FROM data communication equipment

Signals on this circuit are generated by the data communication equipment to indicate whether or not the data set is ready to transmit data.

The ON condition together with the ON condition on interchange circuits CA, CC and, where implemented, CD, is an indication to the data terminal equipment that signals presented on Circuit BA (Transmitted Data) will be transmitted to the communication channel.

The OFF condition is an indication to the data terminal equipment that it should not transfer data across the interface on interchange Circuit BA.

The ON condition of Circuit CB is a response to the occurrence of a simultaneous ON condition on Circuits CC (Data Set Ready) and Circuit CA (Request to Send), delayed as may be appropriate to the data communication equipment for establishing a data communication channel (including the removal of the MARK HOLD clamp from the Received Data interchange circuit of the remote data set) to a remote data terminal equipment.

Where Circuit CA (Request to Send) is not implemented in the data communication equipment with transmitting capability, Circuit CA shall be assumed to be in the ON condition at all times, and Circuit CB shall respond accordingly.

Circuit CC — Data Set Ready (C.C.I.T.T. 107)
Direction: FROM data communication equipment

Signals on this circuit are used to indicate the status of the local data set.

The ON condition on this circuit is presented to indicate that —

a) the local data communication equipment is connected to a communication channel ("OFF HOOK" in switched service),

AND b) the local data communication equipment is not in test (local or remote), talk (alternate voice) or dial* mode, (See section 6.10).

AND c) the local data communication equipment has completed, where applicable

1. any timing functions required by the switching system to complete call establishment, and

2. the transmission of any discreet answer tone, the duration of which is controlled solely by the local data set.

* The data communication equipment is considered to be in the dial mode when circuitry directly associated with the call origination function is connected to the communication channel. These functions include signalling to the central office (dialling) and monitoring the communication channel for call progress or answer back signals.
Where the local data communication equipment does not transmit an answer tone, or where the duration of the answer tone is controlled by some action of the remote data set, the ON condition is presented as soon as all the other above conditions (a, b, and c-1) are satisfied.

This circuit shall be used only to indicate the status of the local data set. The ON condition shall not be interpreted as either an indication that a communication channel has been established to a remote data station or the status of any remote station equipment.

The OFF condition shall appear at all other times and shall be an indication that the data terminal equipment is to disregard signals appearing on any other interchange circuit with the exception of Circuit CE (Ring Indicator). The OFF condition shall not impair the operation of Circuit CE or Circuit CD (Data Terminal Ready).

When the OFF condition occurs during the progress of a call before Circuit CD is turned OFF, the data terminal equipment shall interpret this as a lost or aborted connection and take action to terminate the call. Any subsequent ON condition on Circuit CC is to be considered a new call.

When the data set is used in conjunction with Automatic Calling Equipment, the OFF to ON transition of Circuit CC shall not be interpreted as an indication that the ACE has relinquished control of the communication channel to the data set. Indication of this is given on the appropriate lead in the ACE interface (see EIA Standard RS-366).

Note: Attention is called to the fact that if a data call is interrupted by alternate voice communication, Circuit CC will be in the OFF condition during the time that voice communication is in progress. The transmission or reception of the signals required to condition the communication channel or data communication equipment in response to the ON condition of interchange Circuit CA (Request to Send) of the transmitting data terminal equipment will take place after Circuit CC comes ON, but prior to the ON condition on Circuit CB (Clear to Send) or Circuit CF (Received Line Signal Detector).

Circuit CD — Data Terminal Ready (C.C.I.T.T. 108.2)
Direction: To data communication equipment

Signals on this circuit are used to control switching of the data communication equipment to the communication channel. The ON condition prepares the data communication equipment to be connected to the communication channel and maintains the connection established by external means (e.g., manual call origination, manual answering or automatic call origination).

When the station is equipped for automatic answering of received calls and is in the automatic answering mode, connection to the line occurs only in response to a combination of a ringing signal and the ON condition of Circuit CD (Data Terminal Ready); however, the data terminal equipment is normally permitted to present the ON condition on Circuit CD whenever it is ready to transmit or receive data, except as indicated below.

The OFF condition causes the data communication equipment to be removed from the communication channel following the completion of any “in process” transmission. See Circuit BA (Transmitted Data). The OFF condition shall not disable the operation of Circuit CE (Ring Indicator).
In switched network applications, when circuit CD is turned OFF, it shall not be turned ON again until Circuit CC (Data Set Ready) is turned OFF by the data communication equipment.

*Circuit CE* – Ring Indicator (C.C.I.T.T. 125)
Direction: FROM data communication equipment

The ON condition of this circuit indicates that a ringing signal is being received on the communication channel.

The ON condition shall appear approximately coincident with the ON segment of the ringing cycle (during rings) on the communication channel.

The OFF condition shall be maintained during the OFF segment of the ringing cycle (between "rings") and at all other times when ringing is not being received. The operation of this circuit shall not be disabled by the OFF condition on Circuit CD (Data Terminal Ready).

*Circuit CF* – Received Line Signal Detector (C.C.I.T.T. 109)
Direction: FROM data communication equipment

The ON condition on this circuit is presented when the data communication equipment is receiving a signal which meets its suitability criteria. These criteria are established by the data communication equipment manufacturer.

The OFF condition indicates that no signal is being received or that the received signal is unsuitable for demodulation.

The OFF condition of Circuit CF (Received Line Signal Detector) shall cause Circuit BB (Received Data) to be clamped to the Binary One (Marking) condition.

The indications on this circuit shall follow the actual onset or loss of signal by appropriate guard delays.

On half duplex channels, Circuit CF is held in the OFF condition whenever Circuit CA (Request to Send) is in the ON condition and for a brief interval of time following the ON to OFF transition of Circuit CA. (See Circuit BB.)

*Circuit CG* – Signal Quality Detector (C.C.I.T.T. 110)
Direction: FROM data communication equipment

Signals on this circuit are used to indicate whether or not there is a high probability of an error in the received data.

An ON condition is maintained whenever there is no reason to believe that an error has occurred.

An OFF condition indicates that there is a high probability of an error. It may, in some instances, be used to call automatically for the retransmission of the previously transmitted data signal. Preferably the response of this circuit shall be such as to permit identification of individual questionable signal elements on Circuit BB (Received Data).
Circuit CH – Data Signal Rate Selector (DTE Source) (C.C.I.T.T. 111)
Direction: TO data communication equipment

Signals on this circuit are used to select between the two data signalling rates in the case of dual rate synchronous data sets or the two ranges of data signalling rates in the case of dual range non-synchronous data sets.

An ON condition shall select the higher data signalling rate or range of rates.

The rate of timing signals, if included in the interface, shall be controlled by this circuit as may be appropriate.

Circuit CI – Data Signal Rate Selector (DCE Source) (C.C.I.T.T. 112)
Direction: FROM data communication equipment

Signals on this circuit are used to select between the two data signalling rates in the case of dual rate synchronous data sets or the two ranges of data signalling rates in the case of dual range non-synchronous data sets.

An ON condition shall select the higher data signalling rate or range of rates.

The rate of timing signals, if included in the interface, shall be controlled by this circuit as may be appropriate.

Circuit DA – Transmitter Signal Element Timing (DTE Source) (C.C.I.T.T. 113)
Direction: TO data communication equipment

Signals on this circuit are used to provide the transmitting signal converter with signal element timing information.

The ON to OFF transition shall nominally indicate the center of each signal element on Circuit BA (Transmitted Data). When Circuit DA is implemented in the DTE, the DTE shall normally provide timing information on this circuit whenever the DTE is in a POWER ON condition. It is permissible for the DTE to withhold timing information on this circuit for short periods provided Circuit CA (Request to Send) is in the OFF condition. (For example, the temporary withholding of timing information may be necessary in performing maintenance tests within the DTE.)

Circuit DB – Transmitter Signal Element Timing (DCE Source) (C.C.I.T.T. 114)
Direction: FROM data communication equipment

Signals on this circuit are used to provide the data terminal equipment with signal element timing information. The data terminal equipment shall provide a data signal on Circuit BA (Transmitted Data) in which the transitions between signal elements nominally occur at the time of the transitions from OFF to ON condition of the signal on Circuit DB. When Circuit DB is implemented in the DCE, the DCE shall normally provide timing information on this circuit whenever the DCE is in a POWER ON condition. It is permissible for the DCE to withhold timing information on this circuit for short periods provided Circuit CC (Data Set Ready) is in the OFF condition. (For example, the withholding of timing information may be necessary in performing maintenance tests within the DCE.)
**Circuit DD** — Receiver Signal Element Timing (DCE Source) (C.C.I.T.T. 115)

**Direction:** FROM data communication equipment.

Signals on this circuit are used to provide the data terminal equipment with received signal element timing information. The transition from ON to OFF condition shall nominally indicate the center of each signal element on Circuit BB (Received Data). Timing information on Circuit DD shall be provided at all times when Circuit CF (Received Line Signal Detector) is in the ON condition. It may, but need not be present following the ON to OFF transition of Circuit CF (See section 4.3.2).

**Circuit SBA** — Secondary Transmitted Data (C.C.I.T.T. 118)

**Direction:** TO data communication equipment

This circuit is equivalent to Circuit BA (Transmitted Data) except that it is used to transmit data via the secondary channel.

Signals on this circuit are generated by the data terminal equipment and are connected to the local secondary channel transmitting signal converter for transmission of data to remote data terminal equipment.

The data terminal equipment shall hold Circuit SBA (Secondary Transmitted Data) in marking condition during intervals between characters or words and at all times when no data are being transmitted.

In all systems, the data terminal equipment shall not transmit data on the secondary channel unless an ON condition is present on all of the following four circuits, where implemented:

1. Circuit SCA — Secondary Request to Send
2. Circuit SCB — Secondary Clear to Send
3. Circuit CC — Data Set Ready
4. Circuit CD — Data Terminal Ready

All data signals that are transmitted across the interface on interchange Circuit SBA during the time when the above conditions are satisfied shall be transmitted to the communication channel. See Section 4.3.

When the secondary channel is useable only for circuit assurance or to interrupt the flow of data in the primary channel (less than 10 Baud capability), Circuit SBA (Secondary Transmitted Data) is normally not provided, and the channel carrier is turned ON or OFF by means of Circuit SCA (Secondary Request to Send). Carrier OFF is interpreted as an “Interrupt” condition.

**Circuit SBB** — Secondary Received Data (C.C.I.T.T. 119)

**Direction:** FROM data communication equipment

This circuit is equivalent to Circuit BB (Received Data) except that it is used to receive data on the secondary channel.
When the secondary channel is usable only for circuit assurance or to interrupt the flow of data in the primary channel, Circuit SBB is normally not provided. See interchange Circuit SCF (Secondary Received Line Signal Detector).

**Circuit SCA** — Secondary Request to Send (C.C.I.T.T. 120)
**Direction:** TO data communication equipment

This circuit is equivalent to Circuit CA (Request to Send) except that it requests the establishment of the secondary channel instead of requesting the establishment of the primary data channel.

Where the secondary channel is used as a backward channel, the ON condition of Circuit CA (Request to Send) shall disable Circuit SCA and it shall not be possible to condition the secondary channel transmitting signal converter to transmit during any time interval when the primary channel transmitting signal converter is so conditioned. Where system considerations dictate that one or the other of the two channels be in transmit mode at all times but never both simultaneously, this can be accomplished by permanently applying an ON condition to Circuit SCA (Secondary Request to Send) and controlling both the primary and secondary channels, in complementary fashion, by means of Circuit CA (Request to Send). Alternatively, in this case, Circuit SCB need not be implemented in the interface.

When the secondary channel is usable only for circuit assurance or to interrupt the flow of data in the primary data channel, Circuit SCA shall serve to turn ON the secondary channel unmodulated carrier. The OFF condition of Circuit SCA shall turn OFF the secondary channel carrier and thereby signal an interrupt condition at the remote end of the communication channel.

**Circuit SCB** — Secondary Clear to Send (C.C.I.T.T. 121)
**Direction:** FROM data communication equipment

This circuit is equivalent to Circuit CB (Clear to Send), except that it indicates the availability of the secondary channel instead of indicating the availability of the primary channel. This circuit is not provided where the secondary channel is usable only as a circuit assurance or an interrupt channel.

**Circuit SCF** — Secondary Received Line Signal Detector (C.C.I.T.T. 122)
**Direction:** FROM data communication equipment

This circuit is equivalent to Circuit CF (Received Line Signal Detector) except that it indicates the proper reception of the secondary channel line signal instead of indicating the proper reception of a primary channel received line signal.

Where the secondary channel is usable only as a circuit assurance or an interrupt channel (see Circuit SCA — Secondary Request to Send), Circuit SCF shall be used to indicate the circuit assurance status or to signal the interrupt. The ON condition shall indicate circuit assurance or a non-interrupt condition. The OFF condition shall indicate circuit failure (no assurance) or the interrupt condition.
SECTION FIVE

5. STANDARD INTERFACES FOR SELECTED COMMUNICATION SYSTEM CONFIGURATIONS

5.1 This section describes a selected set of data transmission configurations. For each of these configurations a standard set of interchange circuits (defined in section 4) is listed. (See section 6.2.)

5.1.1 Provision is made for additional data transmission configurations not defined herein. Interchange circuits for these applications must be specified separately, for each application, by the supplier.

5.2 Driven shall be provided for every interchange circuit included in the standard interface. Terminators need not be provided for every interchange circuit included in the standard interface; however, the designer of the equipment which does not provide all of the specified terminators must be aware that any degradation in service due to his disregard of a standard interchange circuit is his responsibility.

In the interest of minimizing the number of different types of equipment, additional interchange circuits may be included in the design of a general unit capable of satisfying the requirements of several different applications.

5.2.1 For a given configuration, interchange circuits which are included in the standard list and for which drivers are provided, but which the manufacturer of equipment at the receiving side of the interface chooses not to use, shall be suitably terminated by means of a dummy load impedance in the equipment which normally provides the terminator. See Section 2.4.

5.2.2 Where interchange circuits not on the standard list are provided for a given configuration, the designer of this equipment must be prepared to find an open circuit on the other side of the interface, and the system shall not suffer degradation of the basic service.

Interference due to unterminated drivers in this category is the responsibility of the designer who includes these drivers.

Terminators shall not interfere with or degrade system performance as a result of open circuited input terminals.

5.3 Circuit configurations for which standard sets of interchange circuits are defined are listed in Figure 5.1.

5.4 The use of Circuit AA (Protective Ground) is optional. Where it is used, attention is called to the applicable Underwriters' regulation applying to wire size and color coding. Where it is not used, other provisions for grounding equipment frames should be made in accordance with good engineering practice.

5.5 The use of Circuit AB (Signal Ground) is mandatory in all systems. See section 1.4.
5.6 Secondary channels, where involved in the standard interfaces, are shown as Auxiliary Channels.

5.6.1 Where secondary channels are intended for use as backward channels, Circuit SCA (Secondary Request to Send) shall be interconnected with Circuit CA (Request to Send) within the data communication equipment and need not be brought out to the interface. See Section 4.4, Interchange Circuit SCA (Secondary Request to Send) for detailed information.

5.6.2 Where secondary channels are usable only for circuit assurance or to interrupt the flow of data in the primary channel, they transmit no actual data and depend only on the presence or absence of the secondary channel carrier. For this application only, Circuit SBA (Secondary Transmitted Data), SBB (Secondary Received Data) and SCB (Secondary Clear to Send) are not provided. Circuit SCA (Secondary Request to Send) turns secondary channel carrier ON and OFF as required and Circuit SCF (Secondary Received Line Signal Detector) recognizes its presence or absence. See definitions of Circuits SCA and SCF in Section 4.4 for details.
<table>
<thead>
<tr>
<th>Data Transmission Configuration</th>
<th>Interface Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmit Only</td>
<td>A</td>
</tr>
<tr>
<td>Transmit Only*</td>
<td>B</td>
</tr>
<tr>
<td>Receive Only</td>
<td>C</td>
</tr>
<tr>
<td>Half Duplex</td>
<td>D</td>
</tr>
<tr>
<td>Duplex</td>
<td>D</td>
</tr>
<tr>
<td>Primary Channel Transmit Only / Secondary Channel Receive Only</td>
<td>E</td>
</tr>
<tr>
<td>Primary Channel Transmit Only / Secondary Channel Receive Only</td>
<td>F</td>
</tr>
<tr>
<td>Primary Channel Receive Only / Secondary Channel Transmit Only*</td>
<td>G</td>
</tr>
<tr>
<td>Primary Channel Receive Only / Secondary Channel Transmit Only</td>
<td>H</td>
</tr>
<tr>
<td>Primary Channel Transmit Only / Half Duplex Secondary Channel</td>
<td>I</td>
</tr>
<tr>
<td>Primary Channel Receive Only / Half Duplex Secondary Channel</td>
<td>J</td>
</tr>
<tr>
<td>Half Duplex Primary Channel / Half Duplex Secondary Channel</td>
<td>K</td>
</tr>
<tr>
<td>Duplex Primary Channel* / Duplex Secondary Channel*</td>
<td>L</td>
</tr>
<tr>
<td>Duplex Primary Channel / Duplex Secondary Channel</td>
<td>M</td>
</tr>
<tr>
<td>Special (Circuits specified by Supplier)</td>
<td>Z</td>
</tr>
</tbody>
</table>

*Note:* Data Transmission Configurations identified with an asterisk (*) indicate the inclusion of Circuit CA (Request to Send) in a One Way Only (Transmit) or Duplex Configuration where it might ordinarily not be expected, but where it might be used to indicate a non-transmit mode to the data communication equipment to permit it to remove a line signal or to send synchronizing or training signals as required.

**Figure 5.1**

*Interface Types for Data Transmission Configurations*
<table>
<thead>
<tr>
<th>Interchange Circuit</th>
<th>Interface Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>AA</td>
<td>A  B  C  D  E  F  G  H  I  J  K  L  M  Z</td>
</tr>
<tr>
<td>AB</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>BA</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>BB</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>CA</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>CB</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>CC</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>CD</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>CE</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>CF</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>CG</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>CH/CI</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>DA/DB</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>DD</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>SBA</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>SBB</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>SCA</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>SCB</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
<tr>
<td>SCF</td>
<td>X  X  X  X  X  X  X  X  X  X  X  X  X  X</td>
</tr>
</tbody>
</table>

Legend:
- * - To be specified by the supplier
- ** - optional
- s - Additional Interchange Circuits required for Switched Service
- t - Additional Interchange Circuits required for Synchronous Channel
- x - Basic Interchange Circuits, All Systems

Figure 5.2

Standard Interfaces For
Selected Communication Systems Configurations
SECTION SIX

6. RECOMMENDATIONS AND EXPLANATORY NOTES

6.1 The data are to be serialized by the data terminal equipment so that the design of the data communication equipment may be independent of the character length and code used by the data terminal equipment. The data communication equipment shall place no restrictions on the arrangement of the sequence of bits provided by the data terminal equipment.

6.2 The control interchange circuits at the interface point are arranged to permit the alternate use of a higher class of communication service as follows:

A. Data terminal equipment designed for Transmit-Only or Receive-Only service may also use either Half-duplex or Duplex service.

B. Data terminal equipment designed for Half-duplex service may also use Duplex service.

6.3 The electrical specifications are intended to provide a two-volt margin in rejecting noise introduced either on interchange circuits or by a difference in reference ground potential across the interface. The equipment designer should maintain this margin of safety on all interchange circuitry.

6.4 To avoid inducing voltage surges on interchange circuits, signals from interchange circuits should not be used to drive inductive devices, such as relay coils. (Note that relay or switch contacts may be used to generate signals on an interchange circuit, with appropriate measures to assure that signals so generated comply with Section 2.7.)

6.5 Alphabetical parenthetical designations are added to the terms used in Sections 2.3, 2.4, and 2.6 to better tie them in with the equivalent circuit of Section 2.1 and stress the point that the 2500 picofarad capacitance \( C_L \) is defined for the receiving end of the interchange circuit and that the capacitance \( C_D \) at the driving end of the interchange circuit, including cable, is not defined. It is the responsibility of the designer to build a circuit capable of driving all of the capacitance in the driver circuitry plus the capacitance in his part of the interconnecting cable (not specified) plus 2500 pF in the load (including the cable on the load side of the interface point).

6.6 The user is reminded that the characteristics of an equivalent load (terminator) circuit used to test for compliance with each of the electrical specifications in section 2 are a function not only of the parameter under test, but also of the tolerance limit to be tested. For example, a driver which just delivers a minimum of 5 Volts into a 7,000 Ohm test load may fail the test if the load is reduced to 3,000 Ohms, whereas, a driver with an output within the 15 Volt limit when driving a 3,000 Ohm load may exceed this limit when driving a 7,000 Ohm load. The 5 Volt tolerance should therefore be tested with a 3,000 Ohm load while the 15 Volt limit should be tested using a 7,000 Ohm load.

6.7 The operation of the transmitting and receiving circuits should minimize the effects of any circuit time constants which would delay the circuit response and introduce time distortion of the signals.
6.8 The turning ON of Circuit CA (Request to Send) does not necessarily imply the turning ON of a line signal on the communication channel. Some data sets might not have a line signal as it is understood in this standard, e.g. the signal can be a modified digital base-band signal.

Conversely, in data sets which do transmit a "line signal", the turning OFF of Circuit CA does not necessarily command the removal of that line signal from the communication channel. On a duplex channel, the data set might autonomously transmit a training signal to hold AGC circuits or automatic equalizers in adjustment, or to keep timing locked (synchronized) when Circuit CA is OFF.

It is not within the scope of this standard to specify in detail what occurs on the communication channel (line) side of the data communication equipment. Therefore the definition for Circuit CA uses the terminology "assume the transmit mode" intentionally avoiding reference to "carrier" or "line signals".

However, the continued requirement for multipoint systems is recognized. Data sets intended for this type of operation should permit the sharing of a communication channel by more than one data set transmitter and should, when in a non-transmit mode, place no signal on the communication channel which might interfere with the transmission from another data set in the network.

6.9 It is important that, at an answering data station, Circuit CC (Data Set Ready) be turned ON independently of any "event" which might occur at the remote (calling) data station. This independence permits the use of the OFF to ON transition of Circuit CC to start an "abort timer" in the data terminal equipment. This timer would cause termination of an automatically answered call (by causing Circuit CD to be turned OFF) if other expected events such as Circuit CF ON or proper exchange of data do not occur in a predetermined time interval. Such independence is necessary to assure the starting of the abort timer when an automatically answered incoming call is the result of a wrong number reached from a regular (non data station) telephone instrument.

6.10 Although the method of operation for multi-line automatic calling equipment, RS-366 (when assigned) Interface Type V, has not yet been fully defined, it appears that a situation could arise during call origination where both the DCE and the ACE appear to be idle (at the interface) even though actively engaged in establishing a connection.

One possible solution to this problem requires that circuit CC be turned ON upon completion of dialing to provide continuity of signaling during call origination. When multiline automatic calling equipment is used, Circuit CC would thus turn ON earlier than specified in Section 4.4 herein. This solution is subject to further study; however, data terminal equipment which may, in the future, be used in systems with multi-line automatic calling equipment should not be adversely affected by this early "Data Set Ready" indication.
SECTION SEVEN

7. GLOSSARY OF NEW TERMS

7.1 This section defines terms used in this standard which are new or used in a special sense.

1. Data Transmission Channel

The transmission media and intervening equipment involved in the transfer of information between data terminal equipments. A data transmission channel includes the signal conversion equipment. A data transmission channel may support the transfer of information in one direction only, in either direction alternately, or in both directions simultaneously and the channel is accordingly classified as defined in the following sections. When the data communications equipment has more than one speed capability associated with it, for example 1200 baud transmission in one direction and 150 baud transmission in the opposite direction, a channel is defined for each speed capability.

2. Primary Channel

The data transmission channel having the highest signaling rate capability of all the channels sharing a common interface connector. A primary channel may support the transfer of information in one direction only, either direction alternately or both directions simultaneously and is then classified as "one way only", "half duplex" or "duplex" as defined herein.

3. Secondary Channel

The data transmission channel having a lower signaling rate capability than the primary channel in a system in which two channels share a common interface connector. A secondary channel may be either one way only, half duplex or duplex as defined later. Two classes of secondary channels are defined, auxiliary and backward.

4. Auxiliary Channel

A secondary channel whose direction of transmission is independent of the primary channel and is controlled by an appropriate set of secondary control interchange circuits.

5. Backward Channel

A secondary channel whose direction of transmission is constrained to be always opposite to that of the primary channel. The direction of transmission of the backward channel is restricted by the control interchange circuit (Circuit CA - Request to Send) that controls the direction of transmission of the primary channel.

6. One Way Only (Unidirectional) Channel

A primary or secondary channel capable of operation in only one direction. The direction is fixed and cannot be reversed. The term "one way only" used to describe a primary channel.
does not imply anything about the type of secondary channel or the existence of a secondary channel; similarly, the use of the term to describe a secondary channel implies nothing about the type of primary channel present.

7. Half Duplex Channel

A primary or secondary channel capable of operating in both directions but not simultaneously. The direction of transmission is reversible. The term half duplex used to describe a primary channel does not imply anything about the type of secondary channel; similarly, the use of the term to describe a secondary channel implies nothing about the type of primary channel present. (Note that as a result of the definitions, both directions of a half duplex channel have the same signaling rate capability.)

8. Duplex Channel (Full Duplex Channel)

A primary or secondary channel capable of operating in both directions simultaneously. The term duplex used to describe a primary channel does not imply anything about the type of secondary channel or the existence of a secondary channel; similarly, the use of the term to describe a secondary implies nothing about the type of primary channel present. (Note that a full duplex channel has the same signaling rate capability in both directions. A system with different rates would be considered to be a one way only primary channel in one direction and a one way only secondary channel in the opposite direction.)

9. Synchronous Data Transmission Channel

A data channel in which timing information is transferred between the data terminal equipment and the data communication equipment. Transmitter Signal Element Timing signals can be provided by either the data terminal equipment or by the data communication equipment. Receiver Signal Element Timing is normally recovered in and provided by the Data Communication Equipment. A synchronous data channel will not accommodate Start/Stop data signals unless they are transmitted isochronously and timing signals are interchanged at least at the transmitting station.

10. Nonsynchronous Data Transmission Channel

A data channel in which no timing information is transferred between the data terminal equipment and the data communication equipment.

11. Dedicated Line

A communications channel which is nonswitched, i.e., which is permanently connected between two or more data stations. These communication channels are also referred to as "leased" or "private"; however, since leased and private switched networks do exist, the term "dedicated" is preferred herein to define a nonswitched connection between two or more stations.
12. Interchange Circuit

A circuit between the data terminal equipment and the data communication equipment for the purpose of exchanging data, control or timing signals. Circuit A,B (signal ground) is a common reference for all interchange circuits.

13. Driver

a. The electronic circuitry or relay contact at the transmitting end (source) of an interchange circuit which transmits binary digital signals to a terminator via an interconnecting cable.

b. The transmitter of a binary digital signal.

14. Terminator

a. The electronic circuitry at the receiving end (sink) of an interchange circuit which receives binary digital signals from a driver via an interconnecting cable.

b. The receiver of a binary digital signal.

15. Signal Conversion Equipment

Those portions of the data communication equipment which transform (e.g., modulate, shape, etc.) the data signals exchanged across the interface into signals suitable for transmission through the associated communication media or which transform (e.g., demodulate, slice, regenerate, etc.) the received line signals into data signals suitable for presentation to the data terminal equipment.
APPENDIX I

INTERFACE CONNECTOR

While no industry standard exists which defines a suitable interface connector, it should be noted that commercial products are available which will perform satisfactorily as electrical connectors for interfaces specified in RS-232C, such as those connectors meeting Military Specification MIL-C-24308 (MS-18275) or equivalent.

It is not intended that the above reference be considered as part of RS-232C or as a standard for the devices to which reference is made.
Appendix B

Figures
Figure 1. A Two Terminal Network.
<table>
<thead>
<tr>
<th>DTE</th>
<th>DCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Protective Ground</td>
<td>Protective Ground</td>
</tr>
<tr>
<td>Ground (Ground)</td>
<td>Ground (Ground)</td>
</tr>
<tr>
<td>Data</td>
<td>Signal Ground (Data)</td>
</tr>
<tr>
<td>Received Data</td>
<td>Received Data (Data)</td>
</tr>
<tr>
<td>Secondary Received Data</td>
<td>Secondary Received Data (Data)</td>
</tr>
<tr>
<td>Transmitted Data</td>
<td>Transmitted Data (Data)</td>
</tr>
<tr>
<td>Secondary Transmitted Data</td>
<td>Secondary Transmitted Data (Data)</td>
</tr>
<tr>
<td>Clear to Send</td>
<td>Clear to Send (Control)</td>
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<tr>
<td>Secondary Clear to Send</td>
<td>Secondary Clear to Send (Control)</td>
</tr>
<tr>
<td>Request to Send</td>
<td>Request to Send (Control)</td>
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<td>Secondary Request to Send</td>
<td>Secondary Request to Send (Control)</td>
</tr>
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<td>Data Set Ready</td>
<td>Data Set Ready (Control)</td>
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<tr>
<td>Data Terminal Ready</td>
<td>Data Terminal Ready (Control)</td>
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<tr>
<td>Signal Quality Detector</td>
<td>Signal Quality Detector (Control)</td>
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<tr>
<td>Ring Indicator</td>
<td>Ring Indicator (Control)</td>
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<td>Received Line Signal Detector</td>
<td>Received Line Signal Detector (Control)</td>
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<td>Secondary Received Line Signal Detector</td>
<td>Secondary Received Line Signal Detector (Control)</td>
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<td>Data Signal Rate Selector</td>
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<td>Secondary Data Signal Rate Selector</td>
<td>Data Signal Rate Selector DCE (Control)</td>
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<td>Transmitter Signal Element Timing DCE</td>
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<td>Receiver Signal Element Timing</td>
<td>Receiver Signal Element Timing (Control)</td>
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<td>Transmitter Signal Element Timing DTE</td>
<td>Transmitter Signal Element Timing DTE (Control)</td>
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<td>Reserved for Data Set Testing</td>
<td>Reserved for Data Set Testing</td>
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<td>Reserved for Data Set Testing</td>
<td>Reserved for Data Set Testing</td>
</tr>
<tr>
<td>Unassigned</td>
<td>Unassigned</td>
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</tbody>
</table>

Figure 2. The Full RS-232-C Connection Diagram.
Figure 3. The Full RS-232-C Interchange Circuit Configuration.
Figure 4. Block Diagram of the $\mu$SAN $\langle$Interchange_Circuit$\rangle$.
Figure 5. Refinement of the $\mu$SAN (Interchange_Circuit).
Figure 6. Diagram of the $\mu$SAN (Electrical Model).
When $v_o^{(0)} = 0V$,

![Diagram showing the RS-232-C Rule Governing the Source Impedance of the $\mu$SAN (Electrical Model).]

**Statement:** The power off source impedance ($R_o$) of the driver side shall not be less than 300 ohms.

**Comment:** The applied voltage ($e_l^{(0)}$) is not greater than 2V magnitude and $v_o^{(0)}$ is 0V.


**Mathematical Representation:**

$$((-2V \leq e_l^{(0)} \leq 2V) \text{ and } (v_o^{(0)} = 0V) \Rightarrow R_o \geq 300 \Omega) ;$$

$$((e_l^{(0)} < -2V) \text{ or } (2V < e_l^{(0)})) \text{ and } (v_o^{(0)} = 0V) \Rightarrow R_o \geq 0 \Omega$$

Figure 7. The RS-232-C Rule Governing the Source Impedance of the $\mu$SAN $\langle$Electrical_Model$\rangle$. 
Statement: The dc resistance ($R_L$) at the terminator will not be less than 3000 ohms.

Comment: The applied voltage ($v_O^{(0)}$) has a magnitude not greater than 25V.


Mathematical Representation:

$$R_L \geq 3000 \, \Omega, \forall v_O^{(0)}, \exists. \ |v_O^{(0)}| \leq 25V;$$

$$R_L \geq 0 \, \Omega, \forall v_O^{(0)}, \exists. \ |v_O^{(0)}| > 25V;$$

Figure 8. The RS-232-C Rule Governing the Minimum Load Resistance of the $\mu$SAN (Electrical Model).
Statement: The dc resistance \((R_L)\) at the terminator shall not be more than 7000 ohms.

Comment: The applied voltage \((v_o^{(0)})\) has a magnitude of 3V to 25V.


Mathematical Representation:

\[
0 \Omega \leq R_L \leq 7000 \Omega, \ \forall \ v_o^{(0)} . \exists. \ 3V \leq |v_o^{(0)}| \leq 25V ;
\]

\[
0 \Omega \leq R_L, \ \forall \ v_o^{(0)} . \exists. \ |v_o^{(0)}| < 3V ;
\]

\[
0 \Omega \leq R_L, \ \forall \ v_o^{(0)} . \exists. \ |v_o^{(0)}| > 25V
\]

Figure 9. The RS-232-C Rule Governing the Maximum Load Resistance of the \(\mu\)SAN \(\langle\text{Electrical Model}\rangle\).
Statement: The shunt capacitance \( (c_l) \) in the terminator side of the interchange circuit shall not exceed 2500 pf.

Comment: Applies at all times.


Mathematical Representation:

\[
0 \, \text{pf} \leq c_l \leq 2500 \, \text{pf} \equiv c_l \in [0, 2500]
\]

Figure 10. The RS-232-C Rule Governing the Load Capacitance of the μSAN \( \langle \text{Electrical Model} \rangle \).
Statement: The open circuit terminator voltage ($e^{(0)}_L$) shall not exceed 2 volts in magnitude.

Comment: Applies at all times.


Mathematical Representation:

\[-2 \text{ V} \leq e^{(0)}_L \leq 2 \text{ V} = e^{(0)}_L \in [-2, 2]\]

Figure 11. The RS-232-C Rule Governing the Load Voltage of the $\mu$SAN (Electrical_Model).
$$P_{\text{Electrical\_Model\_Set}}(v_{\text{Ospec}}) =$$

\[
\{ (R_0, C_0, R_L, C_L, E_L) \mid \\
R_0 \in [300, \infty) \quad \text{and} \\
C_0 + C_L \in [0, 2500] \quad \text{and} \\
R_L \in [3000, 7000] \quad \text{if} \quad |v_{\text{Ospec}}| \in [3, 25] \quad \text{and} \\
R_L \in [3000, \infty) \quad \text{if} \quad |v_{\text{Ospec}}| \in [0, 3] \quad \text{and} \\
R_L \in [0, \infty) \quad \text{if} \quad |v_{\text{Ospec}}| \in (25, \infty) \quad \text{and} \\
E_L \in [-2, 2] \} \]

Figure 12. The Set of All Possible Parameter Arrays for \langle \text{Electrical\_Model} \rangle.
Figure 13. The Reduced $\mu$SAN (Electrical_Model) for Electrical Analysis.
Statement: The open circuit driver voltage ($v_D^{(m)}$) with respect to signal ground shall not exceed 25 volts in magnitude.

Comment: Applies at all times.


Mathematical Representation:

$$-25V \leq v_D^{(m)} \leq 25V \equiv v_D^{(m)} \in [-25, 25]$$

Figure 14. The RS-232-C Rule Governing the Driver Voltage of the $\mu$SAN (Electrical Model).
Statement: The maximum instantaneous rate of voltage change \( v^{(i)}_{\text{driver}} \) shall not exceed 30 volts per microsecond.

Comment: Applies at all times.


Mathematical Representation:

\[-30 \text{V/\mu s} \leq v^{(i)}_{\text{driver}} \leq 30 \text{V/\mu s} \equiv v^{(i)}_{\text{driver}} \in [-30, 30] \]

Figure 15. The RS-232-C Rule Governing the Slope of the Driver Interface Voltage of the \( \mu\text{SAN \langle Electrical\_Model\rangle} \).
Statement: The maximum instantaneous rate of voltage change \( v_{\text{sensor}}^{(t)} \) shall not exceed 30 volts per microsecond.

Comment: Applies at all times.


Mathematical Representation:

\[-30 \text{ V/\mu s} \leq v_{\text{sensor}}^{(t)} \leq 30 \text{ V/\mu s} = v_{\text{sensor}}^{(t)} \in [-30, 30]\]

Figure 16. The RS-232-C Rule Governing the Slope of the Sensor Interface Voltage of the \( \mu \text{SAN (Electrical Model)} \).
Statement: The signal shall be considered in the sensor marking condition when the voltage \( v_{\text{sensor}}^{(0)} \) is more negative than -3V.

Comment: Applies to data interchange circuits.


Mathematical Representation:

Sensor Marking Condition 

\[
\{ v_{\text{sensor}}^{(0)} \leq -3 \} = ( -\infty, -3 )
\]

Figure 17. Definition of an RS-232-C Marking Signal Condition for Sensor Interface Voltage Values.
Statement: The signal shall be considered sensor OFF when the voltage $v_{x_{\text{sensor}}}^{(0)}$ is more negative than -3V.

Comment: Applies to control and timing interchange circuits.


Mathematical Representation:

Sensor OFF \[ \Delta \]

\[ \{ v_{x_{\text{sensor}}} < -3 \text{V} \} = ( -\infty, -3 ) \]
Statement: The signal shall be considered in the sensor spacing condition when the voltage \( v_{x_{\text{sensor}}}^{(0)} \) is more positive than 3V.

Comment: Applies to data interchange circuits.


Mathematical Representation

Sensor Spacing Condition

\[ \{ v_{x_{\text{sensor}}}^{(0)} \geq 3V \} = (3, \infty) \]

---

Figure 19. Definition of an RS-232-C Spacing Signal Condition for Sensor Interface Voltage Values.
Statement: The signal shall be considered sensor ON when the voltage \( v_{X_{\text{sensor}}}^{(0)} \) is more positive than 3V.

Comment: Applies to control and timing interchange circuits.


Mathematical Representation:

\[
\text{Sensor ON } \triangleq \{ v_{X_{\text{sensor}}}^{(0)} > 3V \} = (3, \infty)
\]

Figure 20. Definition of an RS-232-C ON Signal Condition for Sensor Interface Voltage Values.
Statement: The signal shall be considered in the sensor transition region when the voltage \( v_{\text{sensor}}^{(i)} \) is between -3V and 3V.

Comment: Applies to data, control, and timing interchange circuits.


Mathematical Representation:

\[
\text{Sensor Transition Region } \triangleq \left\{ v_{\text{sensor}}^{(i)} : -3V < v_{\text{sensor}}^{(i)} < 3V \right\} = (-3, 3)
\]

Figure 21. The RS-232-C Definition of the Sensor Interface Voltage Transition Region.
Statement: The signal shall be considered in the driver marking condition when the voltage \( v_{\text{driver}}^{(0)} \) is more negative than -5V.

Comment: Applies to data interchange circuits.


Mathematical Representation:

\[
\text{Driver Marking Condition } \triangleq \\
\{ v_{\text{driver}}^{(0)} \in \mathbb{R} \mid v_{\text{driver}}^{(0)} < -5V \} = (-\infty, -5)
\]

Figure 22. Definition of an RS-232-C Marking Signal Condition for Driver Interface Voltage Values.
Statement: The signal shall be considered driver OFF when the voltage \( (V_{\text{Off}}) \) is more negative than -5V.

Comment: Applies to control and timing interchange circuits.


Mathematical Representation:

Driver OFF

\[
\{ v_{\text{driver}} \leq -5V \} = (-\infty, -5]
\]

Figure 23. Definition of an RS-232-C OFF Signal Condition for Driver Interface Voltage Values.
Statement: The signal shall be considered in the driver spacing condition when the voltage \(v_{X_{driver}}^{(0)}\) is more positive than 5V.

Comment: Applies to data interchange circuits.


Mathematical Representation:

\[
\text{Driver Spacing Condition} \triangleq \left\{ v_{X_{driver}}^{(0)} \geq 5V \right\} = (5, \infty)
\]
Statement: The signal shall be considered driver ON when the voltage \( v_{x_{\text{driver}}}^{(0)} \) is more positive than 5V.

Comment: Applies to control and timing interchange circuits.


Mathematical Representation:

\[
\text{Driver ON} \triangleq \left( v_{x_{\text{driver}}}^{(0)} \geq 5V \right) = (5, \infty)
\]

Figure 25. Definition of an RS-232-C ON Signal Condition for Driver Interface Voltage Values.
Statement: The signal shall be considered in the driver transition region when the voltage \(v_{\text{Xdriver}}^{(0)}\) is between -5V and 5V.

Comment: Applies to data, control, and timing interchange circuits.


Mathematical Representation:

\[
\{ v_{\text{Xsensor}} \in R \mid -5V < v_{\text{Xdriver}}^{(0)} < 5V \} = (-5, 5)
\]

Figure 26. The RS-232-C Definition of the Driver Interface Voltage Transition Region.
GT(t, T) \triangleq \\
Set of all times greater than t, given a set of times T = \\
\{ t'. \exists. t' > t \textbf{ and } t' \in T \}
\[ T_{\text{pential}} \triangleq \text{Set of all positive driver enter times of } v_{X\text{driver}}^* = \]
\[
\{ t \in \mathbb{R} \mid v_{X\text{driver}}^*(t) = -5V \text{ and } \exists \delta > 0 \land \forall t', (t-\delta < t' < t, \quad v_{X\text{driver}}^*(t') < -5V) \}
\]

\[ T_{\text{pexit}} \triangleq \text{Set of all positive driver exit times of } v_{X\text{driver}}^* = \]
\[
\{ t \in \mathbb{R} \mid v_{X\text{driver}}^*(t) = 5V \text{ and } \exists \delta > 0 \land \forall t', (t < t' < t+\delta, \quad v_{X\text{driver}}^*(t') > 5V) \}
\]

Figure 28. The Definition of the Set of RS-232-C Positive Driver Enter and Exit Times for \( v_{X\text{driver}}^* \).
\[ T_{\text{enter}} \triangleq \text{Set of all positive sensor enter times of } v_{X_{\text{sensor}}} \cdot = \{ t \in \mathbb{R} : v_{X_{\text{sensor}}}^{(0)}(t) = -3V \text{ and } \exists \delta > 0 . \ \forall t', \ t - \delta < t' < t, \ v_{X_{\text{sensor}}}^{(0)}(t') < -3V \} \]

\[ T_{\text{exit}} \triangleq \text{Set of all positive sensor exit times of } v_{X_{\text{sensor}}} \cdot = \{ t \in \mathbb{R} : v_{X_{\text{sensor}}}^{(0)}(t) = 3V \text{ and } \exists \delta > 0 . \ \forall t', \ t < t' < t + \delta, \ v_{X_{\text{sensor}}}^{(0)}(t') > 3V \} \]

Figure 29. The Definition of the Set of RS-232-C Positive Sensor Enter and Exit Times for \( v_{X_{\text{sensor}}} \cdot \).
\[ [t_{\text{p enter}}, t_{\text{p exit}}] \text{ is a positive driver transition domain of } v_{X\text{driver}} \]

iff \( t_{\text{p enter}} \in T_{\text{p enter}} \) and

\[ t_{\text{p exit}} = \text{MIN}(GT(t_{\text{p enter}}, T_{\text{p exit}})) \text{ and } \]

\( \forall t \in [t_{\text{p enter}}, t_{\text{p exit}}], \)

\(-5V \leq v_{X\text{driver}}(t) \leq 5V \)

Figure 30. The Definition an RS-232-C Positive Driver Transition Domain for \( v_{X\text{driver}} \).
\([t_{\text{penter}}, t_{\text{pexit}}]\) is a positive sensor transition domain of \(v_{X_{\text{sensor}}}\).

\[
\text{iff } t_{\text{penter}} \in T_{\text{penter}} \text{ and } \\
 t_{\text{pexit}} = \min\{GT(t_{\text{penter}}, T_{\text{pexit}})\} \text{ and } \\
 \forall t \in [t_{\text{penter}}, t_{\text{pexit}}], \\
 -3V \leq v_{X_{\text{sensor}}}(t) \leq 3V
\]

Figure 31. The Definition an RS-232-C Positive Sensor Transition Domain for \(v_{X_{\text{sensor}}}\).
Figure 32. The Definition of the Set of RS-232-C Negative Driver Enter and Exit Times for $v_{X_{driver}}$. 
\[ T_{\text{nsenter}} \triangleq \text{Set of all negative sensor enter times of } v_{X_{\text{sensor}}} = \{ t : \exists v_{X_{\text{sensor}}}^{(0)}(t) = 3V \text{ and } \exists \delta > 0 \exists t', t-\delta < t' < t, v_{X_{\text{sensor}}}^{(0)}(t') > 3V \} \]

\[ T_{\text{nsexit}} \triangleq \text{Set of all negative sensor exit times of } v_{X_{\text{sensor}}} = \{ t : \exists v_{X_{\text{sensor}}}^{(0)}(t) = -3V \text{ and } \exists \delta > 0 \exists t', t < t' < t+\delta, v_{X_{\text{sensor}}}^{(0)}(t') < -3V \} \]

Figure 33. The Definition of the Set of RS-232-C Negative Sensor Enter and Exit Times for \( v_{X_{\text{sensor}}} \).
Figure 34. The Definition an RS-232-C Negative Driver Transition Domain for $v_{X\text{driver}}$. 

$[t_{\text{ndenter}}, t_{\text{ndexit}}]$ is a negative driver transition domain of $v_{X\text{driver}}$.

Iff $t_{\text{ndenter}} \in T_{\text{ndenter}}$ and

$t_{\text{ndexit}} = \text{MIN}[\text{GT}(t_{\text{ndenter}}, T_{\text{ndexit}})]$ and

$\forall t \in [t_{\text{ndenter}}, t_{\text{ndexit}}],$

$-5V \leq v^{(0)}_{X\text{driver}}(t) \leq 5V$
$[t_{\text{enter}}, t_{\text{exit}}]$ is a negative sensor transition domain of $v_{X_{\text{sensor}}}$ iff $t_{\text{enter}} \in T_{\text{enter}}$ and
$$t_{\text{exit}} = \text{MIN}[G(T(t_{\text{enter}}, T_{\text{exit}}))]$$ and
$$\forall t \in [t_{\text{enter}}, t_{\text{exit}}],$$
$$-3V \leq v_{X_{\text{sensor}}}(t) \leq 3V$$

Figure 35. The Definition an RS-232-C Negative Sensor Transition Domain for $v_{X_{\text{sensor}}}$.
Figure 36. The Definition of the Set of All RS-232-C Driver Transition Domains for $v_{X_{\text{driver}}}$.

$$T_{\text{transdomain}}(v_{X_{\text{driver}}}) \triangleq$$

Set of all driver transition domains of $v_{X_{\text{driver}}}$ =

$$\{ [t_{\text{init}}, t_{\text{final}}] \; : \; [t_{\text{init}}, t_{\text{final}}] \text{ is a positive driver transition domain}$$

or
$$[t_{\text{init}}, t_{\text{final}}] \text{ is a negative driver transition domain} \}$$
\[ T_{\text{tranadom}}(v_{\text{sensor}}) \triangleq \]

Set of all sensor transition domains of \( v_{\text{sensor}} \) =

\[ \{ [t_{\text{init}}, t_{\text{final}}] : \exists [t_{\text{init}}, t_{\text{final}}] \text{ is a positive sensor transition domain} \]

or

\[ [t_{\text{init}}, t_{\text{final}}] \text{ is a negative sensor transition domain} \}

Figure 37. The Definition of the Set of All RS-232-C Sensor Transition Domains for \( v_{\text{sensor}} \).
Let $x = [x^{(0)}, x^{(1)}, x^{(2)}, \ldots]$ be a simple germ,

$$\text{Dir}(x) \triangleq$$

+ (positive) \iff

$$\exists \ m \in \mathbb{N} \ . \ \exists \ . \ x^{(m)} > 0 \ \text{and}$$

$$\forall \ n = [1 \ldots m-1], \ x^{(n)} = 0;$$

- (negative) \iff

$$\exists \ m \in \mathbb{N} \ . \ \exists \ . \ x^{(m)} < 0 \ \text{and}$$

$$\forall \ n = [1 \ldots m-1], \ x^{(n)} = 0;$$

0 (zero) \iff

$$\forall \ m \in \mathbb{N},$$

$$x^{(m)} = 0$$

Figure 38. The Direction Operation Definition for a Germ.
Statement: The time required for the signal \( (v_{\text{driver}}) \) to pass through the transition region shall not exceed one millisecond.

Comment: For all control interchange circuits.


Mathematical Representation

Given \([t_{\text{init}}, t_{\text{final}}] \in T_{\text{transdomain}}(v_{\text{driver}}),\]

\[
\text{length}([t_{\text{init}}, t_{\text{final}}]) \leq 1 \text{ ms}
\]

Figure 39. The RS-232-C Driver Transition Domain Slew Rate Rule for Control Interchange Circuits.
Statement: The time required for the signal \( v_{\text{sensor}} \) to pass through the transition region shall not exceed one millisecond.

Comment: For all control interchange circuits.


Mathematical Representation

Given \([t_{\text{init}}, t_{\text{final}}] \in T_{\text{transdomain}}(v_{\text{sensor}})\),

\[ \text{length}([t_{\text{init}}, t_{\text{final}}]) \leq 1 \text{ ms} \]

Figure 40. The RS-232-C Sensor Transition Domain Slew Rate Rule for Control Interchange Circuits.
Statement: The time required for the signal \(v_{X_{\text{driver}}}\) to pass through the transition region shall not exceed one millisecond or 4% of the period \(T\) of a signal element, whichever is less.

Comment: For all data and timing interchange circuits.


Mathematical Representation

Given \([t_{\text{init}}, t_{\text{final}}] \in T_{\text{transdomain}}(v_{X_{\text{driver}}})\),

\[
\text{length}([t_{\text{init}}, t_{\text{final}}]) \leq \min(1 \text{ ms}, 0.04 T)
\]

Figure 41. The RS-232-C Driver Transition Domain Slew Rate Rule for Data and Timing Interchange Circuits.
Statement: The time required for the signal \((v_{X_{\text{sensor}}})\) to pass through the transition region shall not exceed one millisecond or 4% of the period \((T)\) of a signal element, whichever is less.

Comment: For all data and timing interchange circuits.


Mathematical Representation

Given \([t_{\text{init}}, t_{\text{final}}] \in T_{\text{transdomain}}(v_{X_{\text{sensor}}})\),

\[
\text{length}([t_{\text{init}}, t_{\text{final}}]) \leq \min(1\ \text{ms}, 0.04\ T)
\]

Figure 42. The RS-232-C Sensor Transition Domain Slew Rate Rule for Data and Timing Interchange Circuits.
Statement: There shall be no reversal of the direction of voltage change while the signal \( v_{X_{driver}} \) is in the transition region.

Comment: Applies when \( v_{X_{driver}} \) is in the transition region.


Mathematical Representation:

Given \([t_{init}, t_{final}] \in T_{transdomain}(v_{X_{driver}})\),

if \([t_{init}, t_{final}] \) is a positive driver transition domain

then \( \forall t \in [t_{init}, t_{final}], \text{Dir}(v_{X_{driver}}(t)) \in \{ +, 0 \} \);

if \([t_{init}, t_{final}] \) is a negative driver transition domain

then \( \forall t \in [t_{init}, t_{final}], \text{Dir}(v_{X_{driver}}(t)) \in \{ -, 0 \} \);

Figure 43. The RS-232-C Driver Transition Domain Direction Rule.
Statement: There shall be no reversal of the direction of voltage change while the signal \( v_{X_{\text{sensor}}} \) is in the transition region.

Comment: Applies when \( v_{X_{\text{sensor}}} \) is in the transition region.


Mathematical Representation:

Given \([t_{\text{init}}, t_{\text{final}}] \in T_{\text{stransdomain}}(v_{X_{\text{sensor}}})\),

if \([t_{\text{init}}, t_{\text{final}}]\) is a positive sensor transition domain

then \( \forall t \in [t_{\text{init}}, t_{\text{final}}], \text{Dir}(v_{X_{\text{sensor}}}(t)) \in (+, 0) \);

if \([t_{\text{init}}, t_{\text{final}}]\) is a negative sensor transition domain

then \( \forall t \in [t_{\text{init}}, t_{\text{final}}], \text{Dir}(v_{X_{\text{sensor}}}(t)) \in (-, 0) \);
The Set of All Preliminary Driver Interface Voltage Time Functions =

\[ V_{\text{XdepcStart}} \land ( V_{\text{XdepcLow}}^* \land V_{\text{XdepcPos}}^* \land V_{\text{XdepcHigh}}^* \land V_{\text{XdepcNeg}}^* ) \land V_{\text{XdepcEnd}}^* \]

\[ V_{\text{XdepcLow}}^* = \{(t \in (t_{\text{start}}, t_{\text{end}} + R^*); v_{\text{XdepcLow}}(t) \in v_{\text{XdepcLowinal}}) \}
\]

\[ \forall t \in (t_{\text{start}}, t_{\text{end}}),
V_{\text{XdepcLow}}^*(t) \in (-\infty, -5) \quad \text{and}
V_{\text{XdepcLow}}^*(t) \in [-30, 30] \quad \text{and}
V_{\text{XdepcLow}}^*(t_{\text{end}}) = V_{\text{XdepcLowinal}}(t_{\text{end}}) \quad \text{and}
V_{\text{XdepcLow}}^*(t_{\text{end}}) \in [-30, 30] \}
\]

\[ V_{\text{XdepcHigh}}^* = \{(t \in (t_{\text{start}}, t_{\text{end}} + R^*); v_{\text{XdepcHigh}}(t) \in v_{\text{XdepcHighinal}}) \}
\]

\[ \forall t \in (t_{\text{start}}, t_{\text{end}}),
V_{\text{XdepcHigh}}^*(t) \in (5, \infty) \quad \text{and}
V_{\text{XdepcHigh}}^*(t) \in [-30, 30] \quad \text{and}
V_{\text{XdepcHigh}}^*(t_{\text{end}}) = V_{\text{XdepcHighinal}}(t_{\text{end}}) \quad \text{and}
V_{\text{XdepcHigh}}^*(t_{\text{end}}) \in [-30, 30] \}
\]

Figure 45. The Set of Preliminary Driver Interface Voltage Time Functions (Part 1 of 2).
\[
V_{\text{XdpecPos}^*} = \{ (t \in (-, t_{\text{init}} + R^*]; V_{\text{XdpecPosinit}} \rightarrow V_{\text{XdpecPosfinal}}) \}
\]

\[
\forall t \in (t_{\text{init}}, t_{\text{final}}),
\begin{align*}
V_{\text{XdpecPosinit}}(t) &\in [-5, 5] \\
V_{\text{XdpecPosinit}}(t) &\in [0, 30] \\
V_{\text{XdpecPosinit}}(t_{\text{final}}) = V_{\text{XdpecPosfinal}}(t_{\text{final}}) \\
V_{\text{XdpecPosfinal}}(t_{\text{final}}) &\in [0, 30]
\end{align*}
\]

\[
V_{\text{XdpecNeg}^*} = \{ (t \in (-, t_{\text{init}} + R^*]; V_{\text{XdpecNeginit}} \rightarrow V_{\text{XdpecNegfinal}}) \}
\]

\[
\forall t \in (t_{\text{init}}, t_{\text{final}}),
\begin{align*}
V_{\text{XdpecNeginit}}(t) &\in [-5, 5] \\
V_{\text{XdpecNeginit}}(t) &\in [-30, 0] \\
V_{\text{XdpecNeginit}}(t_{\text{final}}) = V_{\text{XdpecNegfinal}}(t_{\text{final}}) \\
V_{\text{XdpecNegfinal}}(t_{\text{final}}) &\in [-30, 0]
\end{align*}
\]

\[
V_{\text{XdpecStart}} = \{ (V_{\text{XdpecPos}^*} \cup \lambda \cdot &\lor V_{\text{XdpecHigh}^*} \lor \lambda \cdot &\lor V_{\text{XdpecNeg}^*}) \cup \lambda \cdot\}
\]

\[
V_{\text{XdpecEnd}} = \{ \lambda \cdot \cup (V_{\text{XdpecLow}^*} \lor (\lambda \cdot \lor (V_{\text{XdpecPos}^*} \lor (\lambda \cdot \lor V_{\text{XdpecHigh}^*})))\})\)
\]

Figure 45. The Set of Preliminary Driver Interface Voltage Time Functions (Part 2 of 2).
$V_{X_{\text{spec}}}$: a The Set of All Valid Driver Interface Voltage Time Functions

$$= \{ v_{X_{\text{spec}}} \mid v_{X_{\text{spec}}} \in V_{Xd} \land \max(\text{length}(T_{\text{dranedomain}}(v_{X_{\text{spec}}^\cdot}))) \leq 1\, \text{ms} \land \text{for control interchange circuits} \land \max(\text{length}(T_{\text{dranedomain}}(v_{X_{\text{spec}}^\cdot}))) \leq \min[1\, \text{ms}, 0.04T] \land \text{for data and timing interchange circuits} \}$$

Figure 46. The Set of Valid Driver Interface Voltage Time Functions.
Figure 47. An Example of a Valid Driver Interface Voltage Time Function.
\[ V_{\text{Ospec}} \text{Set} \triangleq \text{The Set of All Preliminary Driver Voltages} \]

\[ = \{ V_{\text{Ospec}} \} \]

\[ \forall t, V_{\text{Ospec}}^{(0)}(t) \in [-25, 25] \}

Figure 48. The Set of Preliminary Driver Voltage Time Functions.
\[ V_{\text{Ospec\_NonAd}} \triangleq \text{The Non Adaptive Set of Valid Driver Voltages} \]
\[ = \{ v_{\text{Ospec\_NonAd}} \mid v_{\text{Ospec\_NonAd}} \in V_{\text{Ospec\_Set}} \text{ and } \forall \ p_{\text{Electrical\_Model}} \in P_{\text{Electrical\_Model\_Set}} (v_{\text{Ospec\_NonAd}}), \]
\[ v_{\text{Xspec}} (p_{\text{Electrical\_Model}}, v_{\text{Ospec\_NonAd}}) \in V_{\text{Xspec\_Set}} \} \]

Figure 49. The Set of Valid Non-Adaptive Driver Voltage Time Functions.
Figure 50. The Set of Adaptive Parameter Arrays for \( \langle \text{Electrical\_Model} \rangle \).
\( \langle V_{\alpha\text{-Controller}} \rangle \) is a non-deterministic continuous state machine.

The states of \( \langle V_{\alpha\text{-Controller}} \rangle \) are

\[
S = \{ \{ -25, 25 \}, \neg, \neg, \cdots \} \rightarrow \{ \{ -25, 25 \}, \neg, \neg, \cdots \}
\]

The input signals of \( \langle V_{\alpha\text{-Controller}} \rangle \) are

\[
X_1 \text{ alias In\_Data} : \text{static} \{ \langle H \rangle, \langle L \rangle \} \rightarrow \{ \text{static} \{ \langle H \rangle, \langle L \rangle \} \}
\]

\[
X_2 \text{ alias } V_{\text{Xdpec}} : [\neg, [-30, 30], \neg, \neg, \cdots] \rightarrow [\neg, [-30, 30], \neg, \neg, \cdots]
\]

The output signals of \( \langle V_{\alpha\text{-Controller}} \rangle \) are

\[
Z_1 \text{ alias } V_{\text{spec}} : \{ [-25, 25], \neg, \neg, \cdots \} \rightarrow \{ [-25, 25], \neg, \neg, \cdots \}
\]

\[
Z_2 \text{ alias } \text{Busy} : \text{static} \{ B, NB \} \rightarrow \{ \text{static} \{ B, NB \} \}
\]

\[
Z_3 \text{ alias } \text{Error} : \text{static null} \rightarrow \text{pulsed} \{ \text{null, error} \} \rightarrow \{ \text{static null} \}
\]

The behavior set of \( \langle V_{\alpha\text{-Controller}} \rangle \) is

\[
B_{\text{NonAd}} = \{ (\neg, \neg), (V_{\text{spec}} \cdot, \neg, \neg) \}
\]

\[
v_{\text{spec}} \cdot \in V_{\text{spec}}\text{NonAd} \cdot
\]

Figure 51. The \( \mu\text{SAN} \) Specification for a Non-Adaptive \( \langle V_{\alpha\text{-Controller}} \rangle \).
\(<V_{\text{O-Controller}}\) is a non-deterministic continuous state machine.

The states of \(<V_{\text{O-Controller}}\) are

\[
S = \{ [-25, 25], \sim, \sim, \cdots \} \rightarrow \{ [-25, 25], \sim, \sim, \cdots \}
\]

The input signals of \(<V_{\text{O-Controller}}\) are

\[
X_1 \text{ alias } \text{In\_Data} : \text{static} \{ \langle H \rangle, \langle L \rangle \} \rightarrow \text{static} \{ \langle H \rangle, \langle L \rangle \}
\]

\[
\forall i \text{ alias } V_{\text{xppec}} : \{ \sim, [-30, 30], \sim, \sim, \cdots \} \rightarrow \{ \sim, [-30, 30], \sim, \sim, \cdots \}
\]

The output signals of \(<V_{\text{O-Controller}}\) are

\[
Z_1 \text{ alias } V_{\text{Ospec}} : \{ [-25, 25], \sim, \sim, \cdots \} \rightarrow \{ [-25, 25], \sim, \sim, \cdots \}
\]

\[
Z_2 \text{ alias } \text{Busy} : \text{static} \{ B, NB \} \rightarrow \text{static} \{ B, NB \}
\]

\[
Z_3 \text{ alias } \text{Error} : \text{static} \text{null} \rightarrow \text{pulsed} \{ \text{null, error} \} \rightarrow \text{static} \text{null}
\]

The behavior set of \(<V_{\text{O-Controller}}\) is

\[
B_{\text{Ad}}^* = \{ (\sim, v_{\text{xppec}}\text{spec}^*), (v_{\text{Ospec}}\text{Ad}^*, \sim, \sim), \ldots \}.
\]

\[
v_{\text{Ospec}}\text{Ad}^* \in V_{\text{OpecSet}}^*
\]

and

\[
\forall \text{P\text{Electrical\_Model}} \in P_{\text{Electrical\_ModelSetAd}}(v_{\text{Ospec}}\text{Ad}, \langle v_{\text{Omin}}(t_i), v_{\text{xppec}}(t_i) \rangle, \ldots, \langle v_{\text{Omax}}(t_K), v_{\text{xppec}}(t_K) \rangle)
\]

\[
v_{\text{xppec}}(\text{P\text{Electrical\_Model}}, v_{\text{Ospec}}\text{Ad}^*) \in V_{\text{xppecSet}}^*
\]

and

\[
\forall i = 1 \ldots K,
\]

\[
v_{\text{xppec}}(\text{P\text{Electrical\_Model}}, v_{\text{Ospec}}\text{Ad}(t_i)) = v_{\text{xppec}}(t_i)
\]

Figure 52. The \(\mu\text{SAN} \) Speciﬁcation for an Adaptive \(<V_{\text{O-Controller}}\).
Driver Interface Voltage

\[ t := -6 \ldots 6 \]

\[ v\text{xdriver}(t) := (0.4 \cdot t)^3 - 0.4 \cdot t^2 + 0.2 \cdot t + 10 \]

![Graph of v\text{xdriver}(t) vs t]

Driver Voltage

\[ C_t := 500 \cdot 10^{-12} \quad R_I := 4000 \]
\[ R_o := 1000 \quad E_I := 1 \]

\[ v_o(t) := R_o \cdot C_t \cdot \frac{d}{dt} v\text{xdriver}(t) + \frac{R_I + R_o}{R_I} \cdot v\text{xdriver}(t) + \frac{R_o \cdot E_I}{R_I} \]

![Graph of v\text{o}(t) vs t]

Figure 53. An Example Behavior of \( \langle V_o_{-\text{Controller}} \rangle \).
\( \langle V_{x\_Sensor} \rangle \) is a finite state machine (FSM).

The states of \( \langle V_{x\_Sensor} \rangle \) are

\[
S = \text{static} \{ \langle H \rangle, \langle L \rangle \} \rightarrow \text{static} \{ \langle H \rangle, \langle L \rangle \}
\]

The input signal of \( \langle V_{x\_Sensor} \rangle \) is

\[
X_1 \text{ alias } V_{x\text{spec}} : \text{cont Real} \rightarrow \text{cont Real}
\]

The output signal of \( \langle V_{x\_Sensor} \rangle \) is

\[
Z_1 \text{ alias } \text{Out\_Data} : \text{static} \{ \langle H \rangle, \langle L \rangle \} \rightarrow \text{static} \{ \langle H \rangle, \langle L \rangle \}
\]

The next state functions of \( \langle V_{x\_Sensor} \rangle \) are

\[
\text{FNS} : CS \times V_{x\text{spec}} \rightarrow NS
\]

where \( CS = NS = \{ \text{static } \langle H \rangle, \text{static } \langle L \rangle \} \)

(1) if \( \text{cs} = \text{static } \langle L \rangle \) and \( v_{x\text{spec}}^{\circ} = 3 \) and \( \text{Dir}(v_{x\text{spec}}) = + \)

then \( \text{ns} = \text{static } \langle H \rangle \)

(2) if \( \text{cs} = \text{static } \langle H \rangle \) and \( v_{x\text{spec}}^{\circ} = -3 \) and \( \text{Dir}(v_{x\text{spec}}) = - \)

then \( \text{ns} = \text{static } \langle L \rangle \)

For all (state, input) combinations not show there is no state transition.

The output signal function of \( \langle V_{x\_Sensor} \rangle \) is

\[
\text{FOUT} : CS \rightarrow Z_1
\]

\[
\text{FOUT}(cs) = Z_1 = cs
\]

Figure 54. The µSAN Specification of \( \langle V_{x\_Sensor} \rangle \).
Figure 55. An Example Behavior of $V_{X_{Sensor}}$. 
BIBLIOGRAPHY


