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A CMOS Chaotic Oscillator

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A CMOS CHAOTIC OSCILLATOR

by

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Boonsin Chansilp

A CMOS CHAOTIC OSCILLATOR

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A chaotic oscillator may be used as the basic component of an associative memory (AM). An AM is capable of pattern separation and noise reduction. Chua's circuit is a widely used chaotic oscillator. This circuit consists of a nonlinear resistor, two capacitors, an inductor and a resistor. A discrete implementation of Chua's circuit may be built using operational amplifiers, resistors, diodes, or discrete bipolar transistors. CMOS integrated circuit technology provides the opportunity for a compact implementation which enables construction of systems requiring a large number of oscillators. This thesis develops an integrated circuit design based on previous work performed by Cruz et. al. (1993).

The IC chip has been designed using a $2\,\mu$ m CMOS process. The IC consists of four operational transconductance amplifiers (OTAs), a resistor and three capacitors. The first two OTAs operate as Chua's diode (Cruz 1993) and the other two OTAs in conjunction with the third capacitor realize an inductor. The design process initially used the Spice3f4 circuit simulation package. The final design used Mentor Graphics for simulation, physical layout, Design Rule Checks (DRC), Layout Versus Schematic checks (LVS) and parasitic extraction. All data files as required by fabrication via the MOSIS service were generated.

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CHAPTER I

INTRODUCTION

In the past several years, synchronized chaos has been studied extensively. Applications include secure communication systems and associative memory [1]. This thesis describes an integrated circuit (IC) implementation of a popular chaotic oscillator based on previous work presented in [2-3].

Associative Memory

An associative memory (AM) stores memory patterns. The patterns are recalled via the presentation of a key pattern [1]. The associative memory is also able to perform noise reduction and pattern separation [4] as shown in Figure 1.

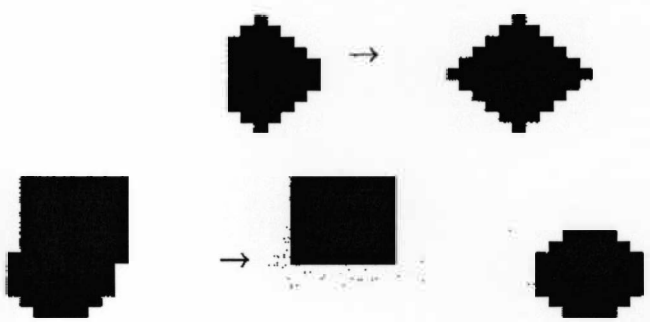


Figure 1. Two Cases of AM Recall Demonstrating Noise Reduction and Pattern Separation. A Diamond, Circle and Square are Stored Patterns (A. Lozowski et.al, 1996).

Source: A. Lozowski, et al. Chaotic CNN for Image Segmentation, in Proceedings ofthe 4th International Workshop on Cellular Neural Networks (CNNA'96), (Seville, Spain), June 24-26 1996: p.223

This figure shows two examples of associative memory operation. The recovery of an incomplete diamond shape demonstrates the noise reduction property of the AM. The associative memory selects the closest match to this key pattern, yielding a complete diamond shape for the output. For pattern separation, a combination of square and circle shapes is presented to the associative memory. The resulting output is a separation of these two patterns.

Interconnected nonlinear oscillators may be used to build an associative memory [4]. A simplified description is shown in Figure 2 [1].

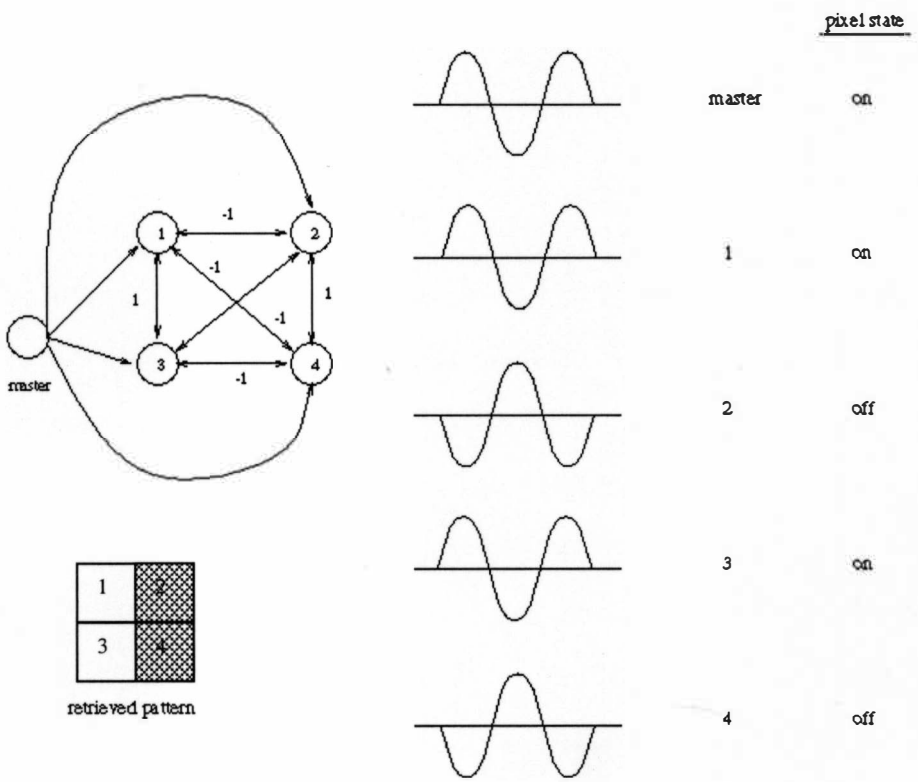


Figure 2. Block Diagram of a Simple Associative Memory (D.A. Miller,et. al,1999).

Source: D.A Miller, et al. Enhancing Electrical and Computer Engineering Education by Building Electronic Artificial Neural Networks. North Central Section Annual Meeting Proceedings. April 8-10, 1999: p. 180

> Each circle represents an oscillator. The lines indicate the presence of a coupling element which tends to either force two oscillators to have either the exact same (synchronization) or the exact opposite (anti-synchronization) output signal. These two states may be used to store binary bit information [1, pp.178].

The synchronization refers to "1 or ON" and anti-synchronization refers to "0 or OFF" in binary bit. The arrows indicate the direction of this influence. In Figure 2, four bits are represented. The key pattern is coupled to the network via specification of the signs (- or +) of the connections to the master free running oscillator. This free running master oscillator provides a reference to which other oscillators (1-4) may be compared to indicate the value of the stored bit [1].

Chua's Circuit: An Easily Realized Chaotic Oscillator

Description

This section describes the chaotic oscillator chosen for implementation. Chua's circuit is the simplest electronic circuit that can produce chaotic signals. The circuit is very simple as shown in Figure 3. It contains three linear storage components, one active resistor and one non-linear resistor. Due to its simplicity, Chua's circuit is widely used to study chaotic behavior. Furthermore, this circuit has been proven to exhibit chaotic behavior [2-3,5-6]. Chua's circuit has been physically realized using both discrete and integrated circuits.

A typical discrete design [5-6] uses a combination of operational amplifiers. The design of interest uses CMOS technology [2-3]. In this study, the design will emulate Cruz's design approach [2-3]. The circuit design uses four operational transconductance amplifiers (OTAs). Three storage capacitors are built using double-poly technology. The resistor will be connected externally. Major components inside the chip will be isolated from each other and connected externally as well. This

enables testing each section separately and the opportunity to replace any internal parts which do not work properly.

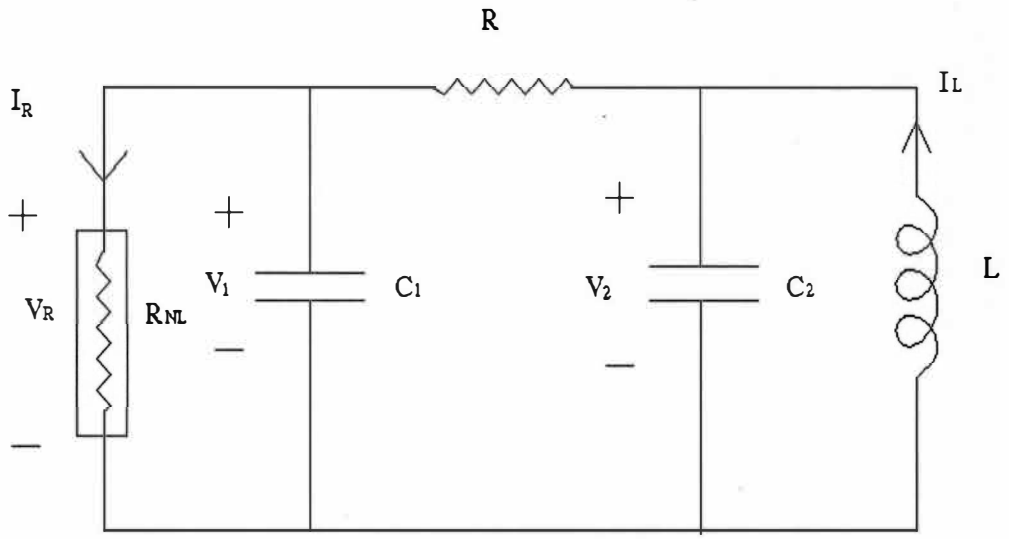


Figure 3. Chua's Circuit.

Chua's circuit is described by the following set of differential equations:

$$\frac{dv_1}{dt} = \frac{1}{RC_1}(v_2 - v_1) - \frac{I_R}{C_1} \qquad (1.1)$$

$$\frac{dv_2}{dt} = \frac{i_L}{C_2} - \frac{1}{RC_2}(v_2 - v_1) \qquad (1.2)$$

$$\frac{di_L}{dt} = -\frac{v_2}{L} \qquad (1.3)$$

where v_1 is voltage across capacitor C_1, v_2 is voltage across capacitor C_2, i_L is the current through inductor L, and I_R is the current through non-linear resistor. The relationship of I_R and V_R is shown in Figure 4.

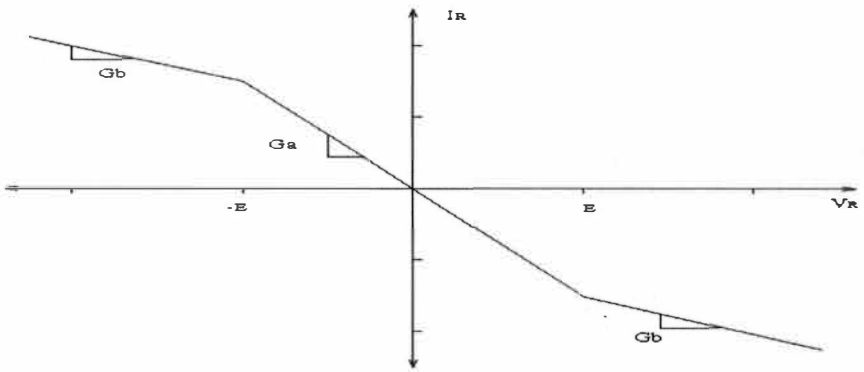


Figure 4. Driving-Point Characteristic of the Nonlinear Resistor.

This relationship can be expressed as:

$$I_R = f(v_R) = \begin{cases} G_b v_R + (G_b - G_a) & if \quad v_R < -E \\ G_a v_R & if \quad -E \le v_R \le E \\ G_b v_R + (G_a - G_b) & if \quad v_R > E \end{cases} \tag{1.4}$$

where G_a is slope of I_R when -E $\le v_R \le$ E, G_b is slope of I_R when $v_R <$ -E and $v_R >$ E , and E is the break point.

Simulation of Circuit Differential Equations

Chua's equation will be simulated by using Mathematica. The source code is shown in Appendix A.

Chua's circuit may be represented in a normalized form where:

$$\alpha = C_2 / C_1 \tag{1.5}$$
$$\beta = R^2 C_2 / L \tag{1.6}$$
$$G_a = -(1+\varepsilon)/R \tag{1.7}$$
$$G_b = -(1-\varepsilon)/R \tag{1.8}$$

The following values of these parameters have been formed to provide robust chaotic behavior for use in associative memories [A.Lozowski]: $\alpha = 10$, $\beta = 16$ and $\varepsilon = -0.5$. Thus, we select $R = 1000\,\Omega$, $C_1 = 15\ pf$ and $E = 1\ V$. Then $C_2 = 150\ pf$, L = 9.375 μ H, G_a = -0.5 mA/V and G_b = -1.5 mA/V.

Before simulating the circuit, the DC operating point of the circuit has been calculated. This computation is illustrated in Figure 5.

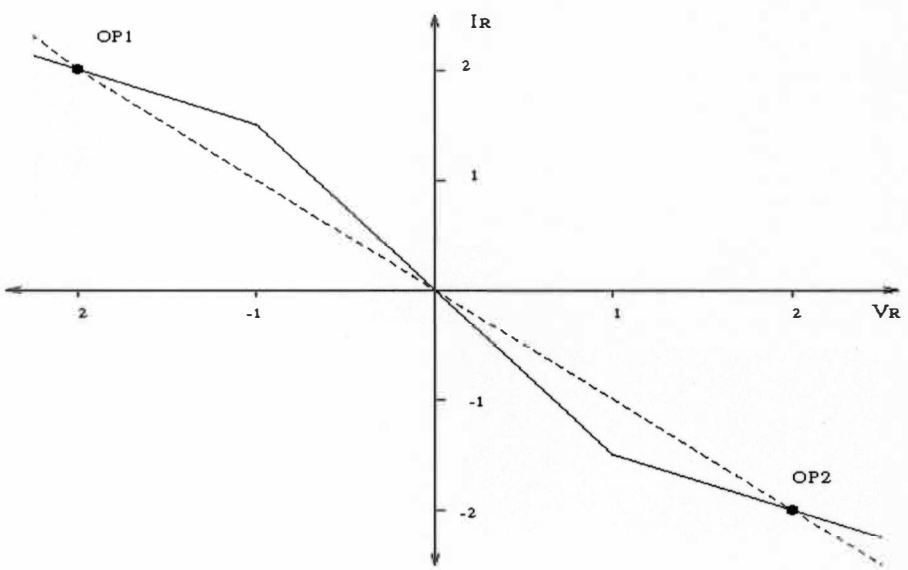


Figure 5. Computation of DC Operating Point.

The operating points are (-2,2) and (2,-2). These points are unstable; however, the output of circuit still remains bounded [5-6]. The state is repelled from one point to another as indicated in Figure 6. Note the complex behavior of these signals. The system state, though completely deterministic, is unpredictable after a short time. Thus the system states appear to be random. This property is useful in endowing AMs with pattern separation abilities.

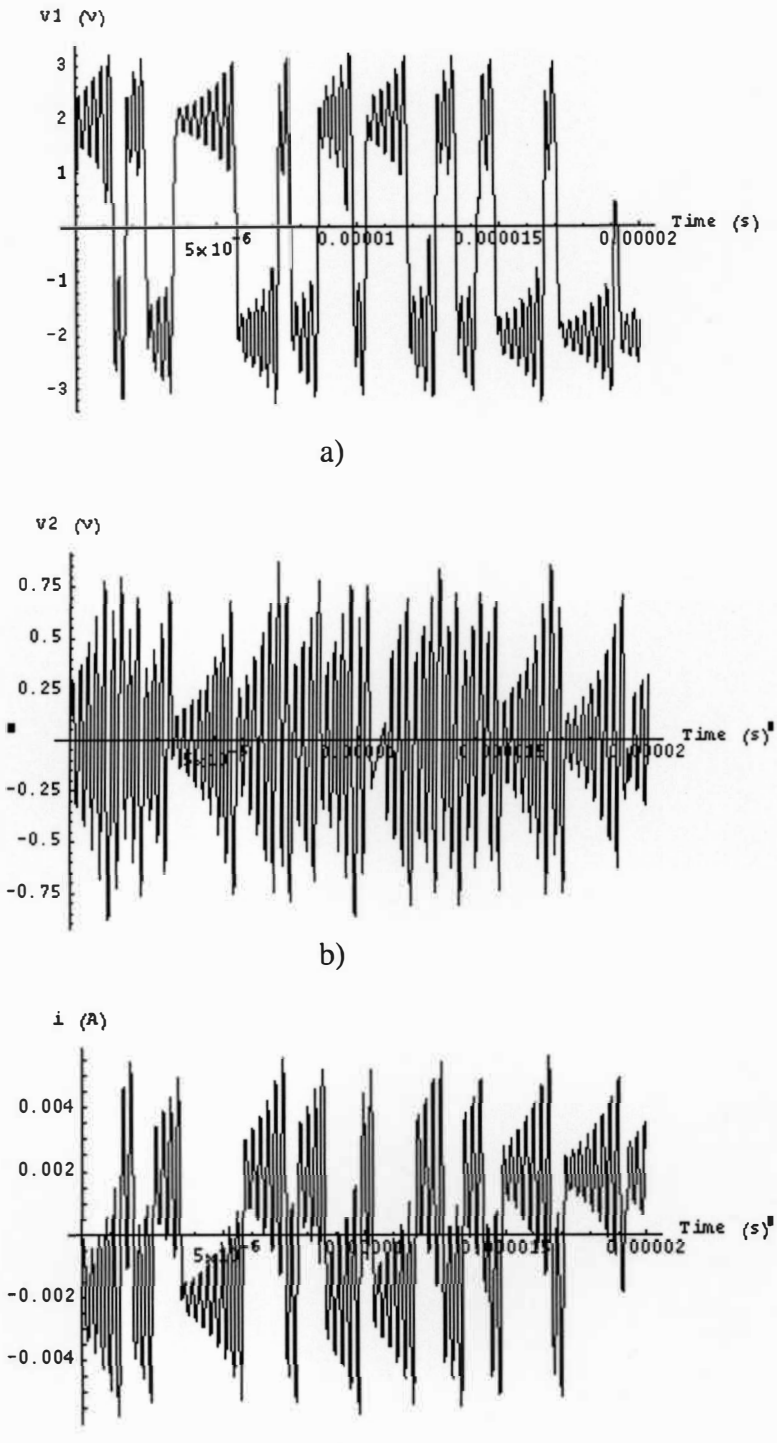
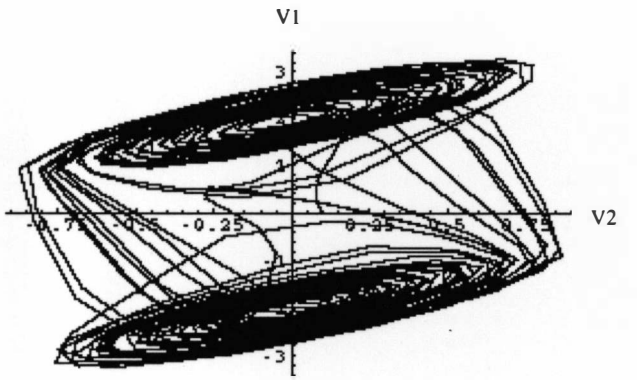
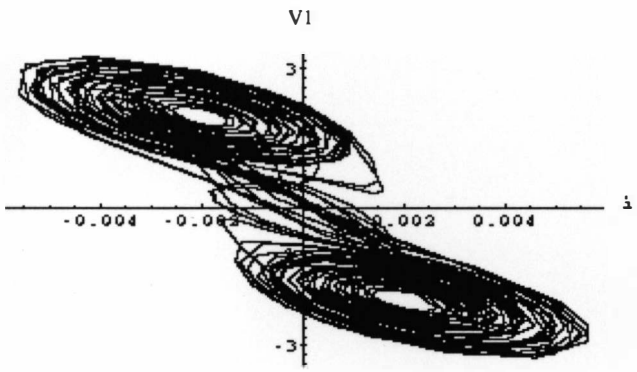


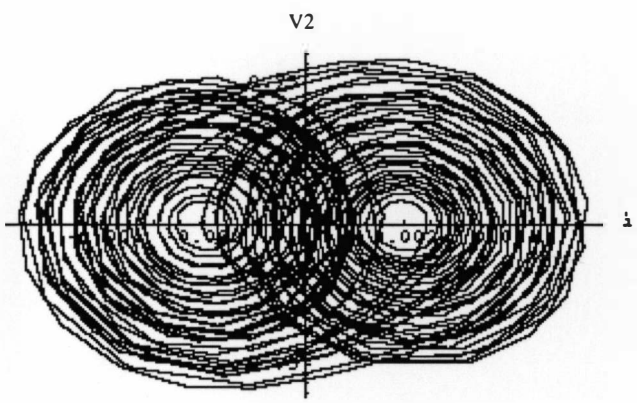
Figure 6. Chaotic Signal Generated by Chua's Circuit (Mathematica Simulation): (a) V_1, (b) V_2, and (c) i.



(a)



(b)



(c)

Figure 7. State Variables of Chaotic Signals Generated by Chua's Circuit (Mathematica Simulation):(a) V_1 vs. V_2, (b) V_1 vs. V_3, and (c) V_2 vs. V_3.

The result is a chaotic signal which oscillates around the previously described fixed points. Example simulated waveforms are shown in Figures 6 and 7. Having described Chua's circuit and its applications, the design of an integrated circuit implementation will now be considered.

CHAPTER II

CIRCUIT DESIGN

Nonlinear Resistor

In this chapter, an IC design of Chua's circuit is described. Again, note that this design is based in large part on the work in [2-3].

This design should realize the driving-point characteristic of Figure 4. The nonlinear resistor is implemented by two operational transconductance amplifiers (OTAs) connected in series [2-3] as shown in Figure 8.

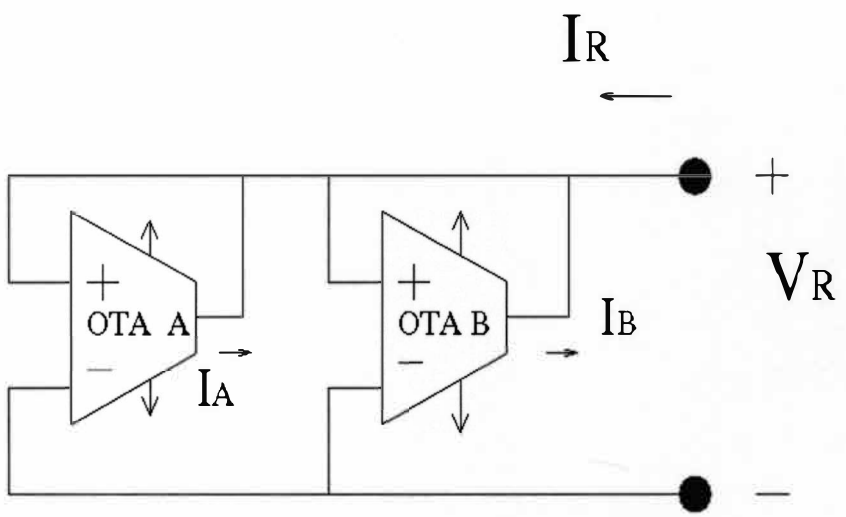


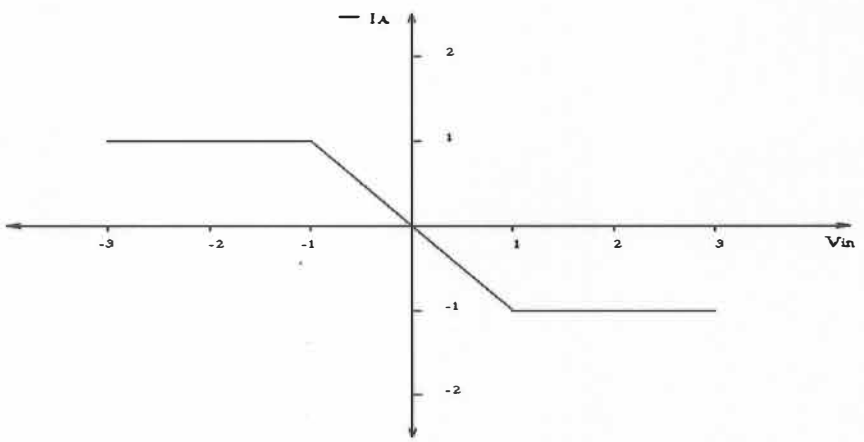
Figure 8. Nonlinear Resistor Implemented With Two OTAs.

The I_R current is the sum of I_A and I_B, where I_A is OTA A's current and I_B is OTA B's current. The transfer characteristics of the two OTAs should be

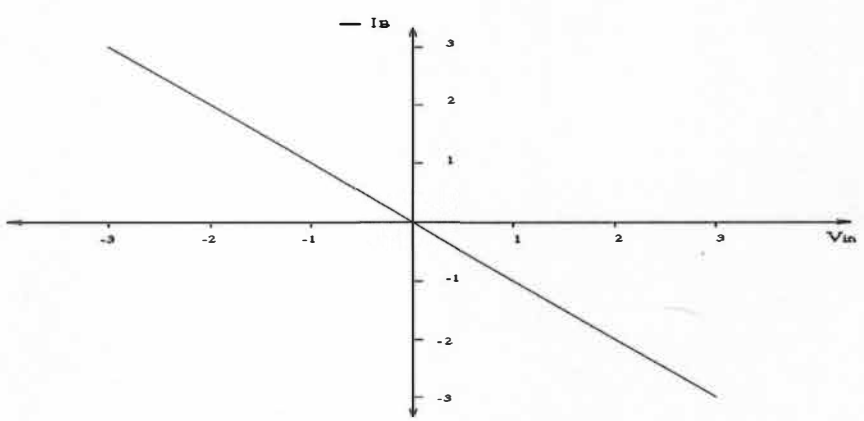
$$I_A = f_A(v_R) = \begin{cases} -g_A E & if \quad v_R < -E \\ g_A v_R & if \quad -E \le v_R \le E \\ g_A E & if \quad v_R > E \end{cases} \tag{2.1}$$

$$I_B = f_B(v_R) = g_B V_R \tag{2.2}$$

The transfer characteristics are shown in Figure 9.



(a)



(b)

Figure 9. Transfer Characteristics: (a) OTA A Transfer Characteristic, and (b) OTA B Transfer Characteristic.

The sum I_R is shown in Figure 4. Thus,

$$G_A = g_A + g_B \text{ , and} \quad (2.3)$$
$$G_B = g_B . \quad (2.4)$$

OTA Design

The OTA design is based on an input differential pair structure with relatively large transistors ($M_7 - M_{10}$). This can reduce flicker noise [2-3]. The OTA architecture is shown in Figure 10.

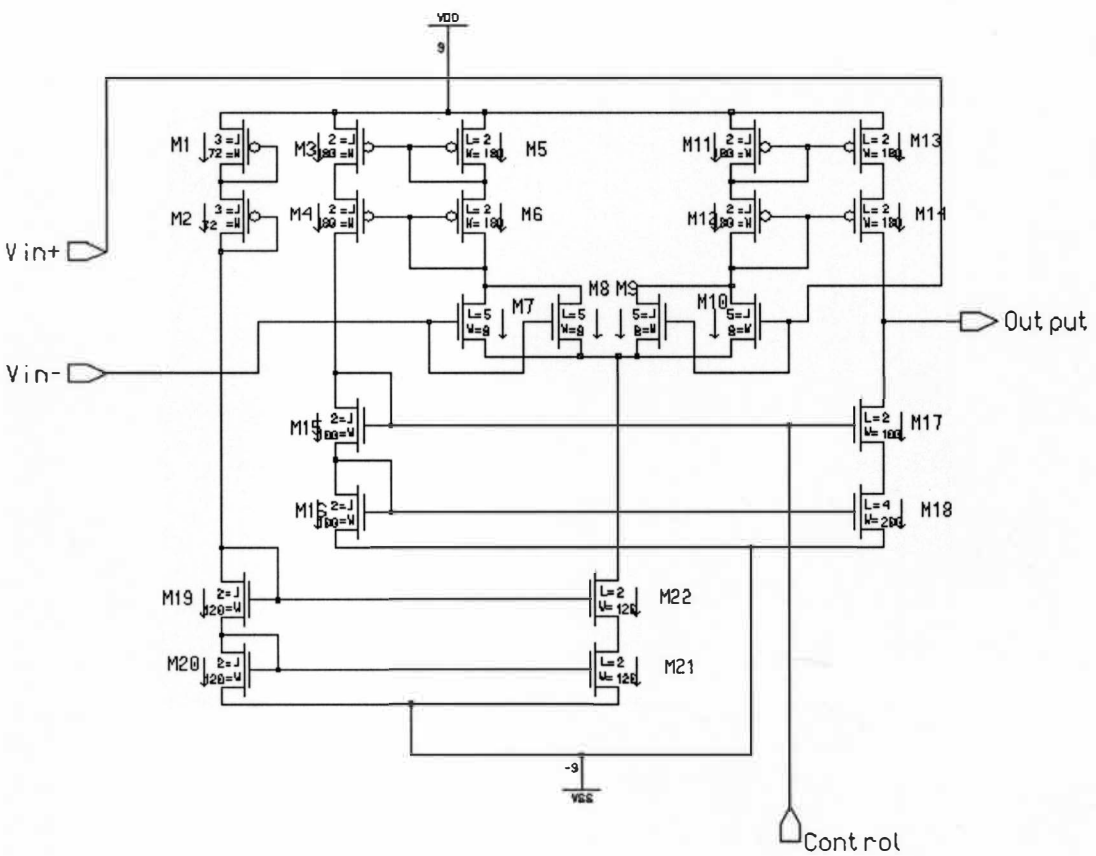


Figure 10. OTA Architecture.

A reference current is generated by the cascading of M_1, M_2, M_{19} and M_{20}. This cascading increases the circuit output resistance. NMOS transistors $M_7 - M_{10}$ form a differential pair. Use of a symmetric configuration with three current mirrors ($M_3 - M_6$ and $M_{11} - M_{22}$) will reduce the offset and increase the output swing [2-3].

In this research, Chua's circuit parameters have been fixed to obtain chaotic signals. From previous chapter, we selected $R = 1000\ \Omega$, $G_a = -1.5\ mA/V$, $G_b = -0.5\ mA/V$, $C_2 / C_1 = 10$, $L = R^2 C_2 / 16\ R$ and $E = 1V$. Selecting $C_2 = 150\ pF$ yields $C_1 = 15\ pF$ and $L = 0.00932\ mH$. From equations 2.4 and 2.5, the transfer characteristics of OTA A and OTA B will be $g_a = -1.0\ mA/V$ and $g_b = -0.5\ mA/V$, respectively. The dimension of a differential pair of an OTA obtained by solving

$$g_a = \sqrt{\mu Cox \frac{W_A}{L_A} I_A} \quad \text{and} \tag{2.4}$$

$$I_A = g_a E, \tag{2.5}$$

where I_A is reference current of the OTA A and μCox is dependent upon the CMOS technology. The μCox value used in the design is 52.58 $\mu A / V^2$ for NMOS transistors and 18.38 $\mu A / V^2$ for PMOS transistors. This yields $W_A / L_A = 2 \times 33/3$, $W_B / L_B = 2 \times 8/5$, $I_A = 1.0$ mA and $I_B = 3.6$ mA.

In additional, OTA B has extra terminals labeled "control". These terminals are connected to the gates of NMOS transistors (M_{15} and M_{17}). The control will connect to an external resistor and a voltage source. This voltage source either increases or decreases the mirror current dependent on voltage source. If the current increases, the transfer characteristic becomes steeper. On the other hand, if the mirror current decreases, the transfer characteristic becomes less steep.

Gyrator

Due to the inability of CMOS technology to provide an inductor, an OTA based gyrator is used. This consists of two OTAs and a capacitor. The design is shown in Figure 11.

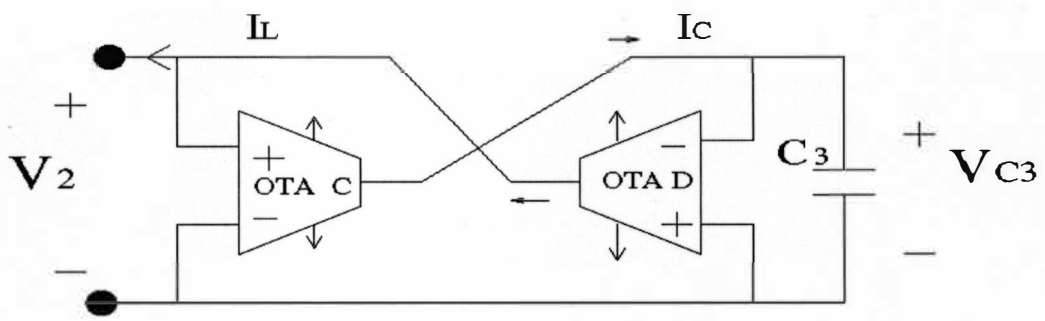


Figure 11. Gyrator Using Two OTAs and a Capacitor.

For OTA C, we can use the architecture of OTA B with a slope of -0.5 mA/V. For OTA D, g_D is selected at –2.0 mA/V. OTA D needs enough voltage swing for V_{C3} and sufficient current swing for I_D. The current I_D and current I_L are identical as shown in Figure 3. From the simulation of Chua's circuit by Mathematica, Figure 6(c) showed that the maximum current I_C is 6 mA. Thus, OTA D needs to generate enough current to cover this range. This can be done by increasing the dimension of active load. The voltage swing can be increased by increasing the dimension of transistors ($M_3 - M_6$ and $M_{11} - M_{14}$). The control of OTA C and D can be done as OTA B.

In Figure 11, The value of g_c, g_d, and C_3 can be obtained from

$$i_c = g_c v_2 = C_3 \frac{dv_{c3}}{dt} \text{ , and} \tag{2.7}$$

$$i_L = g_d v_{c3} \tag{2.8}$$

The Lapalce transform yields

$$I_c(s) = g_c V_2(s) = sCV_{c3}(s) \text{ , and} \quad (2.9)$$
$$I_L(s) = g_d V_{c3}(s) \quad (2.10)$$

Rearranging the equations, we obtain the transfer function

$$\frac{I_L(s)}{V_2(s)} = \frac{g_c g_d}{sC_3} \quad (2.11)$$

which indicates that this circuit has an inductance of

$$L = \frac{C_3}{g_c g_d} \quad (2.12)$$

The design value for L is 9.375 *mH*. Selecting g_c = -0.5 *m A/V* and g_d = -2.0 *m A/V* , yields C_3 = 9.375 *pf*. The actual value in the final design of C_3 is 13 *pf*. This will be discussed in the next chapter.

CHAPTER III

CIRCUIT SIMULATION, LAYOUT AND VERIFICATION

Circuit Simulation

Spice3f4, developed by UC Berkley, and Mentor Graphics were used to design, simulate, and test the transfer characteristics of each OTA and verify the operation of Chua's circuit. The design process initially used Spice3f4 since this package is easier to use. MOSFET level 3 model parameters obtained from the MOSIS service fabrication are used. N91W test run as summarized in Table 1. The model level 3 parameters are shown in Appendix D.

Table 1

Technological Data

Parameters	n-channel	p-channel	Units
V_{th}	0.809	0.846	V
μCox	52.58	18.38	$\mu A/V^2$
γ	0.41	0.55	$\sqrt{V}$

The Spice3f4 source code of the OTAs and Chua's circuit are shown in Appendix A as well. After sizing the transistors to yield the desired simulated results using Spice3f4 the design was further developed using Mentor Graphics since this package also provides layout tools (IC station). The design in Mentor Graphics used

BSIM level 49 parameters obtained from the N91W fabrication test run by MOSIS service. The BSIM model parameters are shown in Appendix C. The simulation procedure started with entering the OTA designs into the Design Architecture in Mentor Graphics. The transistor dimensions of obtained from spice3f4 simulations were used for the initial design. To have the desired outputs in Mentor Graphics, the dimension of transistors needed to be changed because of the different simulation model (BSIM). The final transistor dimensions of the OTAs are shown in Table 2.

Table 2

Mask Device Dimensions

Device	A (microns)		B&C (microns)		D (microns)	
	W	L	W	L	W	L
M1, M2	26	4	72	3	180	2
M3, M4, M5, M6, M11, M12, M13, M14	40	2	180	2	400	2
M7, M8, M9, M10	33	3	8	5	30	5
M15, M16, M17, M18	70	2	100	2	200	2
M19, M20, M21, M22	40	2	120	2	200	2

All designs were subsequently simulated using Accusim II in Mentor Graphics. Each OTA was simulated separately. Then all OTAs were combined with the required resistor and capacitors to form Chua's circuit. The OTA simulation results are shown in Figure 12.

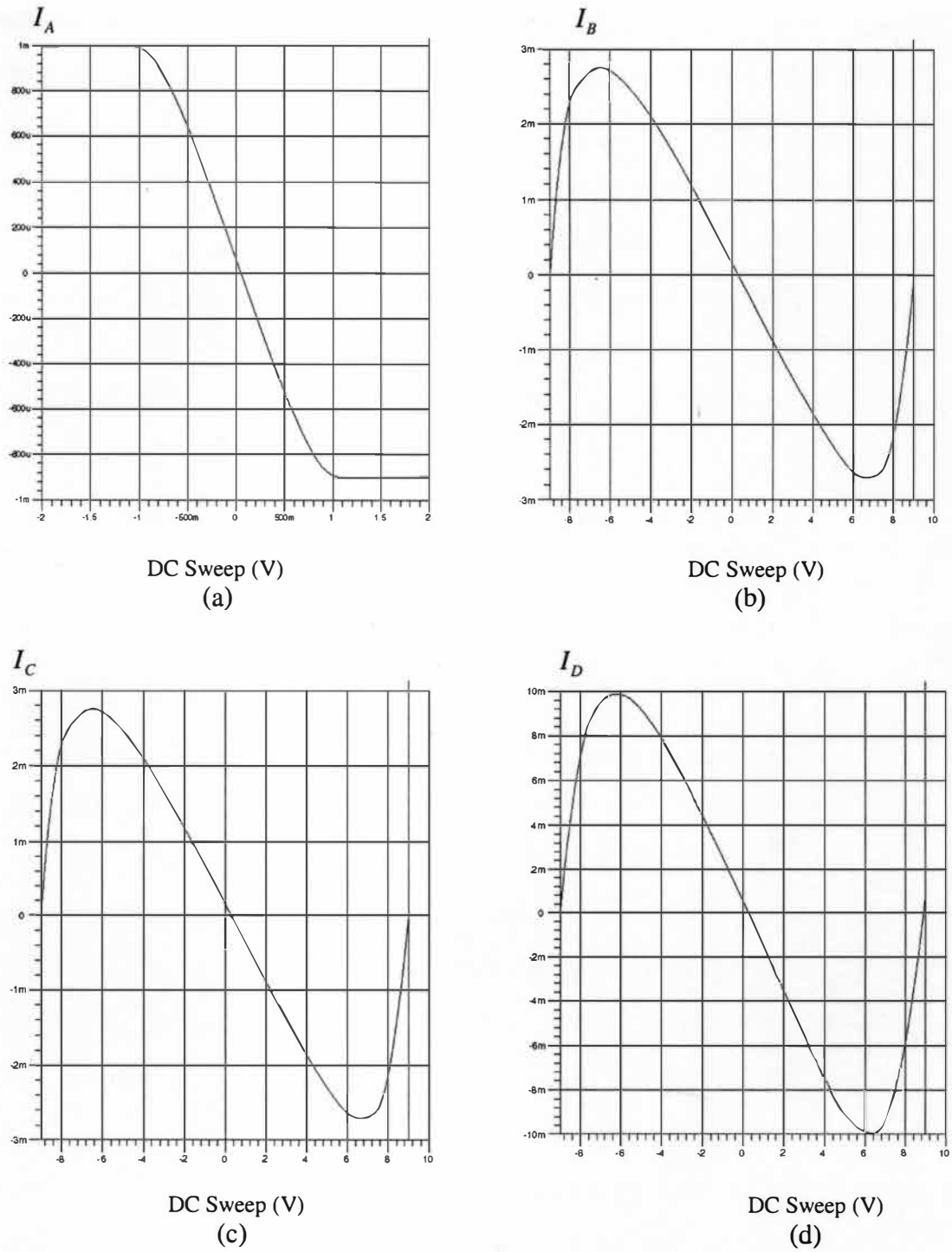
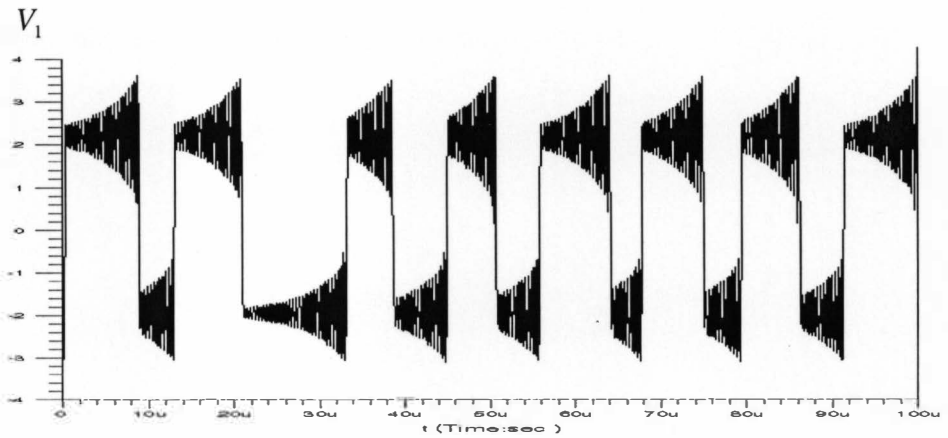


Figure 12. Transfer Characteristic of OTAs:(a) g_a = -1.0mA/V , (b) g_b = -0.5mA/V (c) g_c = -0.5mA/V , and (d) g_d = -2.0mA/V .

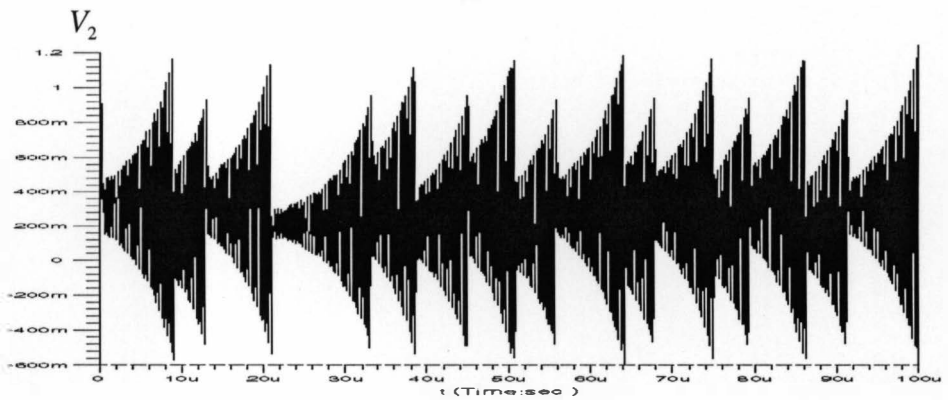
Note that the transfer characteristics are offset; nevertheless; these characteristics yielded acceptable behavior. The transistors dimension can be adjust to yield 1.0 mA for I_A but we cannot obtain I_B= 3.6 mA with g_b= -0.5 mA/V. If we increase the dimension of M_1 and M_2, the slope g_b will less than –0.5 mA/V. The maximum current we can obtain from OTA B was 2.8 mA and the range of voltages before the second break point is –6.2 V and 6.1V. However, this current and range of voltage are sufficient for the swing of V_1. For OTA D, the design needs a wide voltage range to yield the maximum linear region. As a result, the dimension of the current mirror and active load is very large (400/2 microns for $M_3 - M_6$ and $M_{11} - M_{14}$ transistor and 180/2 for active load). After observing all desired outputs of the OTAs, these OTA designs were used to build Chua's circuit in the Design Architecture. This circuit used R = 1000 Ω, C_1= 15 *pf*, C_2= 150 *pf*, and C_3= 16 *pf*. The value of C_3 yielded improved characteristics as compared to the previously computed value of 9.375 *pf*. The capacitors were used a 2 μm double-POLY CMOS technology by implementing POLY1 and POLY2 layers (called Electrode in Mentor Graphics) as capacitor plates. The value of capacitor obtains from

$$C = AC' \qquad (3.1)$$

where A is an area (μm^2) and C' is capacitance per unit area. This design used C' = 462 pF / mm^2 (see N91W test run in appendix D). That made the POLY area for C_1 = 32.47 mm^2, C_2= 324.7 mm^2 and C_3= 34.63 mm^2. In simulation, the initial voltages of capacitors have been set to small values ($V_{C1}(0)$ = 0 V, $V_{C2}(0)$ =0.1V, $V_{C3}(0)$=0V). The result chaotic signals of V_1, V_2 and V_3 are shown in Figure 13.



(a)



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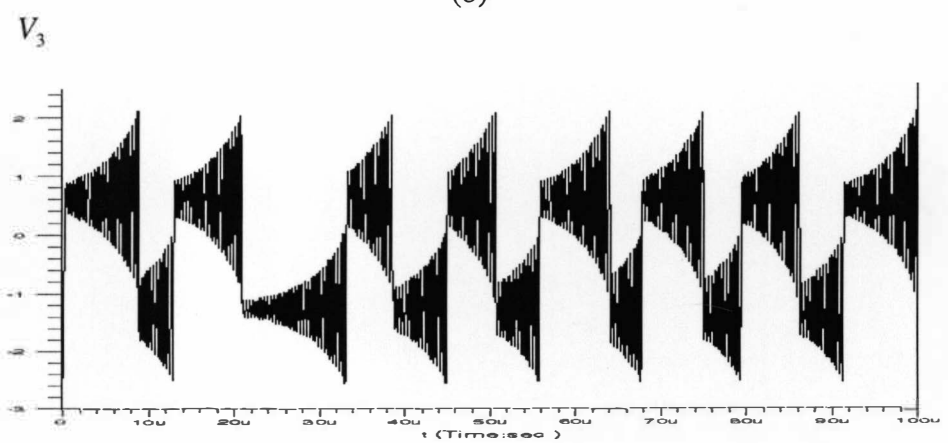
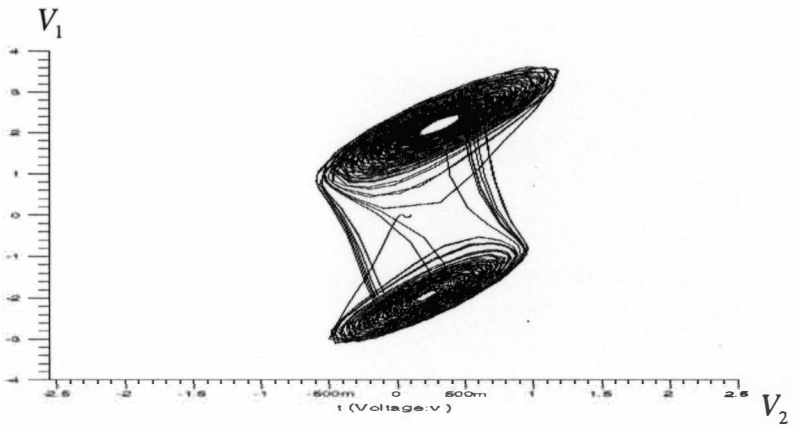
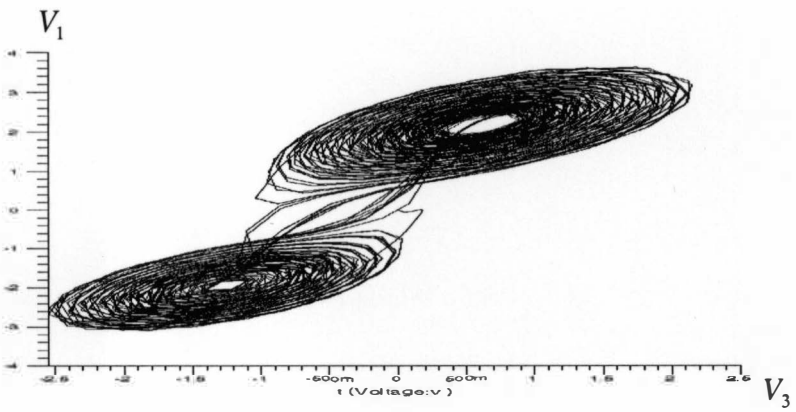


(c)

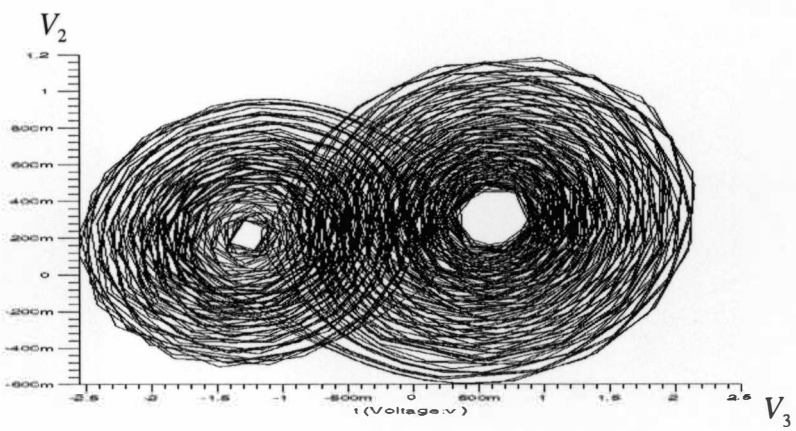
Figure 13. Chaotic Signals Generated by Mentor Graphics:(a) V_1, (b) V_2, and (c) V_3.



(a)



(b)



(c)

Figure 14. State Variable of Chaotic Signals:(a) V_1 vs. V_2, (b) V_1 vs. V_3, and (c) V_2 vs. V_3.

From Figure 13 (a), the chaotic signal oscillated around the +2v and –2v fixed point corresponding to the chaotic signal plotted by solving Chua's equation numerically. Further verification of the chaotic nature of these signals other than this qualitative comparison requires tools beyond the scope of this thesis. The next step of the CMOS chaotic oscillator design is layout and parasitic extraction using IC station.

Layout and Parasitic Extraction

The layout and parasitic extraction process includes the process of Design Rule Checking (DRC) and a Layout versus Schematic check (LVS). The DRC is a dimensional check of layout to verify that no design rules were violated. The LVS is the process that checks to see what was drawn in the layout has the same electrical functionality as the schematic. The LVS will show errors or missing connections if layout devices did not match with schematic devices. An example of LVS report is shown in Appendix C. To avoid mistakes and make the layout easy to fix when performing DRC and LVS, the design is best laid out separately. This means that each OTA will be laid out and tested against Design Rule Checking (DRC) and Layout versus Schematic (LVS) individually before forming Chua's circuit. Our layout does not address issues of device mismatches through variations in the die or temperature. This will be subject of later work. The layout of OTA is shown in Figure 15.

After all OTAs passed DRC and LVS checks successfully, the layout needed to be analyzed for parasitic extraction (IC trace) in the final step. The parasitic resistance and capacitance was back-annotated and the circuit was re-simulated. The performance of the circuit is satisfactory with back-annotation, thus the design is complete. Next, each OTA layout was merged into the Chua's circuit layout. This circuit needs to pass DRC and LVS as well. IC station does not currently have

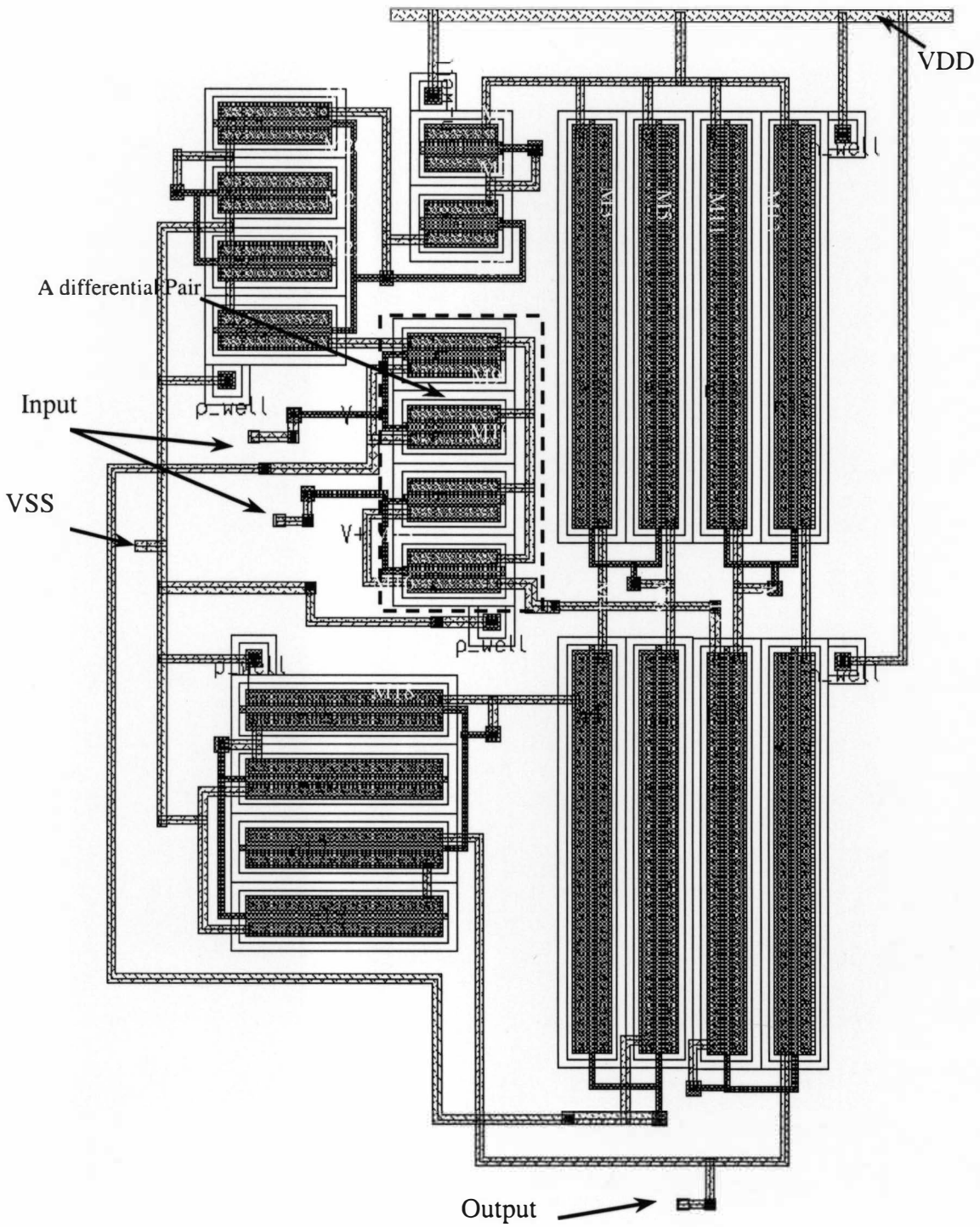


Figure 15. OTA Layout.

automated capacitor or resistor placement. It has only NMOS and PMOS transistor placement. Thus, the designer had to place capacitors manually. The resistor is an external device. The capacitors used were a 2 μm double-poly CMOS technology as referred to in a previous section. Chua's circuit was performed DRC and LVS check. There were no errors in DRC check and passed LVS check. Then, the back-annotation information was generated. The layout of Chua's circuit is shown in Figure 16.

Verification

After the parasitic were extracted, the simulation of the post-layout circuit needed to be done with the back-annotated information. Simulation required that resistor be added as an external device. The results are shown in Figures 17 and 18.

It can be seen that the chaotic signal resulting from post back-annotation simulation takes a slightly more time for swinging from one fixed point (-2V) to the other fixed point (+2V). However, the back-annotation circuit still generates a qualitatively acceptable chaotic signal. Verification of the chaotic nature of the signal will be the subject of later work.

Chip Architecture

The Chua's circuit design uses isolated OTAs and capacitors. These will be connected outside the chip. The circuit also requires an external resistor. OTA B, C and D have extra pins labeled control. These pins are used for adjusting the value of transfer function of OTA. The Chua's circuit architecture is shown in Figure 19.

The circuit uses a DIP 40 pin chip. The inputs and outputs of Chua's circuit had been assigned to the chip as shown in Figure 20.

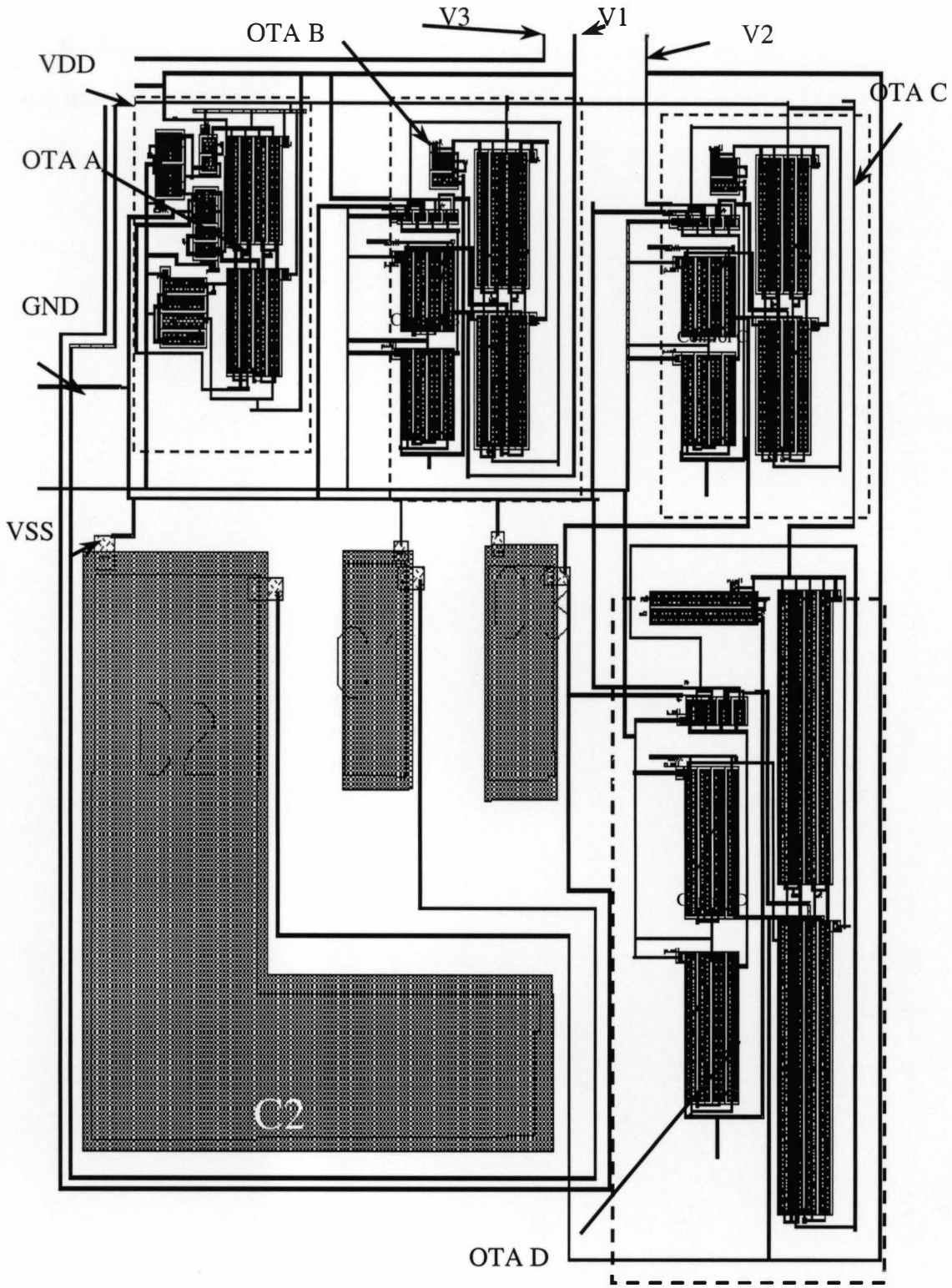


Figure 16. Layout of Chua's Circuit.

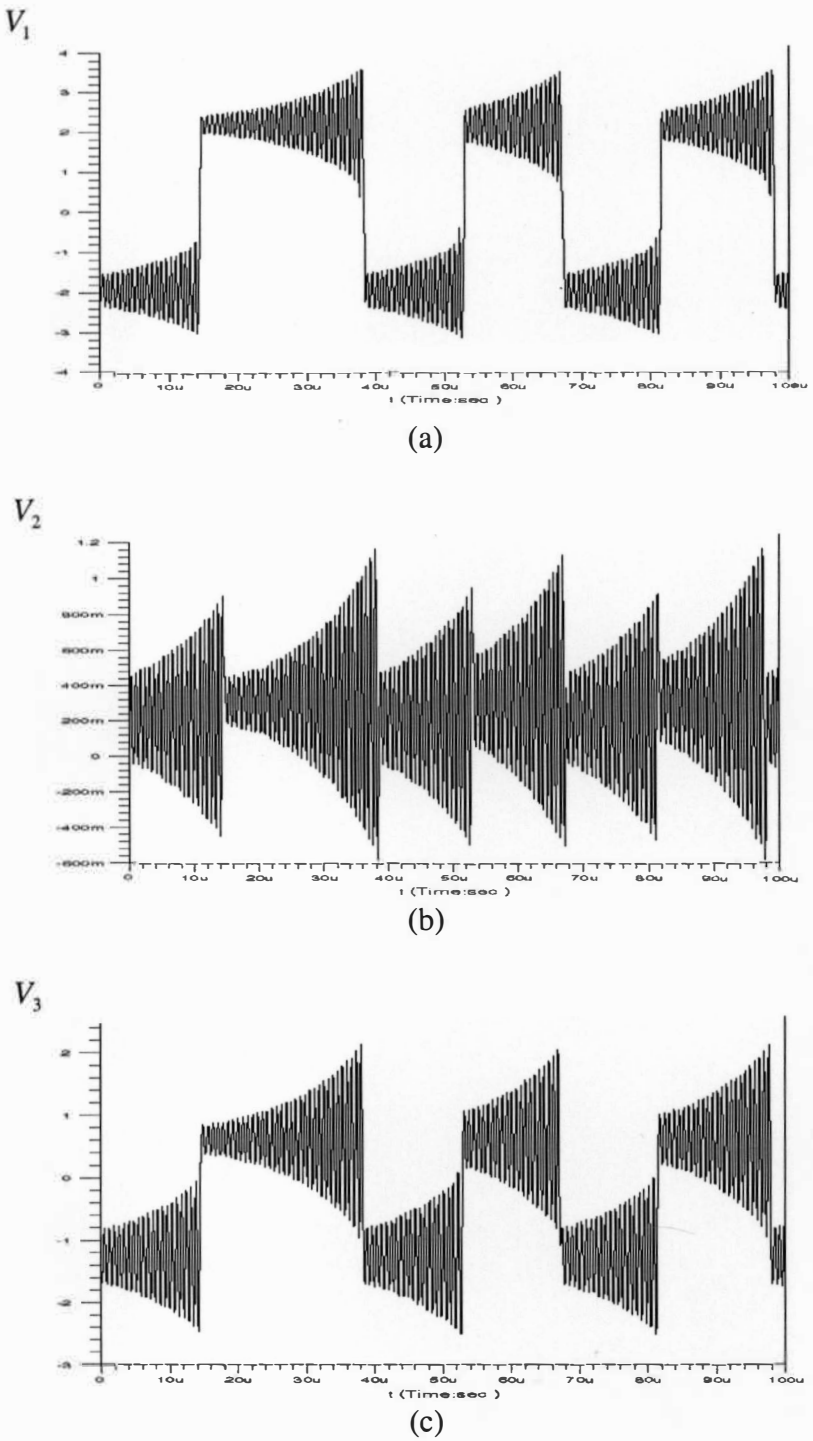
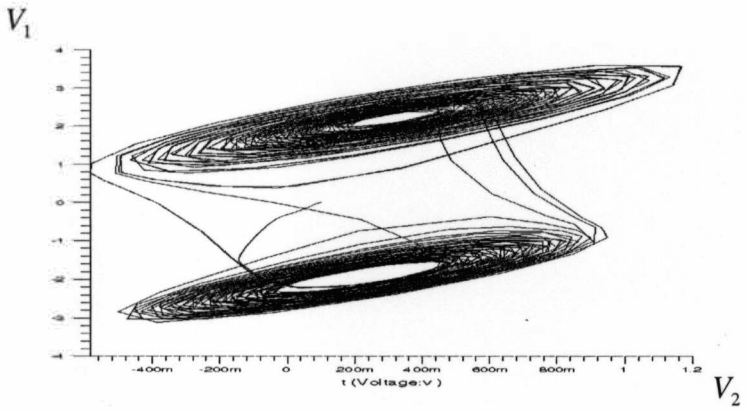
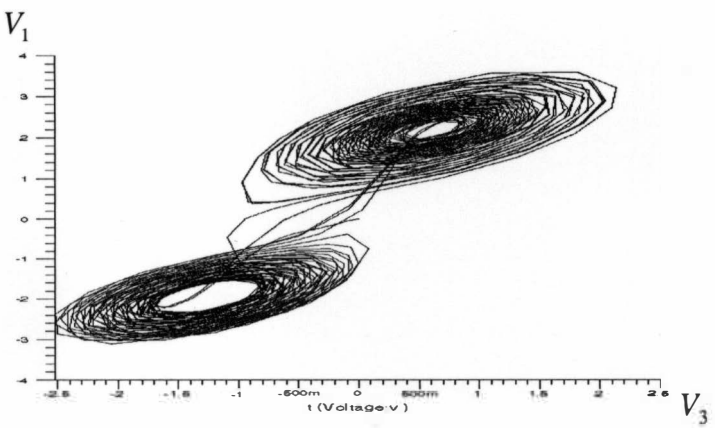


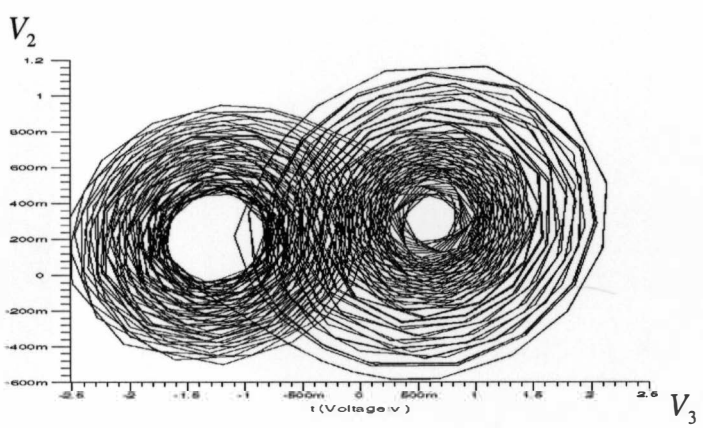
Figure 17. Simulations for Chua's Circuit After Back-Annotation:(a) V_1, (b)V_2, and (c) V_3.



(a)



(b)



(c)

Figure 18. Simulations for State Varible of Chua's Circuit After Back-Annotation: (a) V_1 vs. V_2, (b) V_1 vs. V_3, and (c) V_2 vs. V_3.

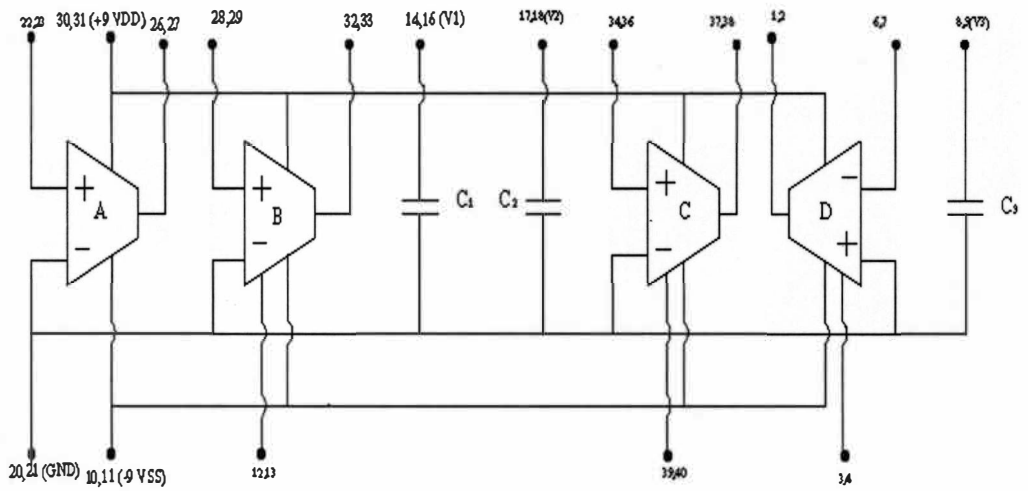


Figure 19. Disconnected Chua's Circuit Architecture.

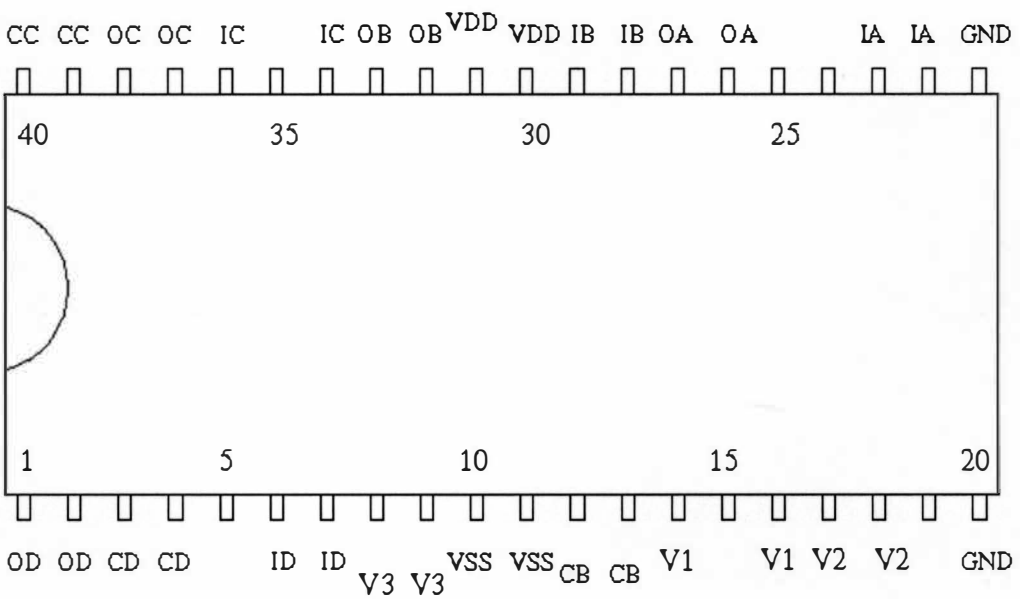


Figure 20. Chip Configuration.

The final chip design needs to have a pad-frame. The MOSIS Design Kit (MDK) provides an analog DIP 40 pad-frame. This pad-frame contains 40 pins. The disconnected Chua's circuit was wired to pad-frames and pin numbers were assigned. The DRC was performed again to make sure that no error while wring. At this time, the DRC found 4186 errors. The layout was re-checked and was found that the providing padframe form MDK had 4054 errors and each analog pad had 33 errors. The DRC error report is shown in Appendix C. One must assume that the libraries are correct that the pads are taking advantage of specialized design. A DRC was performed again and a DRC check of the core circuit returned a result of zero error. The LVS check is not helpful since this final chip has disconnected circuitry. Next, the final layout of Chua's chip was converted to MOSIS formats which are either GDSII or CIF formats. Thus, the chip is ready to be fabricated by the MOSIS service. The final chip layout is shown in Figure 21.

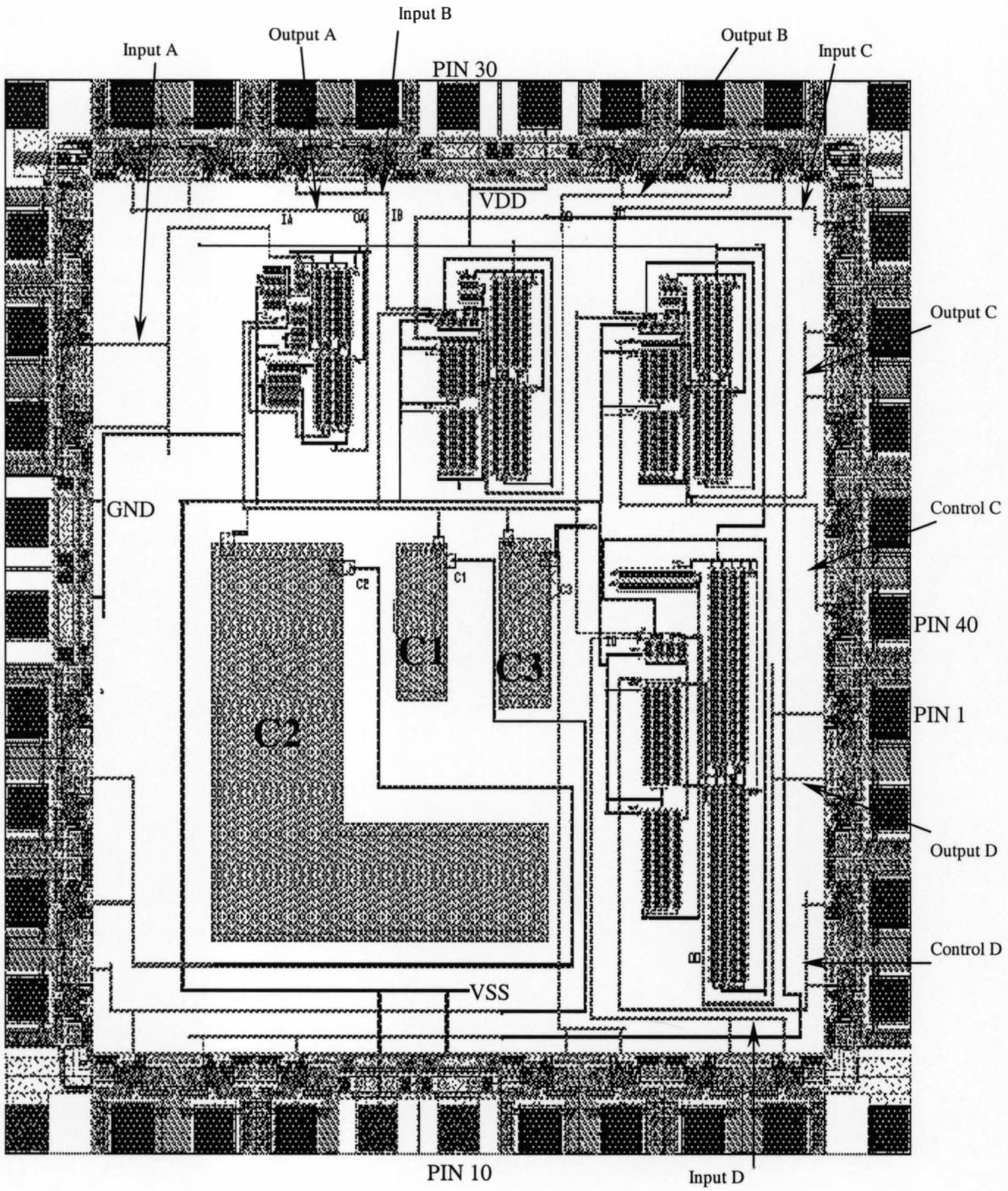


Figure 21. Final Chip Layout.

CHAPTER IV

CONCLUSION AND FUTURE WORK

This thesis described the design and test of a CMOS chaotic oscillator design (Chua's circuit) based on previous work by Cruz (1993) using Spice3f4 and Mentor Graphics. The circuit layout was performed using Mentor Graphics. The chip architecture used isolates OTAs and capacitors for ease of testing. The circuit will also use an external resistor. The simulation result of this circuit produced chaotic signals which are in close qualitative agreement with numerical predictions based on the Chua's equation. Files necessary for fabrication were generated.

The layout did not address the issues of device mismatches and thermal effects. The operation of the vendor supplied input/output pads needs to be verified. These topic will be the subjects of later work. The chaotic nature of the signals also requires future verification. Nevertheless, fabrication of this IC will provide the foundation for future work using this oscillator.

REFERENCES

[1] Miller, D.A., Severance, F.L, Barr, J., Barr, L., Chansilp, B., Kowalski, K.L., Lange, C.E., Marikar, A., Tolliver, J.K., Vieth, J.W. and Whitney, J.M., Enhancing Electrical and Computer Engineering Education by Building Electronic Artificial Neural Networks. North Central Section Annual Meeting Proceedings. April 8-10, 1999: 176-184.

[2] Cruz, J.M. and Chua L.O., A CMOS IC Nonlinear Resistor for Chua's Circuit. IEEE Transactions on Circuits and Systems Dec 1992: 985-995.

[3] Cruz, J.M. and Chua L.O., An IC Chip of Chua's Circuit. IEEE Transaction on Circuits and Systems. Oct 1993: 614-625.

[4] Lozowski, A, Cholewo, T.J, Jankowski, S. and Tworek, M., Chaotic CNN for Image Segmentation. In Proceedings of the 4th International Workshop on Cellular Neural Networks (CNNA'96), Seville, Spain. June 24-26, 1996. pp. 219-223.

[5] Kenedy, M.P., "Three Steps to Chaos-Part I: Evolution." IEEE Transactions on Circuits and Systems Oct. 1993: 640-656.

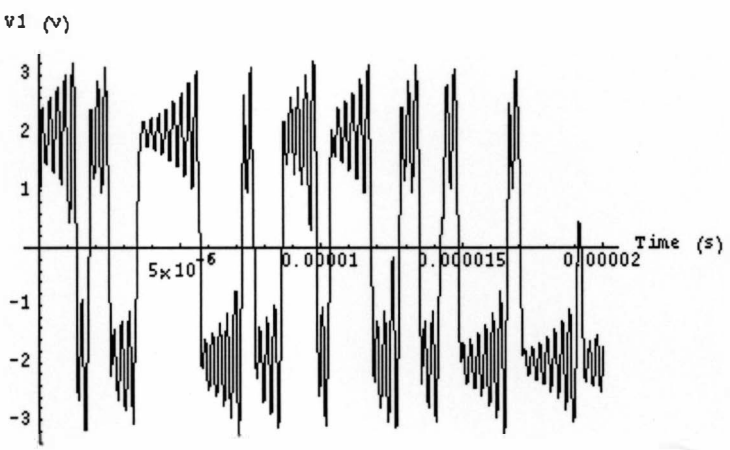
[6] Kenedy, M.P., "Three Steps to Chaos-Part II: A Chua's Circuit Primer." IEEE Transactions on Circuits and Systems Oct. 1993: 657-674.

Appendix A

Mathematica Code

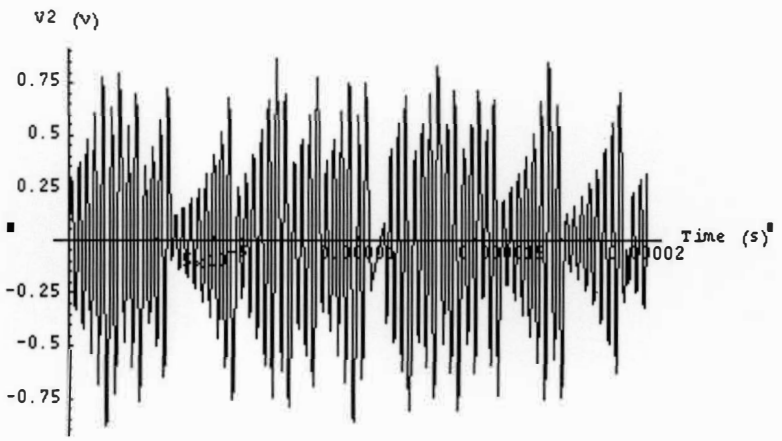
Listing of Mathematica's script for running Chua's equation.

```
E1=1;c1=15*10^-12;c2=150*10^-12;L=9.375*10^-6;G=0.001;m1=-
0.5*10^
-3;m2=-1.5*10^-3;(

sol=NDSolve[{v1'[t]==(G/c1)(v2[t]-v1[t])-((1/c1)(m1 v1[t]+0.5(m2-
m1)(Abs[v1[t]+E1]-Abs[v1[t]-E1]))),v2'[t]==(G/c2)(v1[t]-
v2[t])+(i[t]/c2),i'[t]==-
(v2[t]/L),v1[0]==0,v2[0]==0.1,i[0]==0},{v1,v2,i},{t,0,0.0001},MaxSteps-
>100000]

{{v→InterpolatingFunction[{{0.,0.0001}},<>],
v2→InterpolatingFunction[{{0.,0.0001}},<>],
i→InterpolatingFunction[{{0.,0.0001}},<>]}}



v1=Plot[Evaluate[v1[t] /. sol],{t,0,0.00002}];

Show[v1,AxesLabel->{"Time (s)", "v1 (V)"}]
```



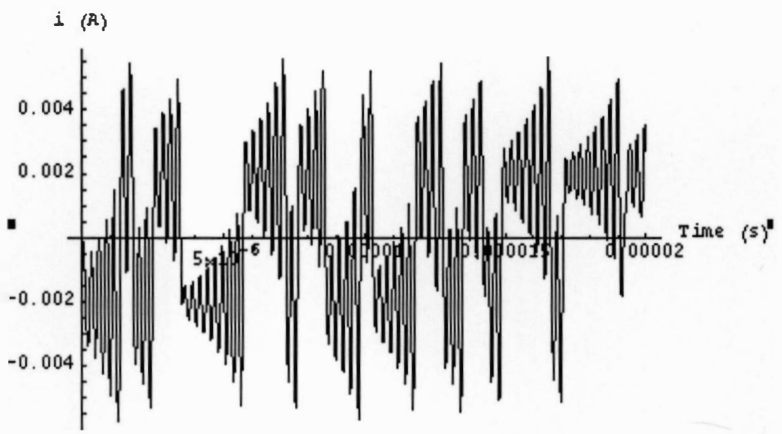
-Graphics-

```
V2=Plot[Evaluate[v2[t] /. sol],{t,0,0.00002}];

Show[v2,AxesLabel->{"Time (s)", "v2 (V)"}]
```



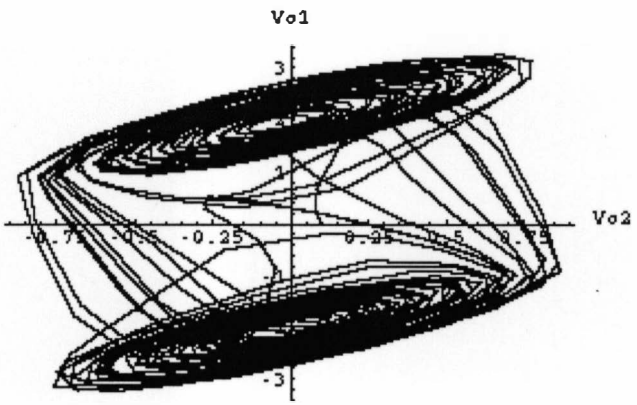
-Graphics-

```
i=Plot[Evaluate[i[t] /. sol],{t,0,0.00002}];

Show[i,AxesLabel->{"Time (s)", "i (A)"}]
```



-Graphics-

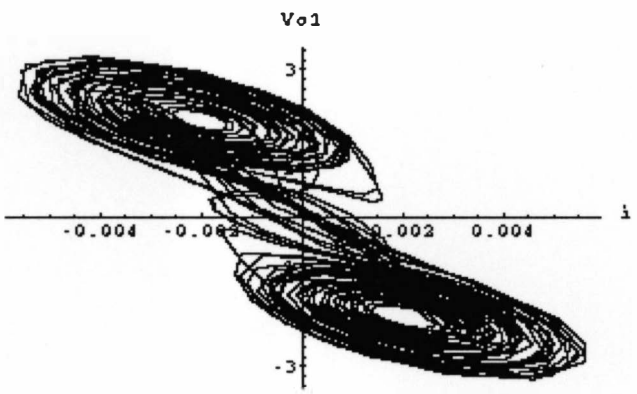
```
v1v2=ParametricPlot[{Evaluate[v2[t] /. sol][[1]],Evaluate[v1[t] /.
sol][[1]]},{t,0,0.00002}];

plot1=Show[v1v2,AxesLabel->{"Vc2", "Vc1"}]
```



-Graphics-

v1i=ParametricPlot[{Evaluate[i[t] /. sol][[1]],Evaluate[v1[t] /. sol][[1]]},{t,0,0.00002}]

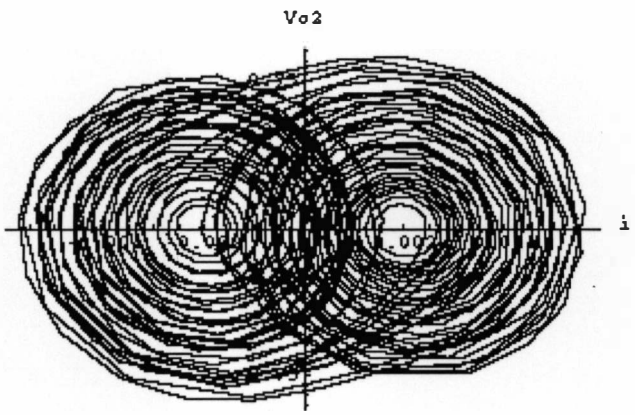
plot2=Show[v1i,AxesLabel->{"i", "Vc1"}]



-Graphics-

v2i=ParametricPlot[{Evaluate[i[t] /. sol][[1]],Evaluate[v2[t] /. sol][[1]]},{t,0,0.00002}]

plot3=Show[v2i,AxesLabel->{"i", "Vc2"}]



-Graphics-

Appendix B

Spice Model

Source code for simulating the circuit using Spice3f4.

This file is Chua's circuit file which contains three subfiles, botaa.mod, botab.mod and botad.mod.

```
*chua

*.OPTIONS NODE NOPAGE
** power Supply
.include botaa.mod
.include botab.mod
.include botad.mod
xamp1 1 2 3 4 5 botaa
xamp2 1 2 3 4 6 botab

xamp3 10 2 3 4 11 botab
xamp4 2 12 3 4 13 17 botad

VCC  3 0 DC 9v
VSS  4 0 DC -9v
*VP 1 0 dc 0v
VN 2 0 dc 0v

va 1 5 dc 0v
vb 1 6 dc 0v
vd 10 13 dc 0v
vc 12 11 dc 0v

R  1 10 1000

c3 12 2 10pf
c1 1 2 15pf
c2 10 2 150pf

*L 10 2 .009375mH

IC v(1)=0v v(10)=0v
IC v(12)=0v

.tran .01us .02ms
*.DC VP  -8 8 0.1
.plot TRAN i(L) v(10) v(1) v(12) i(vc) i(vd)
*.plot DC v(100) i(va) i(vb) i(vc) i(vd)  i(vr)

*.op
.PROBE
.END
```

This file is OTA A subfile which contains transistors and transistor model simulation.

```
*otaa.mod
*.OPTIONS NODE NOPAGE
```

```
** power Supply
.subckt botaa 100 2 1 4 5

*VCC   1 0 DC 5v
*VNEG  4 0 DC -5V

*VP  100 0 DC 0v
*VN  2   0 DC 0v

*va  100 5  DC 0v
*vb  999 13  DC 0v
*vc  99  5   DC 0v

M1    11  11  1   1 pfet W = 65U   L = 10U
M2    12  12  11  1 pfet W = 65U   L = 10U
M3    19  6   1   1 pfet W = 280U  L = 4U
M4    13  7   19  1 pfet W = 280U  L = 4U
M5    6   6   1   1 pfet W = 280U  L = 4U
M6    7   7   6   1 pfet W = 280U  L = 4U
M7    7   2   10    4 nfet W = 66U   L = 6U
M8    7   2   10    4 nfet W = 66U   L = 6U
M9    9   100   10  4 nfet W = 66U   L = 6U
M10   9   100   10  4 nfet W = 66U   L = 6U
M11   9   9   8   1 pfet W = 280U  L = 4U
M12   8   8   1   1 pfet W = 280U  L = 4U
M13   14  8   1   1 pfet W = 280U  L = 4U
M14   5   9   14  1 pfet W = 280U  L = 4U
M15   13  13  16  4 nfet W = 140U  L = 4U
M16   16  16  4   4 nfet W = 140U  L = 4U
M17   5   13  15  4 nfet W = 138U  L = 4U
M18   15  16  4   4 nfet W = 138U  L = 4U
M19   12  12  17  4 nfet W = 100U  L = 5U
M20   17  17  4   4 nfet W = 100U  L = 5U
M21   30  17  4   4 nfet W = 100U  L = 5U
M22   10  12  30  4 nfet W = 100U L = 5U

*N91W SPICE LEVEL3 PARAMETERS

.MODEL nfet NMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08 XJ=0.200000U
TPG=1
+ VTO=0.8093 DELTA=1.6500E+00 LD=4.1440E-07 KP=5.2580E-05
+ UO=618.2 THETA=5.3110E-02 RSH=1.5840E+01 GAMMA=0.4121
+ NSUB=3.7010E+15 NFS=5.9090E+11 VMAX=1.6760E+05
+ ETA=6.4270E-02
+ KAPPA=4.5740E-01 CGDO=5.2869E-10 CGSO=5.2869E-10
+ CGBO=3.4581E-10 CJ=1.4229E-04 MJ=6.2160E-01
+ CJSW=5.0307E-10
+ MJSW=2.4938E-01 PB=3.8328E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09

.MODEL pfet PMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08 XJ=0.200000U
TPG=-1
+ VTO=-0.8460 DELTA=4.6140E-01 LD=4.9340E-07 KP=1.8388E-05
+ UO=216.2 THETA=1.0720E-01 RSH=5.1170E+01 GAMMA=0.5557
+ NSUB=6.7290E+15 NFS=5.9090E+11 VMAX=2.6220E+05 ETA=7.9790E-02
+ KAPPA=1.0000E+01 CGDO=6.2948E-10 CGSO=6.2948E-10
+ CGBO=3.8539E-10 CJ=3.1476E-04 MJ=5.7042E-01 CJSW=3.1623E-10
+ MJSW=2.4970E-01 PB=8.8539E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.6070E-07
```

```
*.DC VP  -2 2 0.1
*.plot DC v(100) i(va) i(vb) i(vc) i(vd)
*.plot DC i(v1) i(va) i(vb) i(vc) i(vd) i(ve) i(vf) i(vg)
*.op
*.PROBE
.ENDS


This file is OTA B subfile which contains transistors and transistor
model simulation.

*OTA` B  ckt
.subckt botab 100 2 1 4 5

*VP  100 0 DC 0v
*VN  2   0 DC 0v

*va  100 5  DC 0v
*vb  999 13  DC 0v
*vc  99  5   DC 0v

M1    11  11  1   1 pfet W = 230U  L = 10U
M2    12  12  11  1 pfet W = 230U  L = 10U
M3    19  6   1   1 pfet W = 350U  L = 4U
M4    13  7   19  1 pfet W = 350U  L = 4U
M5    6   6   1   1 pfet W = 350U  L = 4U
M6    7   7   6   1 pfet W = 350U  L = 4U
M7    7   2   10    4 nfet W = 15U   L = 10U
M8    7   2   10    4 nfet W = 15U   L = 10U
M9    9   100   10  4 nfet W = 15U   L = 10U
M10   9   100   10  4 nfet W = 15U   L = 10U
M11   9   9   8   1 pfet W = 350U  L = 4U
M12   8   8   1   1 pfet W = 350U  L = 4U
M13   14  8   1   1 pfet W = 350U  L = 4U
M14   5   9   14  1 pfet W = 350U  L = 4U
M15   13  13  16  4 nfet W = 200U  L = 4U
M16   16  16  4   4 nfet W = 200U  L = 4U
M17   5   13  15  4 nfet W = 200U  L = 4U
M18   15  16  4   4 nfet W = 200U  L = 4U
M19   12  12  17  4 nfet W = 600U  L = 5U
M20   17  17  4   4 nfet W = 600U  L = 5U
M21   30  17  4   4 nfet W = 600U  L = 5U
M22   10  12  30  4 nfet W = 600U  L = 5U


*N91W SPICE LEVEL3 PARAMETERS

.MODEL nfet NMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08 XJ=0.200000U
TPG=1
+ VTO=0.8093 DELTA=1.6500E+00 LD=4.1440E-07 KP=5.2580E-05
+ UO=618.2 THETA=5.3110E-02 RSH=1.5840E+01 GAMMA=0.4121
+ NSUB=3.7010E+15 NFS=5.9090E+11 VMAX=1.6760E+05 ETA=6.4270E-02
+ KAPPA=4.5740E-01 CGDO=5.2869E-10 CGSO=5.2869E-10
+ CGBO=3.4581E-10 CJ=1.4229E-04 MJ=6.2160E-01 CJSW=5.0307E-10
+ MJSW=2.4938E-01 PB=3.8328E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09

.MODEL pfet PMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08 XJ=0.200000U
TPG=-1
```

```
+ VTO=-0.8460 DELTA=4.6140E-01 LD=4.9340E-07 KP=1.8388E-05
+ UO=216.2 THETA=1.0720E-01 RSH=5.1170E+01 GAMMA=0.5557
+ NSUB=6.7290E+15 NFS=5.9090E+11 VMAX=2.6220E+05 ETA=7.9790E-02
+ KAPPA=1.0000E+01 CGDO=6.2948E-10 CGSO=6.2948E-10
+ CGBO=3.8539E-10 CJ=3.1476E-04 MJ=5.7042E-01 CJSW=3.1623E-10
+ MJSW=2.4970E-01 PB=8.8539E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.6070E-07

*.DC VP  -2 2 0.1
*.plot DC v(100) i(va) i(vb) i(vc) i(vd)
*.plot DC i(v1) i(va) i(vb) i(vc) i(vd) i(ve) i(vf) i(vg)
*.op
*.PROBE
.ENDS

This file is OTA D subfile which contains transistors and transistor
model simulation.

*OTA D  ckt
*.OPTIONS NODE NOPAGE
** power Supply
.subckt botad 100 2 1 4 5 17

*VP  100 0 DC 0v
*VN  2   0 DC 0v
*va  100 5  DC 0v
*vb  999 13  DC 0v
*vc  99  5   DC 0v
*vbs 9999 17 DC 0v

M1    11  11  1   1 pfet W = 400U  L = 4U
M2    12  12  11  1 pfet W = 400U  L = 4U
M3    19  6   1   1 pfet W = 800U  L = 2U
M4    13  7   19  1 pfet W = 800U  L = 2U
M5    6   6   1   1 pfet W = 800U  L = 2U
M6    7   7   6   1 pfet W = 800U  L = 2U
M7    7   2   10   4 nfet W = 40U   L = 5U
M8    7   2   10   4 nfet W = 40U   L = 5U
M9    9   100  10  4 nfet W = 40U   L = 5U
M10   9   100  10  4 nfet W = 40U   L = 5U
M11   9   9   8   1 pfet W = 800U  L = 2U
M12    8    8    1    1 pfet W = 800U  L = 2U
M13    14   8    1    1 pfet W = 800U  L = 2U
M14    5    9    14   1 pfet W = 800U  L = 2U
M15    13   13   16   4 nfet W = 400U  L = 2U
M16    16   16   4    4 nfet W = 400U  L = 2U
M17    5    13   15   4 nfet W = 400U  L = 2U
M18    15   16   4    4 nfet W = 400U  L = 2U
M19    12   12   17   4 nfet W = 400U  L = 4U
M20    17   17   4    4 nfet W = 400U  L = 4U
M21    30   17   4    4 nfet W = 400U  L = 4U
M22    10   12   30   4 nfet W = 400U  L = 4U

*N91W SPICE LEVEL3 PARAMETERS

.MODEL nfet NMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08
XJ=0.200000U TPG=1
+ VTO=0.8093 DELTA=1.6500E+00 LD=4.1440E-07 KP=5.2580E-05
+ UO=618.2 THETA=5.3110E-02 RSH=1.5840E+01 GAMMA=0.4121
```

```
+ NSUB=3.7010E+15 NFS=5.9090E+11 VMAX=1.6760E+05 ETA=6.4270E-
02
+ KAPPA=4.5740E-01 CGDO=5.2869E-10 CGSO=5.2869E-10
+ CGBO=3.4581E-10 CJ=1.4229E-04 MJ=6.2160E-01 CJSW=5.0307E-10
+ MJSW=2.4938E-01 PB=3.8328E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09

.MODEL pfet PMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08
XJ=0.200000U TPG=-1
+ VTO=-0.8460 DELTA=4.6140E-01 LD=4.9340E-07 KP=1.8388E-05
+ UO=216.2 THETA=1.0720E-01 RSH=5.1170E+01 GAMMA=0.5557
+ NSUB=6.7290E+15 NFS=5.9090E+11 VMAX=2.6220E+05 ETA=7.9790E-
02
+ KAPPA=1.0000E+01 CGDO=6.2948E-10 CGSO=6.2948E-10
+ CGBO=3.8539E-10 CJ=3.1476E-04 MJ=5.7042E-01 CJSW=3.1623E-10
+ MJSW=2.4970E-01 PB=8.8539E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.6070E-07
*.tran .01us 1ms
*.DC VP  -2 2 0.1
*.plot TRAN v(100) i(va) i(vb) i(vc) i(vd)  v(5)
*.plot DC i(v1) i(va) i(vb) i(vc) i(vd) i(ve) i(vf) i(vg)
*.op
*.PROBE
.ENDS
```

However, you can run each OTAs individually but you need to change from *.mod* file to *.cir* file and modify some Spice commands.

Appendix C

How to Use Mentor Graphics

Setup for running Design Architecture and AccuSim II

Source: David M. Zar http://germanium.ee.wustl.edu/dzar/tutorials/sdl/sdl_toc.html

To run the Design Architecture and Accusim II, this script need to be put in MGC_LOCATION_MAP. You need to copy this file and put it in your working directory. This file below is an example of my Location_Map file. You may ask for UNIX administrator for help.

```
MGC_LOCATION_MAP_2

#
# MGC HEP Standard customization location
#
$MGC_HEP
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep

$UNIVSIG
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep

$UNIVSIG_LIB
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep

$SCMOS_IC_TECH
/home7/stpa098/s8chansi/mgc/scna20orbit.params3

#
# FROM ~mentorgr/mgc/etc/mgc_location_map
#

# MGC accuparts_lib V8.5_1
$MGC_APLIB
/home3/software/mentorgr/mgc_libs/accuparts_lib

# MGC asim_templt_lib V8.5_1
$MGC_TEMPLATELIB
/home3/software/mentorgr/mgc_libs/asim_templt_lib

# MGC accusim_smb_lib V8.5_1
$MGC_SMBLIB
/home3/software/mentorgr/mgc_libs/accusim_smb_lib

# BPL V8.5_2.1
$BPL_RLS_LIB
/home3/software/mentorgr/bpl_rls_lib
```

```
# MGC gen_lib V8.4
$MGC_GENLIB
/home3/software/mentorgr/mgc_libs/gen_lib

# MGC misc_lib V8.4
$MGC_MISCLIB
/home3/software/mentorgr/mgc_libs/misc_lib

# MGC passive_lib V8.4_2.1
$MGC_PASSIVELIB
/home3/software/mentorgr/mgc_libs/passive_lib
```

Setup for running IC station

This script will help you to run IC Station properly. You can put this file to your directory. The file below is an example for my directory. Ask for help from the UNIX administrator.

```
$setup_auto_checkpoint(@on, 15);
$setup_new_windows(@on, 0.5, 0.5, 1, 10, 0, 0, 5);
$setup_reports([@shape, @path, @text, @property_text, @instance, @device,
@array, @row, @pin, @via_object, @overflow, @net, @port], [@edges,
@properties, @ports, @nets, @row], @window, @notranscript, "");
$load_process("$MGC_HEP/technology/ic/scmos");
$load_rules("$MGC_HEP/technology/ic/scmos.rules");

#$add_menu_item(,$menu_bar_item("MD_K",
"mdk_pulldown",,,"Red"),"user_ic@@default_menu_bar");

$load_userware("/home7/stpa098/s8chansi/mgc/ic/mos", "user_ic", @ample);
$load_userware("/home7/stpa098/s8chansi/mgc/ic/mosfilter.ample","user_ic",
@ample);
$load_userware("$stpa098/s8chansi/mgc/ic/ic_area.ample", "user_ic", @ample);
```

Using DA to Capture a Design

1. Invoke Design Architecture by typing ***DA &*** in your workstation.
2. Once DA is running, open new sheet by using either menu bar or palette menu. Put file name, then an empty sheet will pop up.
3. Now start drawing circuit. Use the Librarian icon to show the ***MDK*** palette menu.
4. Click on ***SDL*** to show the SDL parts palette menu.
5. Now place instances of the n-fet-3 and p-fet-3 (three terminal n-fet and p-fet) to form an OTA design shown in figure 1. To make easier, we'll go through the process (DA to post simulation) with an OTA. After passing every step, then we can capture, simulate, layout, and back-annotate Chua's circuit.

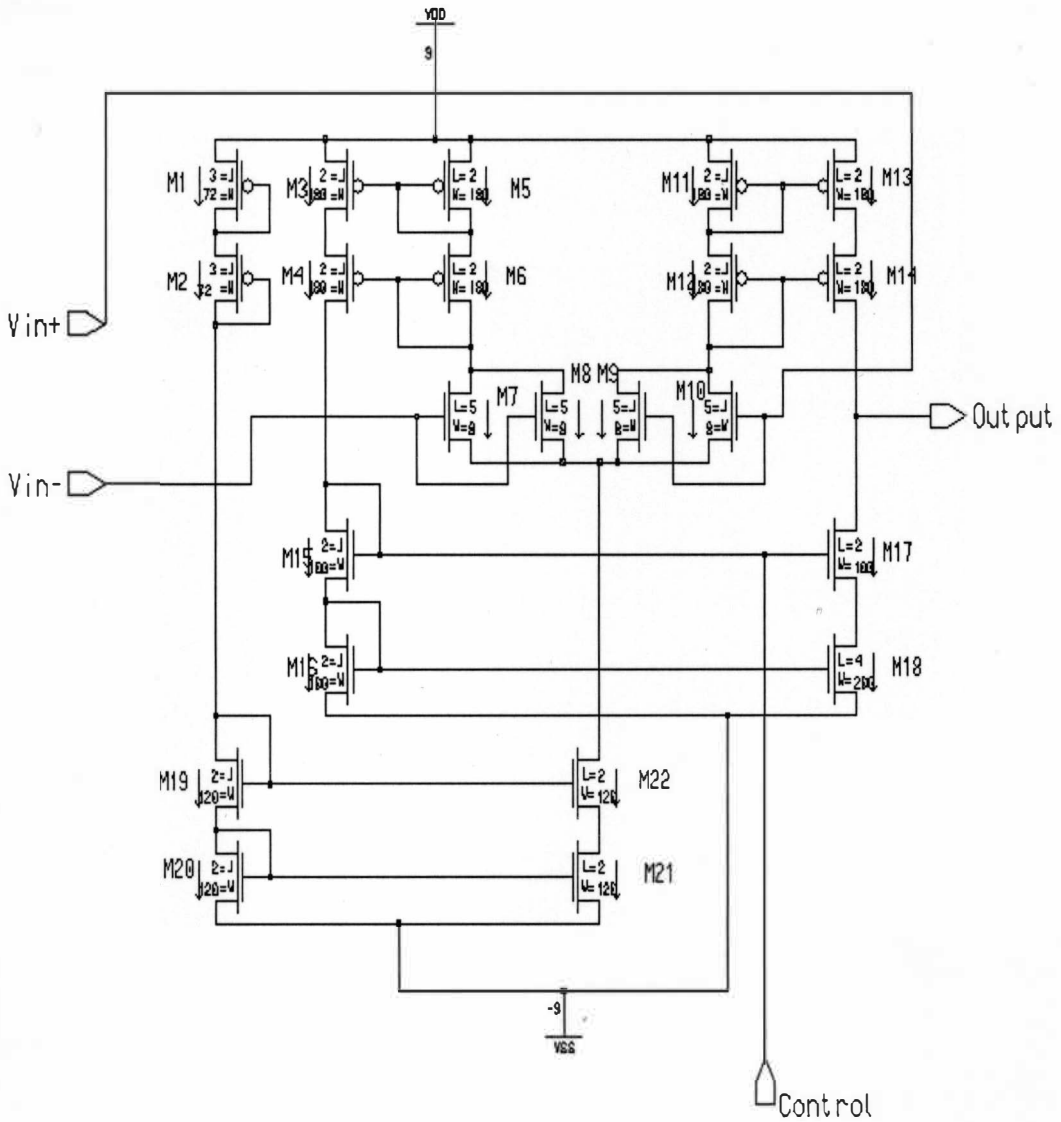


Figure 1. OTA Schematic.

6. Place VDD, VSS, port in, port out and GND from SDL palette menu. Then, wire up the components as shown in figure 1.

7. Before we can change any value and port name, you need to select properties. Do this by clicking on ***Set Select Filter***, then the ***Setup Select Filter*** box will show up. Click on ***Properties*** and leave others at defaults. Accept the box (Figure 2).

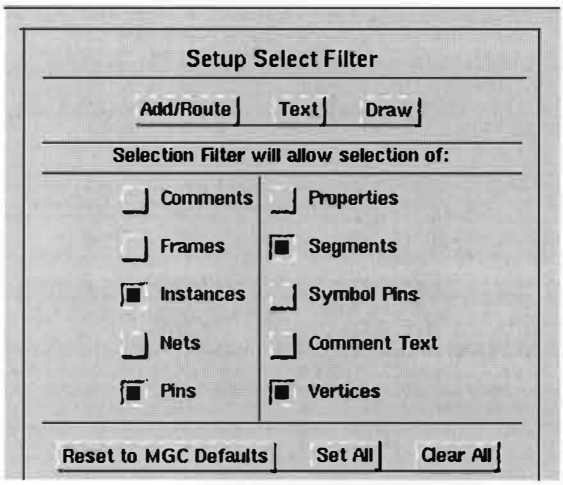


Figure 2. Setup Select Filter Box.

Now you can change value and port name by selecting ***Text*** in palette menu, then the ***Change value*** and ***Name Net*** box will occur at the left corner of screen.

8. Now to make sure that every device has been wired, you can do that by using check sheet operation. Do this by going to ***Check→Sheet→with defaults*** on menu bar. After passing this check, save the sheet.

Preparing Design for Functional Simulation.

Before running any simulation, the designs need to be prepared for simulation. If you want to simulate by QuickSIm II (digital), you need to type ***dsim_prep filename*** in your terminal, e.g.

> dsim_prep ota

In our design, we need to simulate by AccuSim II (analog). It can do by typing ***sdl_prep filename 2.0*** in your terminal e.g.

> sdl_prep ota 2.0

then the screen will show as below;

Simulation with AccuSim II

1. Invoke AccuSim II by entering ***accusim filename/sdl*** e.g.
   > accusim ota/sdl
2. Once Accusim is loaded, you should see your schematic. Then, you need to load model for FETs simulation. To load a model file, use ***File->Auxiliary Files->Load Model Library*** menu. You can enter the filename with your model in it. Use the navigator to load the file that you have created. The model

file (n91wbsim.mod) used in this simulation is based upon a specific MOSIS run named N91W.

3. To see the trace while it is progressing, select voltage or current or port out that want to see output in schematic window. Then click ***trace*** in palette menu (Figure 3). The graphs will show up with your selected signal in it.

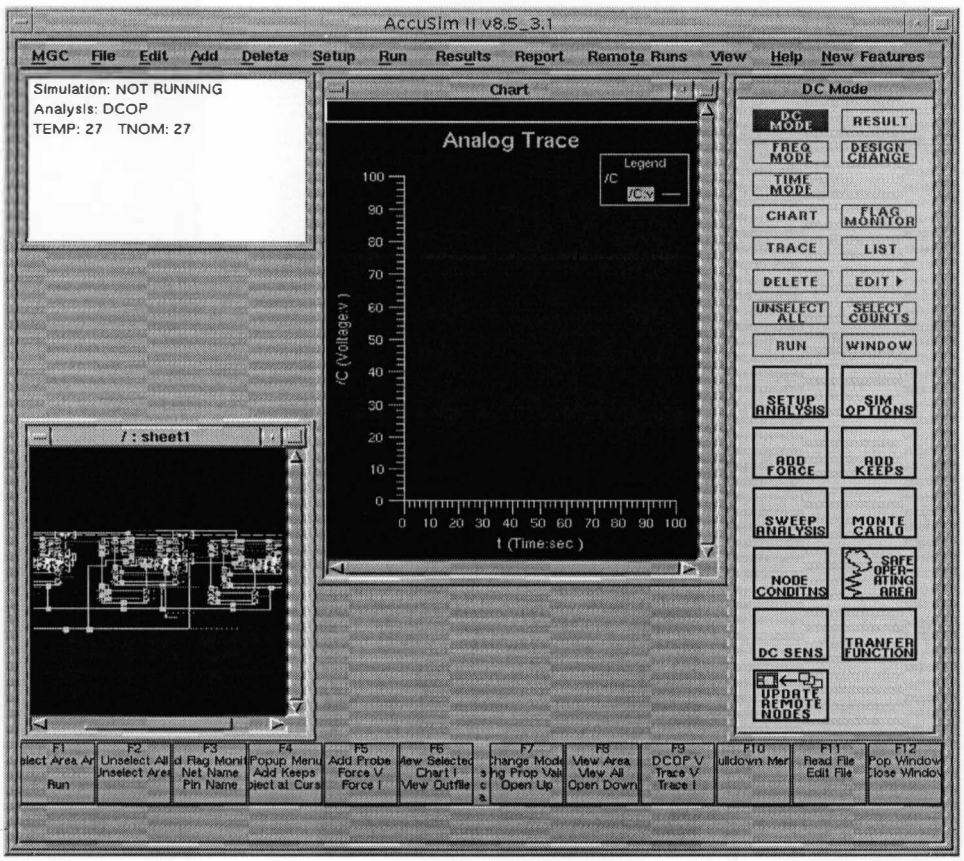


Figure 3. Accusim Window.

4. Set the analysis type by using the ***Setup Analysis*** icon. Since you need to perform DC sweep for OTA, you need to press ***DC sweep*** button to get the dialog box for setting up the DC sweep. Put the node for sweeping and GND for reference signal. Put range of swept voltage (Figure 4). However, when simulate Chua's circuit, the analysis need to be Transient and the initial voltages have to be set. The initial value can set by clicking button under ***Use Initial Conditions (-UIC)*** and click on ***Setup***. Then, the ***Guess/IC/Nodeset*** box will show. Select ***Name*** button and put node name, voltage and set initial as figure 5.

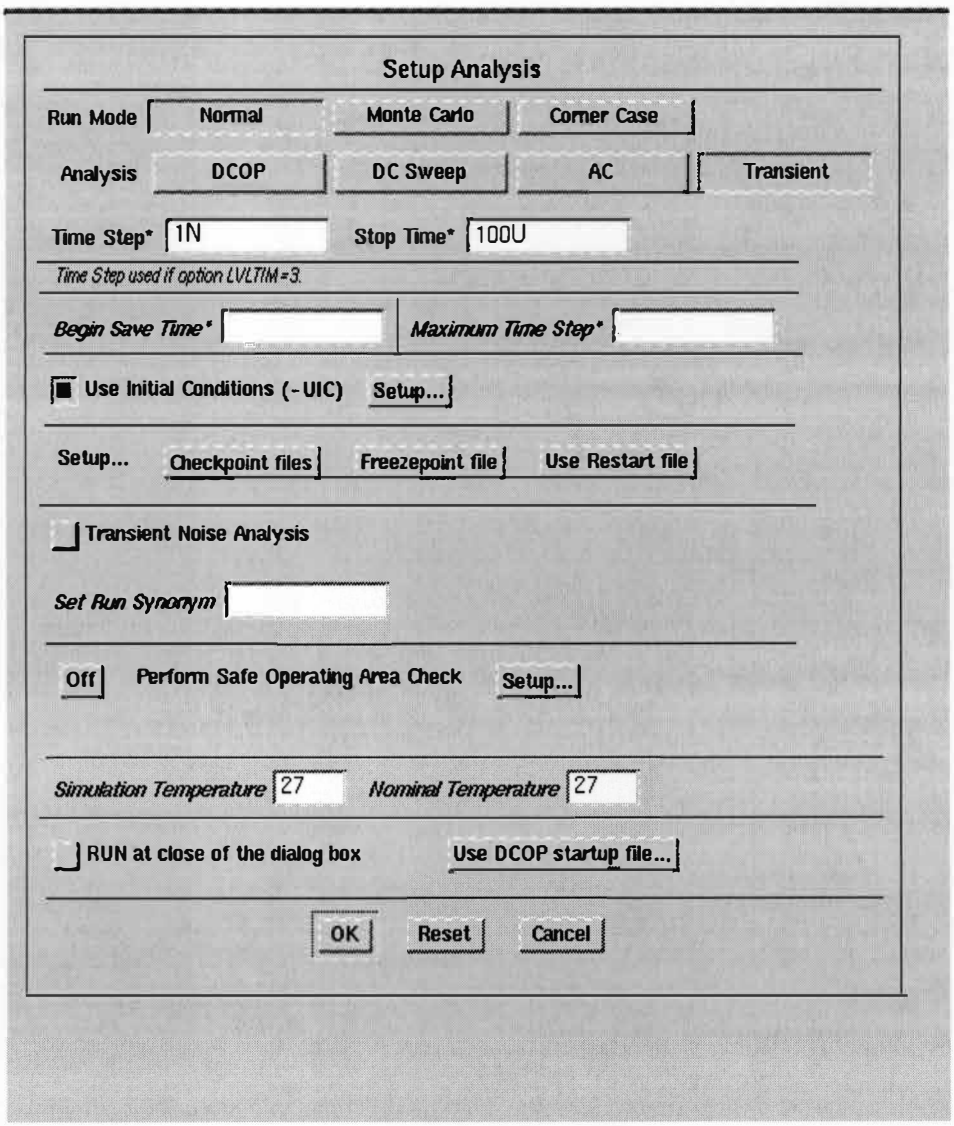


Figure 4. Setup Analysis Window.

5. Now click ***run*** in palette menu to run simulation (figure 3).
6. After simulation is complete, if you want to operate trace of signals such as adding two signals or plotting one signal versus the other signal, you click to X-axis of signal trace. Then click the right button of mouse. The menu will pop up. Select ***chart*** then the chart menu will show up. You can select any operation that you want (Figure 5).

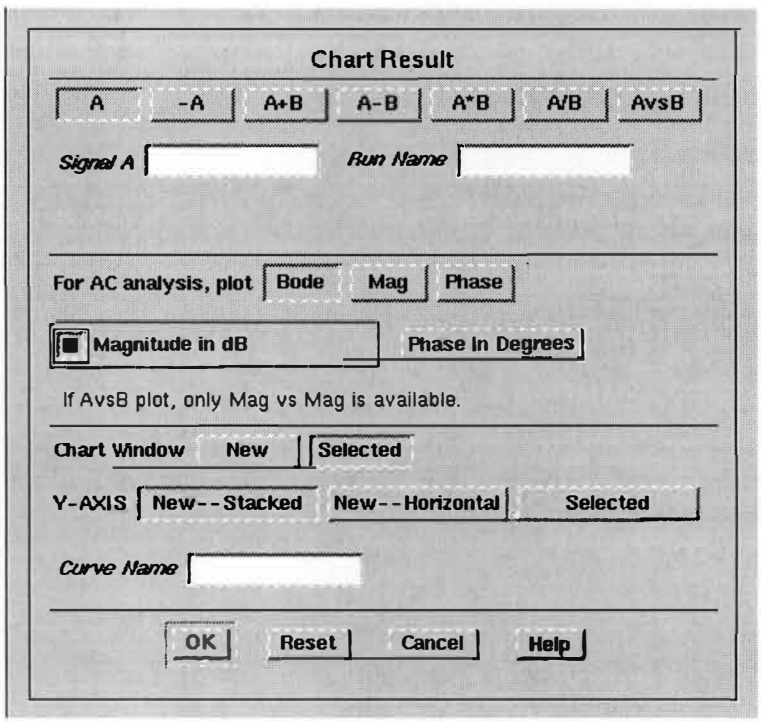


Figure 5. Chart Result Box.

7. Once your simulation is working properly, save your setup for use later. Do this via the ***File->Simulation->Save Setup*** menu.

Do same procedures with Chua's circuit but use transient analysis and set initial voltage condition for V1, V2, and V3. If you don't set initial condition for voltage, the chaotic signal will never occur.

Layout

1. Invoke IC Station by entering
   > ic &
2. Once the window is shown up, you may need to set up the environment for easier use. Using the ***MGC->Setup->Session*** menu. You may select Up Down Tiling or Left Right Tiling in Window Layout as show in figure 6. Leave everything else at the default.

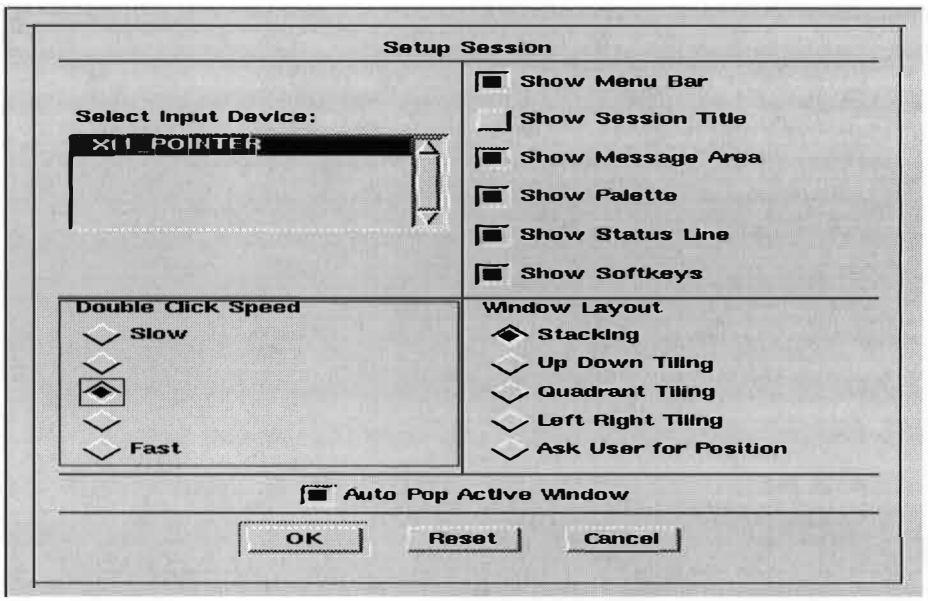


Figure 6. Setup Session Box.

3. Now we need to create new cell. Use the ***Cell→Create*** option on the palette menu or use the ***File→Cell→Create*** menu to do this. Enter file name in cell name box. Then, select ***CE (Connectivity editing mode)*** under ***Connectivity Mode*** (Figure 7). This will allow you to keep the connectivity information between your layout and schematic. Select ***EDDM*** button under Logic Source type and leave everything else blank.

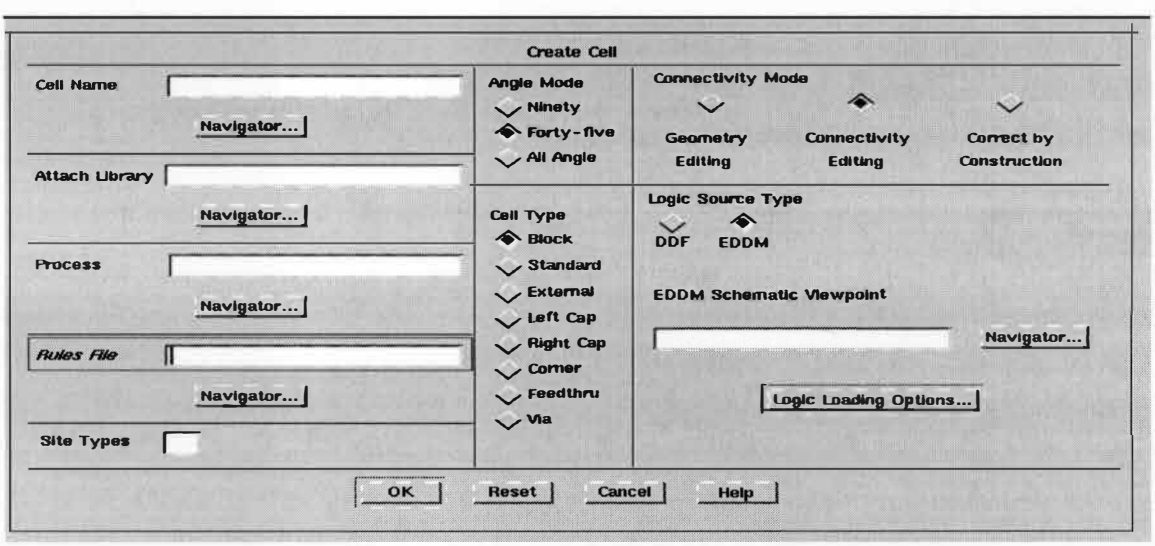


Figure 7. Create Cell Window.

4. Once the empty cell has been opened, you need to set logic source for your cell. To do this, go to the SDL menu via the ***SDL*** button on the palette menu. Under Logic, select ***Set*** and enter the schematic name followed by "/sdl" e.g.

ota/sdl. You can use navigator to select the viewpoint. Then open the schematic by going to ***Open button***. The schematic window will show up. Be sure to select the correct viewpoint for if you don't, the tools will not able to recognize your transistors.

5. At this point, you will have two windows. One is a cell that is empty. The other is a logic source that has your schematic design. Now you can place devices in your cell. Before you do that your cell has to be active. If it is not, click on window to make it active. The device can be placed in two different ways. One is Use Diffusion Sharing so that the ICgraph will automatically merge series and parallel transistors. The other is Don't Use Diffusion Sharing that will place transistors individually. For our OTAs and Chua's circuit, we will use Don't Use Diffusion Sharing. Do this by go to **MDK** menu and select ***Don't Use Diffusion Sharing***.
6. Now you can place the devices into your cell. To do this, click on ***A Int*** under the schematic section of the palette menu (Figure 8). At this point, tools will generate the dimension of device based on the width and length parameters specified on the instances and place into the open cell. Overflow lines (in yellow) will show you the connectivity points in your circuit. These overflows will disappear when you have made the correct connection.

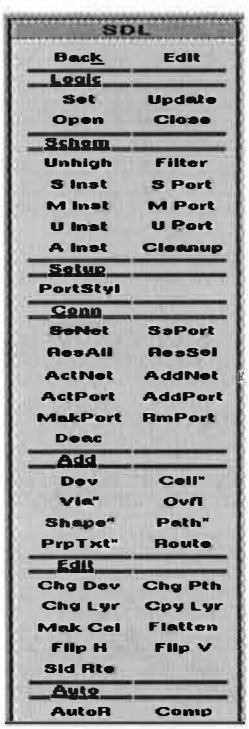


Figure 8. SDL Palette Menu.

7. Now you can wire up the devices. Between wiring, you may need to undo several times. It is very helpful to change the default undo level (three) to a higher value so you can undo more operations. To do this, go to ***Setup→IC***

menu, then change undo level. You may need names of instances while wiring. Do this by turn on name under ***Port/Pin Name Display*** in Setup IC menu as show in figure 9.

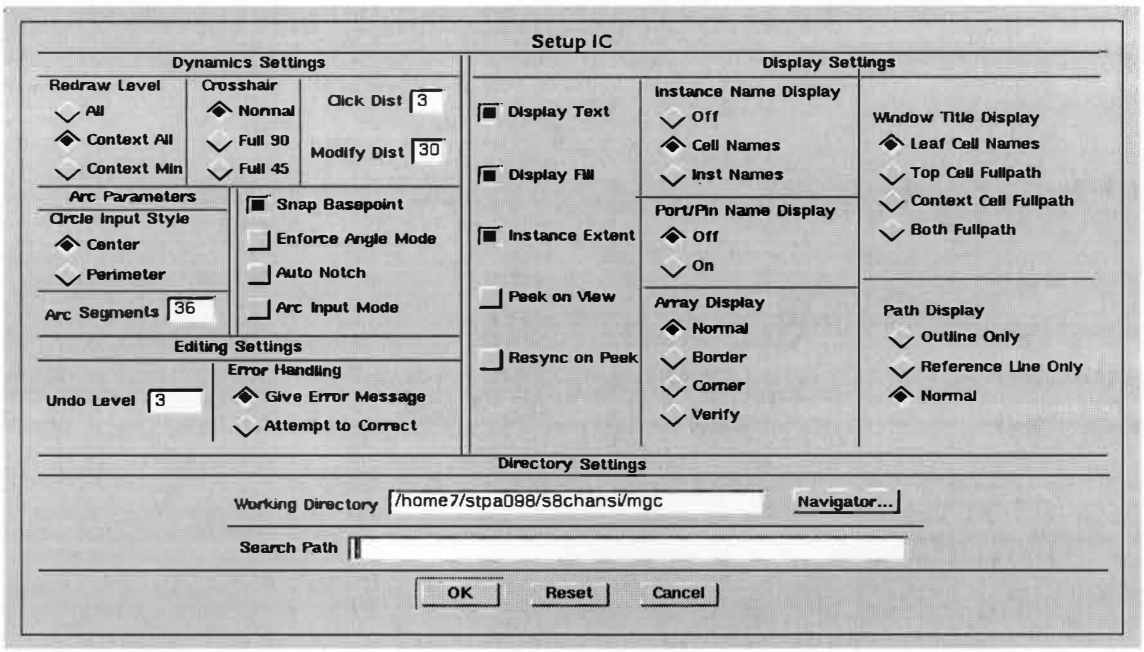


Figure 9. Setup IC Window.

8. Since the routes cannot be only one layer, it needs to use different types of layers such as METAL1, METAL2 and POLY. The layer palette will make it easier. To do this, type ***sho la p*** (This stands for "show layer palette"). Now you can select layers that need to use for routing. For our design, we need METAL1 and METAL2 for source/drain routing , POLY for gate routing, ELECTRODE for capacitors, VIA for contacting METAL1 and METAL2, CONTACT_TO_POLY for contacting POLY and METAL1 and CONTACT_TO_ELECTRODE for contacting ELECTRODE and METAL1. The layer palette will show on upper right corner.
9. Wiring up devices has many ways. For us, we will use ***Path*** in the Add menu or under Easy Edit menu. When you click ***Path***, then the ***ADD PA*** box will pop up on bottom left corner. Select the ***Option*** button to enter width layer as shown in figure 10. Selecting the Keep Option Settings box and exit the dialog box. For our design, we use the width of POLY for 2 micron, of METAL1 for 3 and 4 micron and of METAL2 for 3 and 4 micron. Now you can place layer paths.

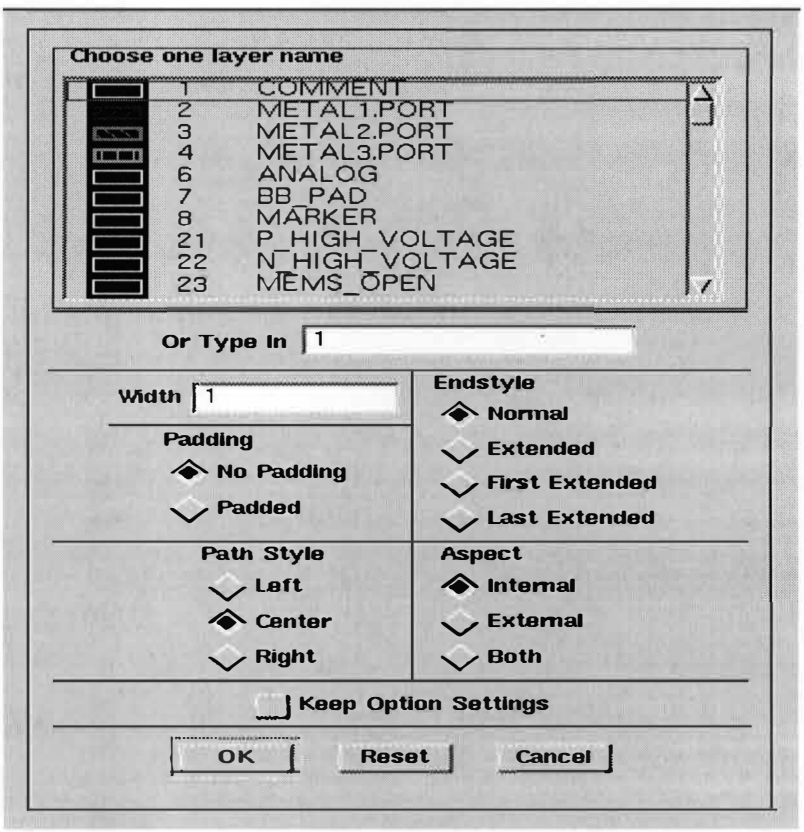


Figure 10. Layer Option Box.

10. Since the different layer can not connect directly, you need to have special layer to connect such as VIA.
    - For connecting METAL1 and METAL2, you need to create 2x2 via, 4x4 METAL1 layer and 4x4 METAL2 layer. Do this by using Shape button in palette menu. The dimension of shape will show on top of cell widow.
    - For connecting POLY and METAL1, you need 5x5 POLY layer, 5x5 METAL1 layer and 2x2 POLY_TO_CONTACT layer.
    - For connecting POLY and METAL2, you need to have METAL1 for connecting because POLY layer can not connect to METAL2 directly. Create 5x5 POLY layer, 2x2 POLY_TO_CONTACT layer and 5x5 METAL1 layer. Then routing POLY layer and METAL1 layer to this connection. Next, create 4x4 METAL2, 4x4 METAL1 and 2x2 VIA and route them.

11. Once the gates, sources and drains are wired up, you need to place the ports for inputs and outputs from your schematic. Click ***PortStly*** on the Setup palette menu as shown in figure 8. You should select ***Process Port*** on the dialog box to display the ports defined for this process (Figure 11)

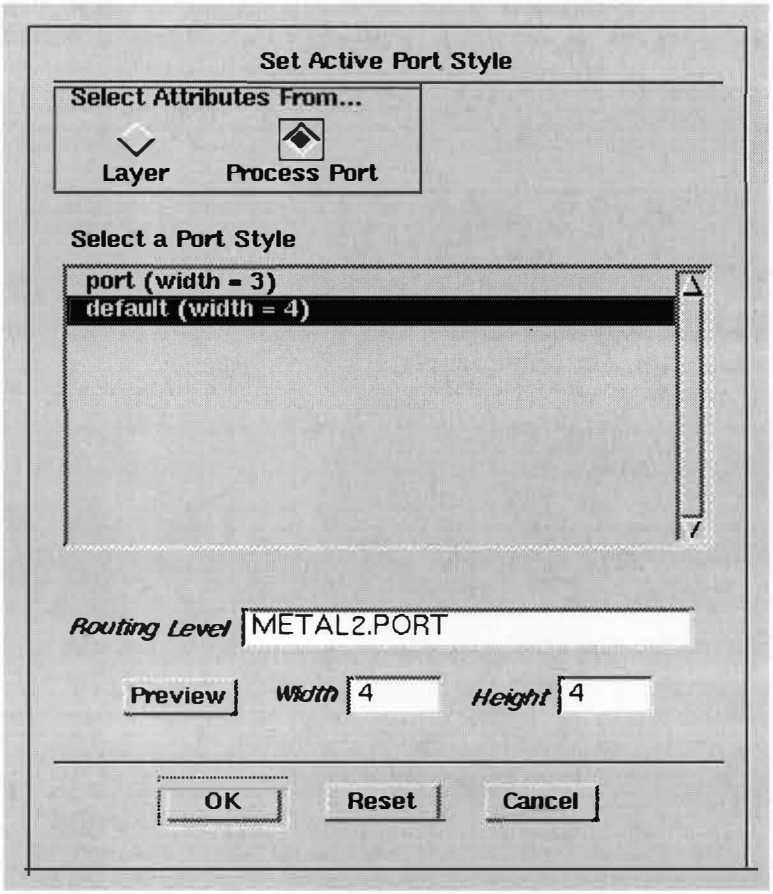


Figure 11. Set Active Port Style Box.

12. We will use METAL2 for ports. Select ***the default*** line and then click on ***Preview*** to see its parameters. Notice that it is on METAL2 and it is 4x4 microns as figure 11.
13. To place ports, click on ***M Port I*** under Schem menu (Figure 8). All nets with a port are selected and a port shape is created and placed. Then you can are prompted to move these ports to where you want.
14. All ports are on METAL2, but the power and ground ports should really be on METAL1. In addition, the size for these ports should be changed so they stretch the full length of the cell.
    a. Change port layer by selecting the VDD and VSS ports and then using the ***Objects →Change →Layer*** menu to move them to METAL1.
    b. Resize the ports by ***Stretching*** them to the desired width and leave them as 4 microns high.
15. You need to change the *direction* of all ports that are not inputs. This is because the port placement routine forces all ports to be IN. Power ports you can ignore but for the output, you need to change its direction to OUT. To do

this, use the ***Object→Change→Port*** menu to change the direction to OUT and make sure the type is ***Signal***. Leave all other items alone. Wire up all ports.

16. Now you need to place the diffusion contacts. In MDK package, they have two contact cells. These are available in *$MGC_HEP/tutorial/sdl/cells* called nwell_contact and pwell_cotact. Get these contacts and abut them to the MOS devices in the layout. Route nwell_contact with VDD and pwell_contact with VSS.
17. Now the layout needs to check by DRC. To do this, go back to the Session palette and then select ***ICrules***. Do a ***check*** of your circuit and then use the scan menu items to locate the errors. If there are any error, you need to fix all DRC errors before saving cell and going to next step.

IC Extraction and Backannotation

1. Before the extraction can be run, your layout must match your schematic. LVS will check this for you. To do this, you select the ***Ictrace (M)*** palette menu. This is mask-based LVS checking. It will ignore all hierarchy and look only at the actual connectivity of your devices.
2. In the Ictrace menu, select the ***LVS*** item to bring up LVS dialog box shown in figure 12.

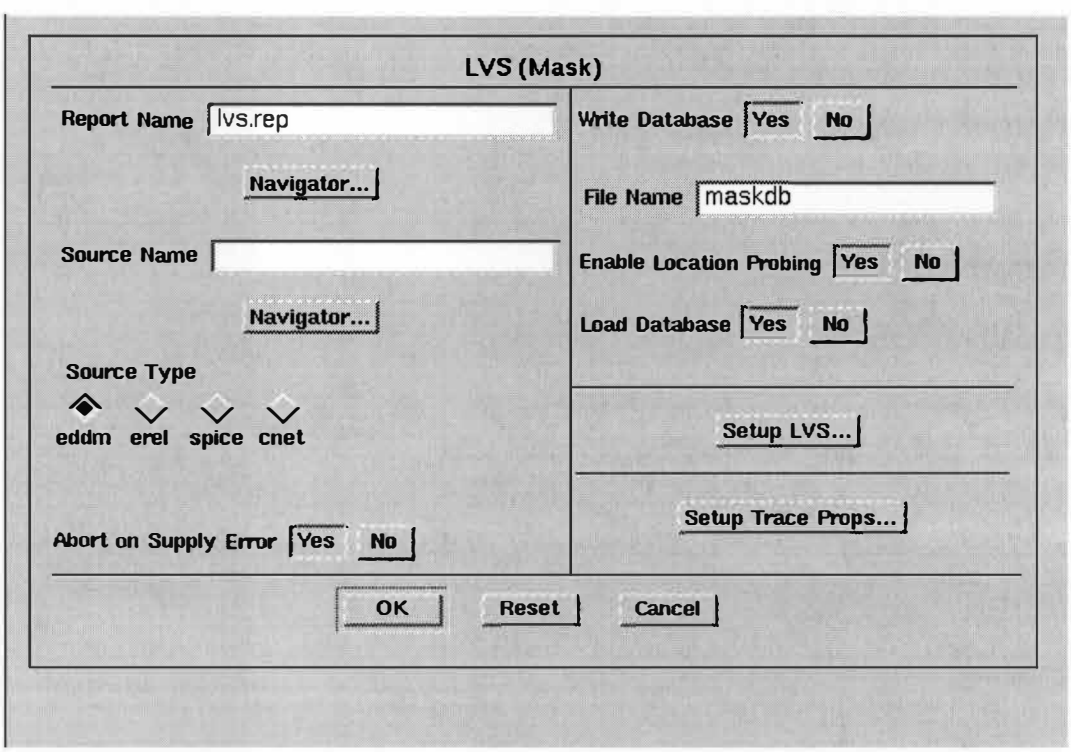


Figure 12. LVS Mark Box.

3. You will need to supply the schematic source name. Use navigator or type in the source name including the viewpoint. If you use the wrong viewpoint, LVS will fail.
4. Then, press the ***Setup LVS*** button to setup the LVS procedure. The dialog box will be brought up. Leave everything alone except you need to turn the ***Recognize Gates*** option off. If you do not, then LVS will try to combine transistors into gates and then try to match those gates up against similar gates in your schematic.
5. Press ***OK*** for Setup dialog box and the LVS dialog box and then LVS will begin. When LVS is complete, you should look at the report by using ***Report→LVS*** item from the LVS palette. A text window will appear displaying the report. Be sure is compared correctly. If it did not, you will need to fix any errors before extraction will work.
6. Once the layout pass LVS, the layout is ready to backannotated parasitic for simulation. We need to do lumped extraction. Lumped extraction will treat each distinct net as one lumped capacitor and/or resistor. Every point on the net will see the full extracted RC delays, therefore. Hence, a transmission line will look the same so matter where you are on that transmission line.
7. To prepare for extraction, be sure your cell is reserved for edit, Go to ***ICextract (M)*** palette menu. Select ***Lumped*** from the palette menu to display the extraction dialog box shown in figure 13.

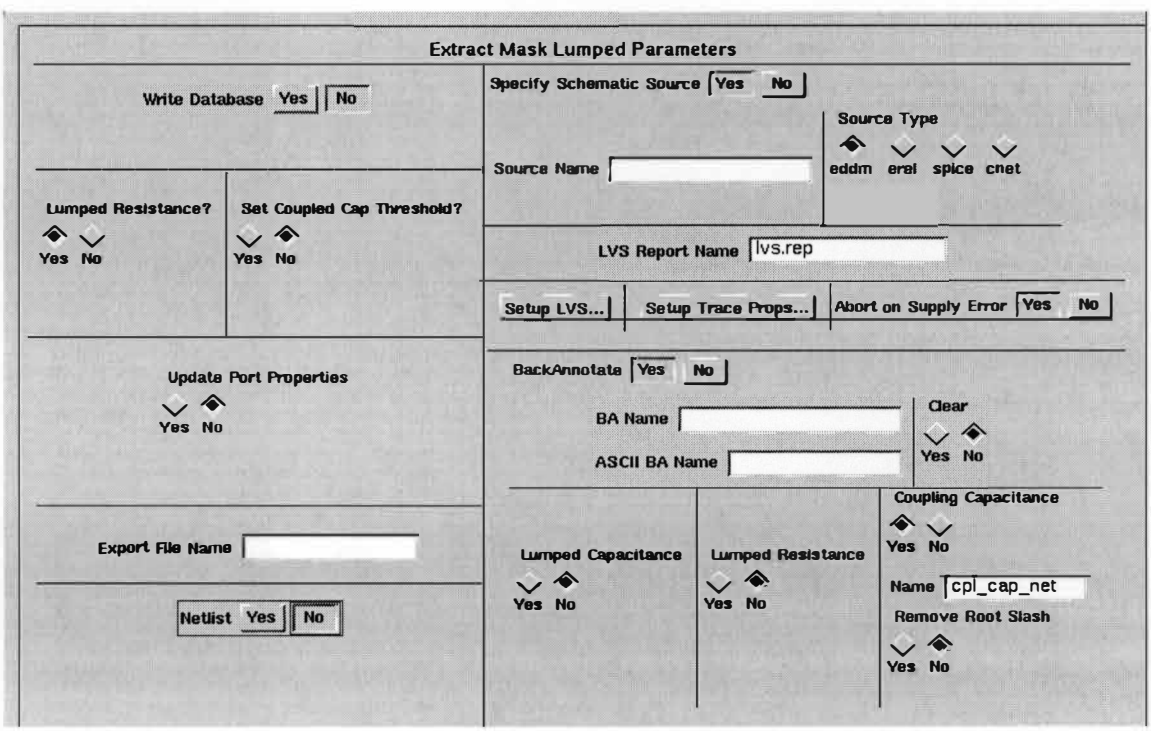


Figure 13. Extract Mask Lumped Parameters Box.

8. Click ***Yes*** to the right of the ***Specify Schematic Source*** to show schematic source. Enter the source name followed by "/sdl" e.g ota/sdl.
9. Click on the Setup LVS…button and check to be sure that the recognize gates option is set to ***NO***. Accept this box.
10. Select ***YES*** in the ***BackAnnotate*** option for backannotation results.
11. Specify the name of a BA file to use. If you choose a previously used name, then you should also select the ***YES*** button under the Clear option to remove any previous annotation.
12. Now select the parameters to backannotated. Accusim will use the ***cpl_cap_net*** property for net capacitance between node and any others. To do this, select ***Yes*** button under ***Coupling Capacitance***. The lumped capacitance can also be used but only you are using GND as opposed to VSS and you change the property name to *cap_net* form the default *icap_net*. For our backannotaion, we don't need to use lumped capacitance. So, select ***No*** button. In addition, Lumped resistance is not used in Accusim.
13. Accept this dialog box and extract will begin. When the extract is done, you will see that your schematic is automatically updated and you will see annotations (red number) on it as shown in figure 14.

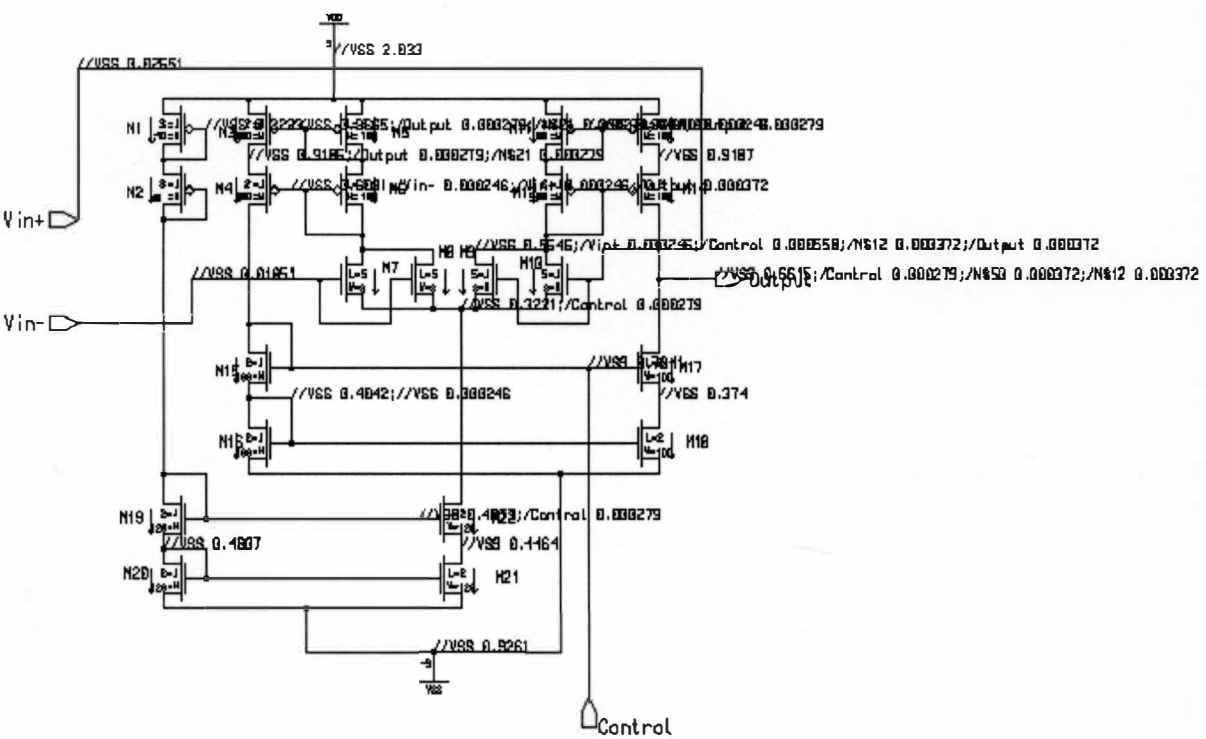


Figure 14. Schematic with Extracted Parasitic.

Post Layout Simulation

1. You can do post simulation the same when your do simulation using Accusim. Type file name to start Accusim e.g. accusim ota/sdl. This will load your schematic with the backannotated lumped resistance and capacitance.
2. You can do the set up in Accuim the same as you did before and see the result. The result should not look much different that your functional simulation because there is not much added capacitance nor resistance the layout.

DRC Report for Chua's Circuit.

```
RULECHECK                    RESULTS              TEXT
                         ORIG   CURR   SCAN
================================================================================
bad_active_area             0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:37 1999                          Active area must be covered by a select
--------------------------------------------------------------------------------
bad_contact_poly            0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:37 1999                          Contact to poly must consist of poly,
CONTACT_TO_POLY, and METAL1
--------------------------------------------------------------------------------
bad_contact_ELECTROD        0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:37 1999                          Contact to ELECTRODE must consist of
ELECTRODE, CONTACT_TO_ELECTRODE, and METAL1
--------------------------------------------------------------------------------
bad_contact_active          0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:37 1999                          Contact to active must consist of active,
CONTACT_TO_ACTIVE, and METAL1
--------------------------------------------------------------------------------
bad_contact_gate            0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:37 1999                          Contact to poly may not be on gate region.
--------------------------------------------------------------------------------
bad_via                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:37 1999                          Via must consist of METAL1, via, and METAL2
--------------------------------------------------------------------------------
bad_contact_via             0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:37 1999                          Via must NOT be stacked with contact
--------------------------------------------------------------------------------
select_overlap              0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:37 1999                          Overlap of N+ and P+ not allowed
--------------------------------------------------------------------------------
bad_nwell                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:37 1999                          Nwell must have well contact
--------------------------------------------------------------------------------
bad_psubstrate              0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                          Psubstrate must have a substrate contact
--------------------------------------------------------------------------------
bad_pgate                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                          P-type gate must not be in psubstrate
--------------------------------------------------------------------------------
bad_ngate                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                          N-type gate must not be in nwell
--------------------------------------------------------------------------------
DRC1_1                      0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                          N-Well width = 10L
--------------------------------------------------------------------------------
DRC1_2                      0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                          N-well spacing (different potential) = 9L
--------------------------------------------------------------------------------
DRC2_1                      0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                          Active area width = 3L
```

```
--------------------------------------------------------------------------------
DRC2_2                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      Active area spacing = 3L
--------------------------------------------------------------------------------
DRC2_3                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      Source/Drain Active to Well Edge = 5L
--------------------------------------------------------------------------------
DRC2_4                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      Substrate/Well Contact, Active to Well Edge
= 3L
--------------------------------------------------------------------------------
DRC3_1                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      Poly width = 2L
--------------------------------------------------------------------------------
DRC3_2                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      Poly spacing = 2L
--------------------------------------------------------------------------------
DRC3_3                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      Gate poly overlap of active = 2L
--------------------------------------------------------------------------------
DRC3_4                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      Active overlap of gate poly = 3L
--------------------------------------------------------------------------------
DRC3_5                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      Field poly to active = 1L
--------------------------------------------------------------------------------
DRC4_1_n                  0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      N+ select overlap of channel to gate poly =
3L
--------------------------------------------------------------------------------
DRC4_1_p                  0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      P+ select overlap of channel to gate poly =
3L
--------------------------------------------------------------------------------
DRC4_2                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      Select overlap of active = 2L
--------------------------------------------------------------------------------
DRC4_3_p                  0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:38 1999                      P+ select overlap of contact to well = 1L
--------------------------------------------------------------------------------
DRC4_3_n                  0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:39 1999                      N+ select overlap of contact to well = 1L
--------------------------------------------------------------------------------
DRC4_4_p_width            0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:40 1999                      P+ select width = 2L
--------------------------------------------------------------------------------
DRC4_4_p_space            0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:40 1999                      P+ select space = 2L
--------------------------------------------------------------------------------
DRC4_4_n_width            0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:40 1999                      P+ select width = 2L
--------------------------------------------------------------------------------
DRC4_4_n_space            0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:40 1999                      N+ select space = 2L
```

```
--------------------------------------------------------------------------------
DRC5A_1                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:40 1999                       Contact to poly size exactly 2L X 2L
--------------------------------------------------------------------------------
DRC5A_2                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:40 1999                       Poly overlap for contact = 1.5L
--------------------------------------------------------------------------------
DRC5A_3                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:40 1999                       Contact to poly spacing = 2L
--------------------------------------------------------------------------------
DRC6A_1                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:40 1999                       Contact to active exactly 2L X 2L
--------------------------------------------------------------------------------
DRC6A_2                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:40 1999                       Active overlap for contact = 1.5L
--------------------------------------------------------------------------------
DRC6A_3                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:41 1999                       Contact to active spacing = 2L
--------------------------------------------------------------------------------
DRC6A_4                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:42 1999                       Contact to active space to gate of
transistor = 2L
--------------------------------------------------------------------------------
DRC7_1                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:43 1999                       Metal1 width = 3L
--------------------------------------------------------------------------------
DRC7_2                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:43 1999                       Metal1 spacing = 3L
--------------------------------------------------------------------------------
DRC7_3                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:43 1999                       Metal1 overlap of contact to poly = 1L
--------------------------------------------------------------------------------
DRC7_4                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:43 1999                       Metal1 overlap of contact to active = 1L
--------------------------------------------------------------------------------
DRC8_1                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:45 1999                       Via size exactly 2L X 2L
--------------------------------------------------------------------------------
DRC8_2                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:45 1999                       Via spacing = 3L
--------------------------------------------------------------------------------
DRC8_3                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:45 1999                       Via overlap by METAL1 = 1L
--------------------------------------------------------------------------------
DRC8_4                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:45 1999                       Via space to poly or active edge = 2L
--------------------------------------------------------------------------------
DRC8_5                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:45 1999                       Via spacing to contact = 2L
--------------------------------------------------------------------------------
DRC9_1                     0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                       Metal2 width = 3L
```

```
--------------------------------------------------------------------------------
DRC9_2                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        Metal2 spacing = 4L
--------------------------------------------------------------------------------
DRC9_3                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        Metal2 overlap of via = 1L
--------------------------------------------------------------------------------
DRC11_1                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        ELECTRODE width = 3L
--------------------------------------------------------------------------------
DRC11_2                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        ELECTRODE spacing = 3L
--------------------------------------------------------------------------------
DRC11_3                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        Poly overlap of ELECTRODE = 2L
--------------------------------------------------------------------------------
DRC11_4                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        ELECTRODE spacing to active or well = 2L
--------------------------------------------------------------------------------
DRC11_5                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        ELECTRODE spacing to Contact to Poly = 3L
--------------------------------------------------------------------------------
DRC11_sel                 0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        Capacitor and Select may not intersect
--------------------------------------------------------------------------------
DRC12_1                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        ELECTRODE width = 2L
--------------------------------------------------------------------------------
DRC12_2                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        ELECTRODE spacing = 3L
--------------------------------------------------------------------------------
DRC13_1                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        Contact to ELECTRODE size exactly 2L X 2L
--------------------------------------------------------------------------------
DRC13_2                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        Contact to ELECTRODE spacing = 2L
--------------------------------------------------------------------------------
DRC13_3                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        ELECTRODE overlap for contact = 3L ON CAP
PLATE
--------------------------------------------------------------------------------
DRC13_4                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        ELECTRODE overlap for contact = 2L NOT ON
CAP PLATE
--------------------------------------------------------------------------------
DRC13_5                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        Contact to ELECTRODE space to Poly or
Active = 3L
--------------------------------------------------------------------------------
DRC14_1                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:46 1999                        Via2 size exactly 2L X 2L
--------------------------------------------------------------------------------
DRC14_2                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                        Via2 spacing = 3L
```

```
--------------------------------------------------------------------------------
DRC14_3                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Via2 overlap by METAL2 = 1L
--------------------------------------------------------------------------------
DRC14_4                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Via2 spacing to via = 2L
--------------------------------------------------------------------------------
DRC15_1                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Metal3 width = 6L
--------------------------------------------------------------------------------
DRC15_2                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Metal3 spacing = 4L
--------------------------------------------------------------------------------
DRC15_3                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Metal3 overlap of via2 = 2L
--------------------------------------------------------------------------------
DRC16_1                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Analog Contact to active exactly 2L X 2L
--------------------------------------------------------------------------------
DRC16_2                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum select overalp of emitter contact =
3L
--------------------------------------------------------------------------------
DRC16_3                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum pbase overalp of emitter select =
2L
--------------------------------------------------------------------------------
DRC16_4                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum spacing between emitter select and
base select = 4L
--------------------------------------------------------------------------------
DRC16_5                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum pbase overlap of base contact = 2L
--------------------------------------------------------------------------------
DRC16_6                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum select overlap of base contact = 2L
--------------------------------------------------------------------------------
DRC16_7                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum nwell overlap of pbase = 6L
--------------------------------------------------------------------------------
DRC16_8                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum spacing between pbase and collector
= 4L
--------------------------------------------------------------------------------
DRC16_9                    0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum active overlap of collector contact
= 2L
--------------------------------------------------------------------------------
DRC16_10                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum nwell overlap of collector active =
3L
--------------------------------------------------------------------------------
DRC16_11                   0      0      0  Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 20 02:37:47 1999                         Minimum select overlap of collector active
= 2L
```

DRC Report for Padframe.

RULECHECK RESULTS TEXT
ORIG CURR SCAN
==========
bad_active_area 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Active area must be covered by a select
---
bad_contact_poly 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Contact to poly must consist of poly,
CONTACT_TO_POLY, and METAL1
---
bad_contact_ELECTROD 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Contact to ELECTRODE must consist of ELECTRODE,
CONTACT_TO_ELECTRODE, and METAL1
---
bad_contact_active 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Contact to active must consist of active,
CONTACT_TO_ACTIVE, and METAL1
---
bad_contact_gate 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Contact to poly may not be on gate region.
---
bad_via 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Via must consist of METAL1, via, and METAL2
---
bad_contact_via 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Via must NOT be stacked with contact
---
select_overlap 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Overlap of N+ and P+ not allowed
---
bad_nwell 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Nwell must have well contact
---
bad_psubstrate 6 6 6 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:55:59 1999 Psubstrate must have a substrate contact
---
bad_pgate 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules

Oct 19 14:56:00 1999 P-type gate must not be in psubstrate

---

bad_ngate 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 N-type gate must not be in nwell

DRC1_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 N-Well width = 10L

DRC1_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 N-well spacing (different potential) = 9L

DRC2_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 Active area width = 3L

DRC2_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 Active area spacing = 3L

DRC2_3 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 Source/Drain Active to Well Edge = 5L

DRC2_4 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 Substrate/Well Contact, Active to Well Edge = 3L

DRC3_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 Poly width = 2L

DRC3_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 Poly spacing = 2L

DRC3_3 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 Gate poly overlap of active = 2L

DRC3_4 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 Active overlap of gate poly = 3L

DRC3_5 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:00 1999 Field poly to active = 1L

DRC4_1_n 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules

Oct 19 14:56:00 1999 N+ select overlap of channel to gate poly = 3L

DRC4_1_p 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:01 1999 P+ select overlap of channel to gate poly = 3L

DRC4_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:01 1999 Select overlap of active = 2L

DRC4_3_p 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:01 1999 P+ select overlap of contact to well = 1L

DRC4_3_n 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:01 1999 N+ select overlap of contact to well = 1L

DRC4_4_p_width 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:02 1999 P+ select width = 2L

DRC4_4_p_space 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:02 1999 P+ select space = 2L

DRC4_4_n_width 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:02 1999 P+ select width = 2L

DRC4_4_n_space 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:02 1999 N+ select space = 2L

DRC5A_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:02 1999 Contact to poly size exactly 2L X 2L

DRC5A_2 680 680 680 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:02 1999 Poly overlap for contact = 1.5L

DRC5A_3 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:02 1999 Contact to poly spacing = 2L

DRC6A_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:02 1999 Contact to active exactly 2L X 2L

DRC6A_2 3368 3368 3368 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules

Oct 19 14:56:02 1999 Active overlap for contact = 1.5L

DRC6A_3 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:05 1999 Contact to active spacing = 2L

DRC6A_4 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:06 1999 Contact to active space to gate of transistor = 2L

DRC7_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:07 1999 Metal1 width = 3L

DRC7_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:07 1999 Metal1 spacing = 3L

DRC7_3 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:07 1999 Metal1 overlap of contact to poly = 1L

DRC7_4 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:07 1999 Metal1 overlap of contact to active = 1L

DRC8_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:08 1999 Via size exactly 2L X 2L

DRC8_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:08 1999 Via spacing = 3L

DRC8_3 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:08 1999 Via overlap by METAL1 = 1L

DRC8_4 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:09 1999 Via space to poly or active edge = 2L

DRC8_5 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:09 1999 Via spacing to contact = 2L

DRC9_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Metal2 width = 3L

DRC9_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules

Oct 19 14:56:10 1999 Metal2 spacing = 4L

DRC9_3 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Metal2 overlap of via = 1L

DRC11_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 ELECTRODE width = 3L

DRC11_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 ELECTRODE spacing = 3L

DRC11_3 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Poly overlap of ELECTRODE = 2L

DRC11_4 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 ELECTRODE spacing to active or well = 2L

DRC11_5 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 ELECTRODE spacing to Contact to Poly = 3L

DRC11_sel 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Capacitor and Select may not intersect

DRC12_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 ELECTRODE width = 2L

DRC12_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 ELECTRODE spacing = 3L

DRC13_1 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Contact to ELECTRODE size exactly 2L X 2L

DRC13_2 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Contact to ELECTRODE spacing = 2L

DRC13_3 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 ELECTRODE overlap for contact = 3L ON CAP PLATE

DRC13_4 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules

Oct 19 14:56:10 1999 ELECTRODE overlap for contact = 2L NOT ON CAP PLATE

DRC13_5 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Contact to ELECTRODE space to Poly or Active = 3L

DRC14_1 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Via2 size exactly 2L X 2L

DRC14_2 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Via2 spacing = 3L

DRC14_3 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Via2 overlap by METAL2 = 1L

DRC14_4 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Via2 spacing to via = 2L

DRC15_1 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Metal3 width = 6L

DRC15_2 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Metal3 spacing = 4L

DRC15_3 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Metal3 overlap of via2 = 2L

DRC16_1 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Analog Contact to active exactly 2L X 2L

DRC16_2 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum select overalp of emitter contact = 3L

DRC16_3 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum pbase overalp of emitter select = 2L

DRC16_4 0 0 0 Rule File Pathname: /home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum spacing between emitter select and base select = 4L

DRC16_5 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum pbase overlap of base contact = 2L

DRC16_6 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum select overlap of base contact = 2L

DRC16_7 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum nwell overlap of pbase = 6L

DRC16_8 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum spacing between pbase and collector =
4L

DRC16_9 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum active overlap of collector contact = 2L

DRC16_10 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum nwell overlap of collector active = 3L

DRC16_11 0 0 0 Rule File Pathname:
/home3/software/mentorgr/mgc_libs/gen_lib/mgc_hep/technology/ic/scmos.rules
Oct 19 14:56:10 1999 Minimum select overlap of collector active = 2L

LVS Report for Chua's Circuit.

```
################################################
##                                            ##
##     CALIBRE SYSTEM                       ##
##                                            ##
##       LVS REPORT                         ##
##                                            ##
################################################
```

REPORT FILE NAME: /home7/stpa098/s8chansi/mgc/lvs.rep
LAYOUT NAME: /home7/stpa098/s8chansi/mgc/chua/ch2
SOURCE NAME: /home7/stpa098/s8chansi/mgc/chua01/sdl
LVS MODE: Direct
ICGRAPH CONFIGURATION: Connectivity Editing (CE)
CREATION TIME: Mon Oct 18 19:51:59 1999
CURRENT DIRECTORY: /home7/stpa098/s8chansi/mgc
USER NAME: s8chansi

OVERALL COMPARISON RESULTS

```
  #     ####################
 #      #                  #
# #     #   CORRECT        #
 ##     #                  #
  #     ####################
```

Error: Different numbers of instances (see below).
Warning: Ambiguity points were found and resolved arbitrarily.

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	6	6	
Nets:	62	62	
Instances:	48	48	MN (3 pins)
	40	40	MP (3 pins)
	3	3 *	C (2 pins)
Total Inst:	91	91	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	6	6	
Nets:	62	62	
Instances:	40	40	MN (3 pins)
	40	40	MP (3 pins)
	3	3 *	C (2 pins)

Total Inst:	83	83

* = Number of objects in layout different from number in source.

****

LVS PARAMETERS

****

o LVS Setup:

Component Type Properties:	phy_comp element comp
Subtype Property:	model
Pin Name Properties:	phy_pin
Power Net Names:	VDD VSS
Ground Net Names:	ground
Ignore Ports:	NO
All Capacitor Pins Swappable:	NO
Reduce Parallel Mos Transistors:	YES
Recognize Gates:	NO
Reduce Split Gates:	YES
Reduce Parallel Bipolar Transistors:	YES
Reduce Series Capacitors:	YES
Reduce Parallel Capacitors:	YES
Reduce Series Resistors:	YES
Reduce Parallel Resistors:	YES
Reduce Parallel Diodes:	YES
Filter Unused Mos Transistors:	NO
Filter Unused Bipolar Transistors:	NO
Reverse WL:	NO
Property Resolution Maximum	50

o Numeric Trace Properties:

Component Type	Component Subtype	Source Property Name	Direct Property Name	Mask Property Name	Tole- rance	Trace
mn	instpar(w)	width	w	0%	NO	
mp	instpar(w)	width	w	0%	NO	
me	instpar(w)	width	w	0%	NO	
md	instpar(w)	width	w	0%	NO	
mn	instpar(l)	length	l	0%	NO	
mp	instpar(l)	length	l	0%	NO	
me	instpar(l)	length	l	0%	NO	
md	instpar(l)	length	l	0%	NO	
r	instpar(r)	resistance	r	0%	NO	
c	instpar(c)	capacitance	c	0%	NO	
d	Instpar(a)	area	a	0%	NO	
d	Instpar(p)	perimeter	p	0%	NO	

o Filter Properties:

Component Type	Component Subtype	Filter All	Property Name	String	Filter Constraint Nets	Short	Source	Layout	Direct	Mask
sch_filter_direct_open		YES				NO	YES	NO	YES	NO
sch_filter_direct_short		YES				YES	YES	NO	YES	NO
sch_filter_mask_open		YES				NO	YES	NO	NO	YES
sch_filter_mask_short		YES				YES	YES	NO	NO	YES
lay_filter_direct_open		YES				NO	NO	YES	YES	NO
lay_filter_direct_short		YES				YES	NO	YES	YES	NO

****

INFORMATION AND WARNINGS

****

Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type

Ports:	6	6	0	0	
Nets:	62	62	0	0	
Instances:	40	40	0	0	MN
	40	40	0	0	MP
	0	0	3	3	C
Total Inst:	80	80	3	3	

o Statistics:

16 parallel layout mos transistors were reduced to 8.
16 parallel source mos transistors were reduced to 8.

1 net was matched arbitrarily.

o Initial Correspondence Points:

Ports: VDD VSS ground V3 V2 V1

o Ambiguity Resolution Points:

(Each one of the following objects belongs to a group of indistinguishable objects.
The listed objects were matched arbitrarily by the Ambiguity Resolution feature of LVS.
Arbitrary matching may be prevented by assigning names to these objects or to adjacent nets).

Layout	Source
Nets	
9504	/N$3

****

SUMMARY

****

Total CPU Time: 0 sec
Total Elapsed Time: 0 sec

Appendix D

Technological Data From MOSIS

The description below is parametric test results for 2.0 micron technology. It contains parameters for both Spice and Mentor Graphic simulations.

Source: http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/supertex-scna20/n91w-params.txt

MOSIS PARAMETRIC TEST RESULTS

RUN: N91W VENDOR: ORBIT
TECHNOLOGY: SCNA20 FEATURE SIZE: 2.0 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: Orbit Semiconductor 2.0 um n-well.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3/2			
Vth		0.84	-0.88	Volts
SHORT	18/2			
Idss		166	-92	uA/um
Vth		0.78	-0.86	Volts
Vpt		10.0	-15.0	Volts
WIDE	50/2		-9.0	Volts
Ids0		0.1	-2.8	pA/um
LARGE	18/18			
Vth		0.81	-0.87	Volts
Vjbkd		14.7	-15.8	Volts
Ijlk		-26.2	-3.1	pA
Gamma		0.47	0.92	V^0.5
K' (Uo*Cox/2)		28.1	-10.1	uA/V^2

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	6/4			
Vth		0.84	-1.34	Volts
SHORT	12/4			
Vth		0.81	-1.32	Volts
LARGE	36/36			
Vth		0.80	-1.31	Volts
K' (Uo*Cox/2)		21.2	-6.2	uA/V^2

COMMENTS: XL_ORB_SCNA20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>16.4	<-14.2	Volts

BIPOLAR PARAMETERS	W/L	NPN	UNITS
2X1	2X1		
Beta		86	
V_early		69.6	Volts
Vce,sat		0.5	Volts
2X2	2X2		
Beta		77	
V_early		66.2	Volts
Vce,sat		0.2	Volts
2X4	2X4		
Beta		77	
V_early		62.0	Volts
Vce,sat		1.7	Volts
2X8	2X8		
Beta		75	
V_early		61.2	Volts
Vce,sat		1.1	Volts
BVceo		18.4	Volts
BVcbo		21.2	Volts
BVebo		8.4	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	N_WELL	UNITS
Sheet Resistance	30.1	61.3	21.5	21.6	0.06	0.03	2819	ohms/sq
Width Variation (measured - drawn)	0.04	-0.16	-0.43	-0.29	-0.27	-0.25		microns
Contact Resistance	12.2	38.2	7.2	7.3		0.05		ohms
Gate Oxide Thickness	406							angstroms

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	N_WELL	UNITS
Area (substrate)	138	313	55		23	12	23	aF/um^2
Area (N+active)			850	625	45	22		aF/um^2
Area (P+active)			844	621				aF/um^2
Area (poly)				462	41	19		aF/um^2
Area (poly2)					42			aF/um^2
Area (metal1)						31		aF/um^2
Fringe (substrate)	490	322			58	36		aF/um
Fringe (poly)					53	44		aF/um
Fringe (metal1)						56		aF/um
Overlap (N+active)			343					aF/um
Overlap (P+active)			453					aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.16	Volts
Vinv	1.5	2.39	Volts
Vol (100 uA)	2.0	0.25	Volts
Voh (100 uA)	2.0	4.69	Volts
Vinv	2.0	2.54	Volts
Gain	2.0	-9.21	
Ring Oscillator Freq.			
MOSIS (31-stage,5V)		36.62	MHz
DIV16 (31-stage,5V)		40.24	MHz

Ring Oscillator Power
DIV16 (31-stage,5V) 1.51 uW/MHz/g

N91W SPICE LEVEL3 PARAMETERS

```
.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08 XJ=0.200000U TPG=1
+ VTO=0.8093 DELTA=1.6500E+00 LD=4.1440E-07 KP=5.2580E-05
+ UO=618.2 THETA=5.3110E-02 RSH=1.5840E+01 GAMMA=0.4121
+ NSUB=3.7010E+15 NFS=5.9090E+11 VMAX=1.6760E+05 ETA=6.4270E-02
+ KAPPA=4.5740E-01 CGDO=5.2869E-10 CGSO=5.2869E-10
+ CGBO=3.4581E-10 CJ=1.4229E-04 MJ=6.2160E-01 CJSW=5.0307E-10
+ MJSW=2.4938E-01 PB=3.8328E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09
.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8460 DELTA=4.6140E-01 LD=4.9340E-07 KP=1.8388E-05
+ UO=216.2 THETA=1.0720E-01 RSH=5.1170E+01 GAMMA=0.5557
+ NSUB=6.7290E+15 NFS=5.9090E+11 VMAX=2.6220E+05 ETA=7.9790E-02
+ KAPPA=1.0000E+01 CGDO=6.2948E-10 CGSO=6.2948E-10
+ CGBO=3.8539E-10 CJ=3.1476E-04 MJ=5.7042E-01 CJSW=3.1623E-10
+ MJSW=2.4970E-01 PB=8.8539E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.6070E-07
```

N91W SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```
* DATE: Mar 24/99
* LOT: n91w                    WAF: 05
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27               TOX     = 4.06E-8
+XJ      = 2E-7         NCH     = 8E16             VTH0    = 0.7800861
+K1      = 1.3257304    K2      = -0.2663331       K3      = 3.3540235
+K3B     = -5.7456265   W0      = 1E-7             NLX     = 5.017841E-8
+DVT0W   = 0            DVT1W   = 5.3E6            DVT2W   = -0.032
+DVT0    = 0.8934518    DVT1    = 0.3510562        DVT2    = -0.3868226
+U0      = 695.2799467  UA      = 2.564957E-9      UB      = 1.028628E-19
+UC      = 4.805942E-11 VSAT    = 1.099499E5       A0      = 0.5000461
+AGS     = 0.1671009    B0      = 2.068932E-6      B1      = 3.876022E-6
+KETA    = -0.0241171   A1      = 0                A2      = 1
+RDSW    = 1.288299E3   PRWG    = -2.512952E-3     PRWB    = -2.015395E-7
+WR      = 1            WINT    = 2.001109E-7      LINT    = 4.393779E-7
+XL      = 0            XW      = 0                DWG     = -4.181007E-8
+DWB     = 9.275506E-8  VOFF    = -0.1050041       NFACTOR = 0.361228
+CIT     = 0            CDSC    = 1.506004E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 2.218414E-3      ETAB    = -9.030716E-4
+DSUB    = 5.04009E-3   PCLM    = 5.478981         PDIBLC1 = 0.4735148
+PDIBLC2 = 1.987973E-4  PDIBLCB = -1E-3            DROUT   = 0.3150364
+PSCBE1  = 4.176147E10  PSCBE2  = 1.217414E-6      PVAG    = 1.7815725
+DELTA   = 0.01         MOBMOD  = 1                PRT     = 0
+UTE     = -1.5         KT1     = -0.11            KT1L    = 0
+KT2     = 0.022        UA1     = 4.31E-9          UB1     = -7.61E-18
+UC1     = -5.6E-11     AT      = 3.3E4            WL      = 0
+WLN     = 1            WW      = 0                WWN     = 1
+WWL     = 0            LL      = 0                LLN     = 1
+LW      = 0            LWN     = 1                LWL     = 0
+CAPMOD  = 2            XPART   = 0.4              CGDO    = 5.29E-10
+CGSO    = 5.29E-10     CGBO    = 0                CJ      = 1.422861E-4
+PB      = 0.383282     MJ      = 0.6215988        CJSW    = 5.030745E-10
```

```
+PBSW    = 0.6814339      MJSW    = 0.2493804      PVTH0   =
5.216115E-3
+PRDSW   = -1.96936E3     PK2     = -0.0576815     WKETA   = 0.0466172
+LKETA   = 9.874513E-3     )
*
*
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 4.06E-8
+XJ      = 2E-7           NCH     = 8E16           VTH0    = -0.826916
+K1      = 0.7250266      K2      = -0.025237      K3      = 8.0698586
+K3B     = -2.3474126     W0      = 2.191076E-6    NLX     = 1.31782E-7
+DVT0W   = 0              DVT1W   = 5.3E6          DVT2W   = -0.032
+DVT0    = 3.3322671      DVT1    = 0.5057503      DVT2    = -0.1240424
+U0      = 283.9100584    UA      = 5.532261E-9    UB      = 3.1826E-18
+UC      = -9.52819E-11   VSAT    = 1.442493E5     A0      = 0.9541691
+AGS     = 0.1224104      B0      = 7.056174E-7    B1      = 4.277515E-7
+KETA    = -4.299405E-3   A1      = 0              A2      = 1
+RDSW    = 2.69947E3      PRWG    = -0.011933      PRWB    = -8.892093E-3
+WR      = 1              WINT    = 2.153686E-7    LINT    = 5.09883E-7
+XL      = 0              XW      = 0              DWG     = -4.372868E-8
+DWB     = 2.597449E-8    VOFF    = -0.053662      NFACTOR = 0.3339533
+CIT     = 0              CDSC    = 1.57364E-4     CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.0210985      ETAB    = 1.54997E-4
+DSUB    = 0.0259152      PCLM    = 6.9799452      PDIBLC1 = 0.3662639
+PDIBLC2 = 0.0099931      PDIBLCB = 0              DROUT   = 4.192685E-3
+PSCBE1  = 2.699703E9     PSCBE2  = 3.839271E-9    PVAG    = 0.7819165
+DELTA   = 0.01           MOBMOD  = 1              PRT     = 0
+UTE     = -1.5           KT1     = -0.11          KT1L    = 0
+KT2     = 0.022          UA1     = 4.31E-9        UB1     = -7.61E-18
+UC1     = -5.6E-11       AT      = 3.3E4          WL      = 0
+WLN     = 1              WW      = 0              WWN     = 1
+WWL     = 0              LL      = 0              LLN     = 1
+LW      = 0              LWN     = 1              LWL     = 0
+CAPMOD  = 2              XPART   = 0.4            CGDO    = 6.29E-10
+CGSO    = 6.29E-10       CGBO    = 0              CJ      = 3.147558E-4
+PB      = 0.885389       MJ      = 0.5704172      CJSW    = 3.162317E-10
+PBSW    = 0.9895045      MJSW    = 0.2496954      PVTH0   = 0.0684301
+PRDSW   = -1.880324E3    PK2     = -2.514253E-3   WKETA   = 9.4713E-3
+LKETA   = -9.1405E-3      )
*
```

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