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Transceiver Design and Radio Frequency Integrated Circuits Evaluation via Electronic Design Automation

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TRANSCEIVER DESIGN AND RADIO FREQUENCY INTEGRATED CIRCUITS EVALUATION VIA ELECTRONIC DESIGN AUTOMATION

by

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This thesis study presents the theory and design methodology of Radio Frequency Integrated Circuits (RFIC) and analyzes a RF frond-end receiver and down-conversion mixers using circuit evaluation tools. The theory of RF is described on both architectures and circuit levels with respect to monolithic implementation in integrated semiconductor technologies. The design methodology provides an efficient and practical way to approach the theoretical values by using an Electronic Design Automation (EDA) tool called Cadence Virtuoso custom design platform Based on the libraries provided by the Cadence Virtuoso, a Heterodyne receiver and two Gilbert mixer circuits have been evaluated through the simulator to reveal the system behavioral. The Heterodyne receiver is imitated with blocks of RF components by using a network synthesis technique as a design method. Both mixer circuits are evaluated in a setup of low-power and high radio frequency conditions. The evaluation results are discussed at the end of this thesis study.

TABLE OF CONTENTS

Table of Contents---continued

CHAPTER

CHAPTER

Table of Contents—continued

LIST OF TABLES

LIST OF FIGURES

List of Figures—continued

CHAPTER I

INTRODUCTION

Background

The radio frequency (RF) circuit in wireless equipment is essentially the interface to the antenna. In the past, RF circuits were based on a number of discrete components, such as transistors and coils. Nowadays, many radio frequency circuits or components have been heavily integrated and packed into monolithic LSIs (Large Scale Integrations). This gave increase to an expectation for significant improvements in the miniaturization of wireless equipment with lower power consumption and increased convenience of fabrication.

Due to the increase of integrations and the miniaturization of electronic devices, the many parts of internal RF circuits for wireless devices, both analog and digital components, are being mixed on a single integrated circuit (IC) chip. These integrated systems increasingly have a mixed signal design, embedding high performance analog blocks and sensitive RF front-ends together with complex digital circuitry. In Figure1-1 shows an example of a typical IC chip that integrates with digital and analog wireless devices such as: memories (RAM and ROM), random logic, a central processing unit, and analog signal processing frond-ends [9]. This figure illustrates one type of design that many RF engineers tend to use.

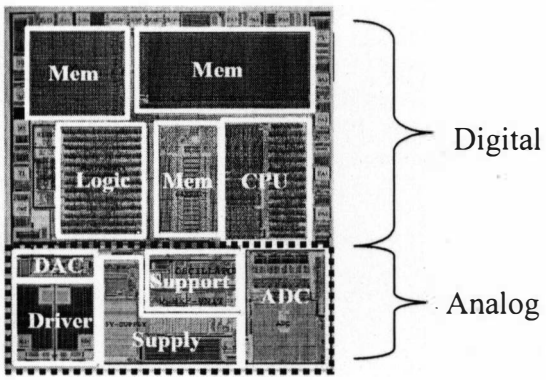


Figure 1-1 A typical mixed signal IC design. [9]

Most modern radio systems need frond-end analog signal processing components. The frond-end transceiver components can also be integrated in a mixed-signal chip. These components may include voltage-controlled oscillators (VCOs), phase-locked loops (PLLs), mixers, filters, amplifiers, Digital Analog Converters (DACs) and Analog Digital Converters (ADCs). The Figure 1-2 shows a frond-end system on a single chip.

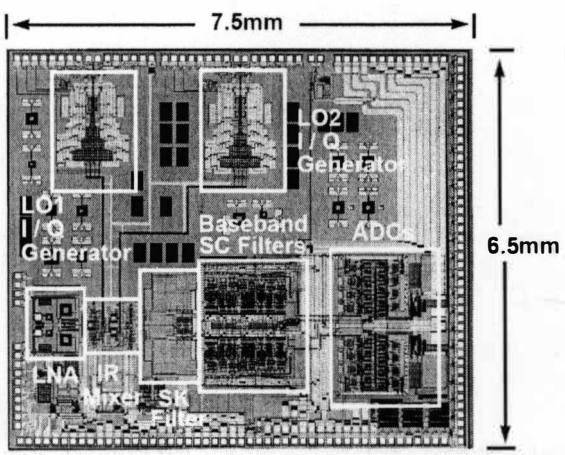


Figure 1-2 A sample of frond-end transceiver. [15]

The diverse functional nature of these components requires simulation in both time and frequency domains to be able to capture their individual behavior. In addition, these systems operate at high frequencies performing high speed communication using advanced transmitting methods, such as Orthogonal Frequency Division Multiplexing (OFDM) and fast frequency hopping. These significant characteristics make them extremely sensitive to active and passive device models, distributed layout parasites, substrate coupling effects, inter-stage impedances, IC packaging and power-supply noise. As a result of complexity, RF circuits are more difficult to design and layout on an IC chip. Besides this, the Radio Frequency (RF) circuits show several distinguishing characteristics that make them more difficult to simulate by using traditional Spice transient analysis. Therefore, in order to capture the behavior of RF circuits, an advanced Electronic Design Automation (EDA) tool named Cadence Virtuoso custom IC design platform will be used to simulate the thesis study RF circuits.

Objective of This Work

This thesis focuses on the theory, analysis, and evaluation of Radio Frequency Integrated Circuit (RFIC) design. For this work, a Heterodyne receiver and two types of mixers are evaluated and tested, with results presented at the end of the study. By using the Electronic Design Automation tool, the results can be discussed and analyzed with respect to the desired characteristics of mixer circuits.

CHAPTER II

BASIC CONCEPTS OF RF DESIGN

Introduction

An ideal Radio Frequency (RF) circuit in an ideal communication environment, it regenerates a perfect match of the desired output communication signal from its RF input signal. However, in the real world, a circuit will introduce many other waveforms generated by any component from the circuit itself or by radio frequencies from outside of the circuit. Those introducing waveforms will become noise and distortion in an output signal. Noise presented by resistors and active devices can limit the minimum detectable signal in a radio communication. Circuit nonlinearity can cause an output signal to become distorted and limit the maximum signal amplitude. In order to design a radio frequency integrated circuit with realistic specifications, a discussion of noise on minimum detectable signals and effect of nonlinearity on distortion is needed.

Noise

Noise is always being picked up by a receiver from the rest of the universe when a desired signal is being fed into a system. Noises can be introduced into a circuit during a radio signal transformation. There is one kind of noise, which is called thermal energy, generated due to the temperature related motion of charged particles. Thermal energy is caused by atoms and electrons move in a random way resulting in random currents in a circuit itself. On the other hands, there are also many other man-made noises coming from outside the

circuit system, such as microwave, cell phones, and even power chargers. In order to check out how much noise has been added to a source signal, a ratio of the signal to noise power is defined for a receiver. The sum of thermal noise power and circuit generated noise presented at the receiver front-end is defined as the noise floor. To detect a reliable signal, the minimum detectable signal level must typically be larger than its noise floor.

Thermal Noise

Resistors are the most possible components that will cause noise in a circuit. Due to thermal energy, noise will be generated in resistors causing random currents in the circuit. The formula of thermal noise in spectral density from resistors can be expressed as follows:

$$N_{resistor} = 4\kappa TR$$

where K is Boltzmann's constant ($1.38 \times 10^{-23} J/K$)

T is the Kelvin temperature of the resistor

R is the value of resistor

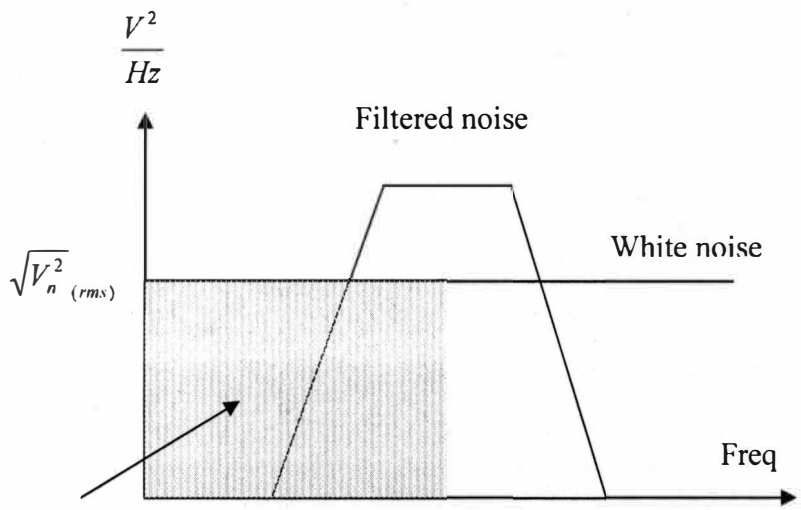
In additional, thermal noise is also white noise. This means that the thermal noise involves a constant power spectral density with respect to frequency. Therefore, to find out how much power is generated in a finite bandwidth in a resistor, the formula is presented as follows:

$$v_n^2 = 4\kappa TR\Delta f\,(v^2/Hz)$$

where Δf is the bandwidth

v_n is the noise voltage in rms value.

Usually, the mean value of noise will be zero when noise is random. Therefore, in order to measure the dissipated noise power, it is needed to use mean square values. The following Figure 2-1 shows the spectral noise power density with respect to frequency.



Total square noise V_n^2 can be found by integrating the spectral density function.

Figure 2-1 Noise power in spectral density respect to frequency.

The following Figure 2-2 shows a model of resistor noise a voltage source:

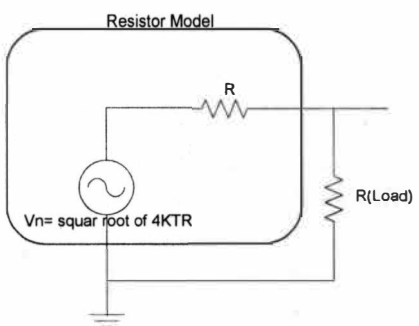


Figure 2-2 Model of resistor noise with a voltage source. [19]

The previous model can also be represented as a noise current rather than a noise voltage.

$$i_n^2 = \frac{4\kappa T \Delta f}{R}$$

The following Figure 2-3 shows a model of resistor using a current source:

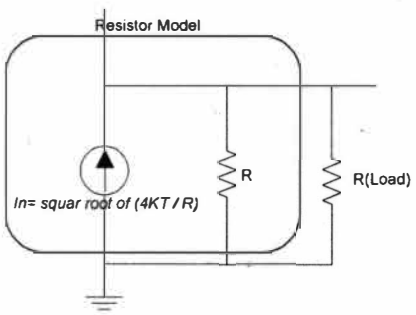


Figure 2-3 Model of resistor noise with a current source. [19]

Noise Factor and Noise Figure

Noise Factor, which is abbreviated as F, is a measure of how much noise is coming from the electronics and the signal to noise ratio degraded through a system. Any noise coming from electronics will usually be added to the noise from input. Therefore, for an accurate detection, the previously calculated minimum detectable signal level needs to be modified to involve the noise from the active circuitry.

$$F = \frac{SNR_i}{SNR_o} = \frac{\dfrac{S_i}{N_{i(source)}}}{\dfrac{S_o}{N_{o(total)}}} = \frac{\dfrac{S_i}{N_{i(source)}}}{\dfrac{S_i \cdot G}{N_{o(total)}}} = \frac{N_{o(total)}}{G \cdot N_{i(source)}}$$

where,

$S_o = G \cdot S_i$,

S_o : *Output Signal Power*

G : *Power Gain*

S_i : *Input Signal Power*

$N_{o(total)} = N_{o(source)} + N_{o(added)}$

$N_{o(total)}$: *total noise at the output*

$N_{o(source)}$: *noise at the output originating at the source*

$N_{o(added)}$: *noise at the output added by the electronic circuitry*

The noise factor can also be simplified as:

$$F = \frac{N_{o\,(total)}}{G \cdot N_{i(source)}} = \frac{N_{o(total)}}{N_{o(source)}} = \frac{N_{o(source)} + N_{o(added)}}{N_{o(source)}} = 1 + \frac{N_{o(added)}}{N_{o(source)}}$$

This result shows that the minimum possible noise factor is equal to 1 if the electronics do not produce any noise. The relation between Noise Figure (NF) and noise factor (F) is:

$$Noise \quad Figure(NF) = 10 \cdot \log_{10} Noise \quad Factor(F)$$

This means the noise figure is 0 when noise factor is 1. From a system point of view, if the electronics that added no noise will cause the value of the noise figure to be 0dB.

In RF receiver, the components are usually connected in series stages. Therefore, the calculation of the noise figure in series is determined based on the total output noise $N_{O(total)}$ and output noise due to the source $N_{O(source)}$

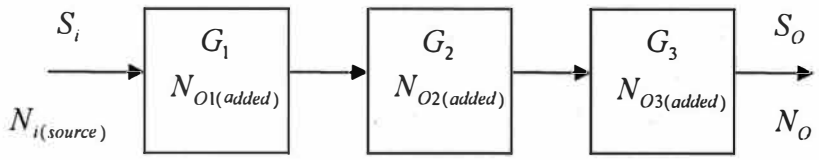


Figure 2-4 Noise figure in cascaded circuits with gain and noise added. [19]

Based on the Figure 2-4, the total output noise is:

$$N_{O(total)} = N_{i(source)}G_1G_2G_3 + N_{O1(added)}G_2G_3 + N_{O2(added)}G_3 + N_{O3(added)}$$

The input noise is:

$$N_{i(source)} = kT$$

The output noise due to the source is:

$$N_{O(source)} = N_{i(source)}G_1G_2G_3$$

Therefore, the noise factor (F) can be defined as:

$$F = \frac{N_{O(total)}}{N_{O(source)}} = \frac{N_{O(total)}}{N_{O(source)}} = \frac{N_{i(source)}G_1G_2G_3 + N_{O1(added)}G_2G_3 + N_{O2(added)}G_3 + N_{O3(added)}}{N_{i(source)}G_1G_2G_3}$$

$$F = 1 + \frac{N_{O1(added)}}{N_{i(source)}G_1} + \frac{N_{O2(added)}}{N_{i(source)}G_1G_2} + \frac{N_{O3(added)}}{N_{i(source)}G_1G_2G_3} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2}$$

In a case of noise factor for Nth stages, the equation is defined as

following:

$$F = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots\ldots\ldots\ldots$$

The above formula shows that the presence of gain preceding a stage causes the effective noise figure to be decreased with respect to the measured noise figure of a stage by itself [19].

Flicker Noise

Flicker Noise, which is also called 1/f noise, is one kind of noise associated with the nature of a transistor device. It is basically due to variation in the conduction mechanism. There is no outstanding solution to decreasing it yet, but techniques do exist to minimize the effect. The power in spectral density of 1/f noise is inversely proportional to frequency and the equation is given as in following [19]:

$$\overline{i_{bf}^2} = KI_C^m \frac{1}{f^\alpha}$$

Where m is between 0.5 and 2

α is around to 1.

K is a process constant.

The flicker noise is important in direct down-conversion receivers, as the output signal is so close to DC [19]. In some cases the flicker noise can be much worse for MOS transistors, where it can be significant (up to 1 MHz) [19].

Nonlinearity and Time Variance

In an ideal system, linear time-invariant (LTI) operations is expected which allows the outputs to be expressed as a linear combination of responses to inputs. For example, if there are two input signals, $x_1(t)$ and $x_2(t)$, the outputs of these signals can be:

$$x_1(t) \rightarrow y_1(t), \qquad x_2(t) \rightarrow y_2(t)$$

Therefore, a linear system has to be satisfied in the following condition.

$$a \cdot x_1(t) + b \cdot x_2(t) \rightarrow a \cdot y_1(t) + b \cdot y_2(t)$$

However, in any real RF component, the transfer function is much more complicated. These complexities can be due to active or passive components in a RF circuit or the signal swing being limited by the power supply rails.

It is common to have nonlinearity and time variance present in a system. Mathematically, any nonlinearity function can be written as a series expansion of power terms. Assume a nonlinear system $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)$ is memoryless and has an input signal $x(t) = A\cos(\omega t)$.

where α_1 α_2 α_3 are functions of time.

then, the result of the system is

$$\begin{aligned} y(t) &= \alpha_1 A\cos(\omega t) + \alpha_2 A^2 \cos^2(\omega t) + \alpha_3 A^3 \cos^3(\omega t) \\ &= \alpha_1 A\cos(\omega t) + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \\ y(t) &= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + 3\frac{\alpha_3 A^3}{4})\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \quad \text{(Equ.2-1)} \end{aligned}$$

where the output term $\frac{\alpha_2 A^2}{2}$ is called the "DC" signal, $(\alpha_1 A + 3\frac{\alpha_3 A^3}{4})\cos\omega t$ is called the "fundamental," signals and another other term

$\frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega$ are called the " harmonics" signals.

From the output expansion equation $y(t)$, it can be shown that even order harmonics results such as α_2 will vanish if the system has odd symmetry. Odd symmetry is defined where $x(t) = -x(-t)$. A system or circuit having odd symmetry is called differential or "balanced".

Gain Compression and 1-dB Compression Point

According to the Eequation 2-1, the term $\alpha_1 A$ can be observed to be greater than other terms containing the value A. The α_1 value can therefore be defined as a small signal gain for the RF circuit. However, when the signal amplitude is large, the α_1 value may no longer dominate. In many circuits, the output is a "compressive" or "saturating" function of the input. Therefore, a value called "1-dB Compression Point", which is shown in Figure 2-5, is defined as an increase signal input causing the small signal gain to decrease from the linear gain by 1-dB [31].

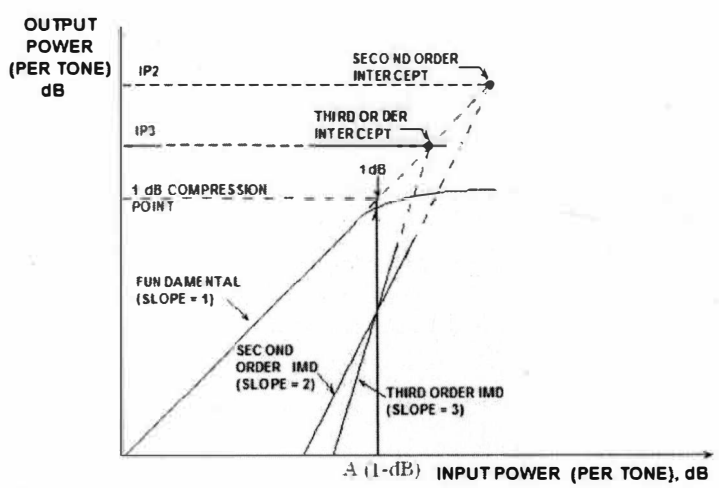


Figure 2-5 1-dB compression point.

In fact, the nonlinearity is approximated as variations of a small signal gain with the input level. From Equation 2-1, the 1-dB compression point can be calculated as follows:

$$20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 A_{1-dB}^2\right| = 20\log|\alpha_1| - 1dB$$

then

$$A_{1-dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}$$

Third Order Intercept Point IP3

Some components used in a down conversion such as mixers are based on fundamental nonlinear principles and modulation with incoming signals. However, these signals may become corrupted by nearby interfering signals due to a third order inter-modulation. Meanwhile, these components must also be able to amplify a range of incoming signals in a linear function. Therefore, there is a parameter called the "Third Order Intercept (IP3) point" measured by a two-tone test in which a value A is chosen to be sufficiently small so that higher-order nonlinear terms are negligible and the gain is relatively constant and equal to α_1. A two-tone test is another common way of analyzing the linearity of a RF circuit. For example, assume a system has two-tone input signals.

$$x(t) = A\cos\omega_1 t + B\cos\omega_2 t = X_1 + X_2$$

Apply this function to $y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)$, the result of $y(t)$ can be expressed as,

$$y(t) = \alpha_0 + \alpha_1(X_1 + X_2) + \alpha_2(X_1 + X_2)^2 + \alpha_3(X_1 + X_2)^3$$

where $\alpha_1(X_1 + X_2)$ is fundamental term

$\alpha_2(X_1 + X_2)^2$ is second-order

$\alpha_3(X_1 + X_2)^3$ is third-order

$$y(t) = \alpha_0 + \alpha_1(X_1 + X_2) + \alpha_2(X_1^2 + 2X_1X_2 + X_2^2) + \alpha_3(X_1^3 + 3X_1^2X_2 + 3X_1X_2^2 + X_1^3)$$

By using trigonometric identities, some terms can be simplified into few components that may have a zero frequency (DC) component and another inter-modulation component. For example, the value of X_1^2 can be expended and expressed into $X_1^2 = (A\alpha_2 \cos\omega_1 t)^2 = \frac{A^2\alpha_2^2}{2}(1 + \cos 2\omega_1 t)$. Therefore, for the two-tone test, it can be concluded that the second and third order terms can be expended as:

$$(X_1 + X_2)^2 = \underbrace{X_1^2}_{DC+HD2} + \underbrace{2X_1X_2}_{MIX} + \underbrace{X_2^2}_{DC+HD2}$$

$$(X_1 + X_2)^3 = \underbrace{X_1^3}_{FUND+HD3} + \underbrace{3X_1^2X_2}_{FUND+IM3} + \underbrace{3X_1X_2^2}_{FUND+IM3} + \underbrace{X_2^3}_{FUND+HD3}$$

where, DC is called zero frequency

HD2 is called second harmonic frequency

FUND is called fundamental frequency

MIX is called mixing frequency

IM3 is called third-order inter-modulation

Note that sometimes MIX may have second harmonics HD2 with mixing frequencies. The mixing frequencies basically represent the sum and difference components of the two-tone signals.

This measure describes having two input signals spaced relatively close together on the frequency spectrum, fed into nonlinear RF components such as a

mixer in the real world. The collaborated effects of these signals are known as inter-modulation. Most critical are third-order Inter-Modulation (IM3) components that appear at the output of a signal.

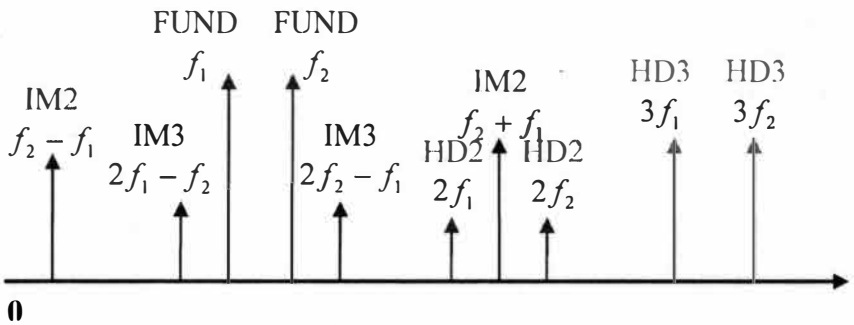


Figure 2-6 Inter-modulation signals.

From the Figure 2-6, the two undesired frequencies $2f_1 - f_2$ and $2f_2 - f_1$ are the most difficult infer-modulation frequencies that may be hard to filter them out.

The undesired inter-modulated signals are basically amplified by a non-linear cubic relationship to the input signal strength. Ideally this is to say that as the RF input power increases, the output power of the undesired IM3 signals will intersect the output power of the desired signal. It is the intersection that is referred to as the IP3 point.

In reality, neither of the signals will saturate and this intercept point will never occur, however an extrapolation of their linear slopes will serve as a good estimate. If the IP3 is referenced to the input power of the mixer, it is known as the Input Third-Order Intercept Point (IIP3) [25].

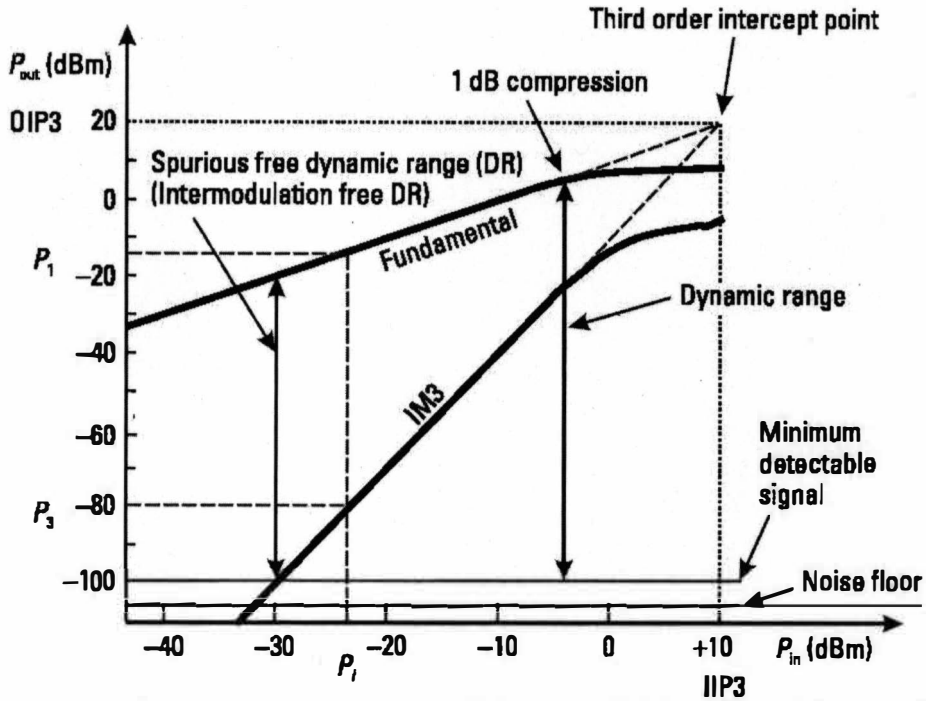


Figure 2-7 Dynamic range.

Spurious Free Dynamic Range (SFDR)

The Spurious Free Dynamic Range (SFDR) is a measurement that quantifies how mixers can accommodate a wide range of signal strength in a RF system. Depending on signal strengths, weak signals are governed by the noise floor and strong signals are governed by the 1-dB compression point shown in Figure 2-7. The Spurious Free Dynamic Range (SFDR) is defined as a ratio where the input power level is distinguished by the intersection of the IM3 term and the minimally detected signal.

S-Parameter

RF systems can be analyzed in many ways. There is a way to simplify the system analysis which retains input and output performances except details analysis from the inside structure of the system [31]. A set of parameters, which describes the scattering and reflection of signal waves, can be defined as "Scattering Parameters" or "S-Parameters". S-Parameters are normally used to characterize for high frequency circuits or network systems. They retain a desirable property by defining input and output variables in term of incident and reflected (scattered) voltage waves, rather than port voltages or currents [31]. The following Figure 2-8, it defines the input and output variables. Z_0 is the source and load terminations.

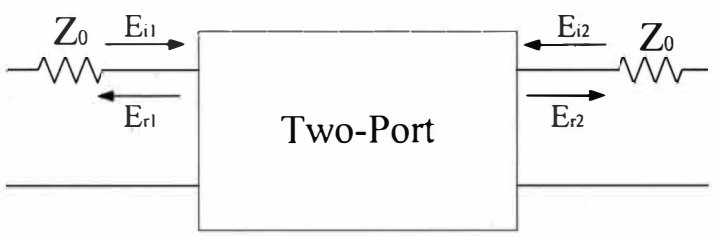


Figure 2-8 Two-tone S-parameter model.

The two-port relations can then be written as:

$$b_1 = s_{11}a_1 + s_{12}a_2 - (1)$$
$$b_2 = s_{21}a_1 + s_{22}a_2 - (2)$$

, where

$$a_1 = \frac{E_{i1}}{\sqrt{Z_0}}$$
$$a_2 = \frac{E_{i2}}{\sqrt{Z_0}}$$
$$b_1 = \frac{E_{r1}}{\sqrt{Z_0}}$$
$$b_2 = \frac{E_{r2}}{\sqrt{Z_0}}$$

By setting $a_2 = 0$, the Equations one and two can become the following relations.

$$s_{11} = \frac{b_1}{a_1} = \frac{E_{r1}}{E_{i1}} = \Gamma_1$$

$$s_{21} = \frac{b_2}{a_1} = \frac{E_{r2}}{E_{i1}}$$

s_{11} and Γ_1 can now be defined as the "input reflection coefficient" and s_{21} is the value of "gain" relating an output wave to an input wave. By having $a_1 = 0$, the "output reflection coefficient" (s_{22} and Γ_2) and the "reverse transmission" (s_{12}) can be expressed in following equations.

$$s_{22} = \frac{b_2}{a_2} = \frac{E_{r2}}{E_{i2}} = \Gamma_2$$

$$s_{12} = \frac{b_1}{a_2} = \frac{E_{r1}}{E_{i2}}$$

Even though the S-parameters model helps RF designers to analyze a system without knowing anything about the internal working of the two-port, it may also discard some important information, such as sensitivity to parameter or process variation [31].

CHAPTER III

RFIC INTEGRATION TECHNOLOGY

Introduction

IC fabrication is another important issue in RF circuits design. Based on the variations of materials and topologies, the system products may fall into in different performance ranges. The demand and the range of system performance requirements have brought in some innovative advancement in IC designs and fabrication for engineers. Besides, more and more research teams have tried to integrate many RF components into a single integrated circuit chip and design RF systems working toward more flexible and higher frequencies. These trends have made quite challenging tasks for RF designs.

Most of the modern wireless circuits are implemented with different types of transistors. There are mainly two kinds of transistors used for modulation and mixing, amplification, oscillation, switching, digital gates and so forth. The first kind of transistor is bipolar transistors which includes Bipolar Junction Transistor (BJT) and high frequency equivalent the Heterojunction Bipolar Transistor (HBT). The other kind of transistor is Field Effect Transistors (FET) which includes Metal Oxide Semiconductor FETs (MOSFETs), Metal Semiconductor FETs (MESFETs), and High Electron Mobility Transistors (HEMTs). The behavior between these transistors is quite similar within the families. For example, HBTs operate in a very similar manner to BJTs, and HEMTs do also have similar behavior to MESFETs. The following Table 3-1 lists the most common transistors used in RF circuit design.

Types of Transistors	Description	Applications
MOSFET	Metal Oxide Field Effect Transistor	Using in most electronics circuits in VLSI, Integration scale is up to 10^8 transistors per chip.
CMOS	Complementary Metal Oxide Field Effect Transistor	Low power. Short channel makes fairly high speed of operation.
BiCMOS	Bipolar CMOS	High speed and performance.
a-Si TFTs	Amorphous Silicon Thin Film Transistors	Typical gate sizes 3 to 15μm. Used in flat panel display, consumer products.
Poly Si TFTs	Polysilicon TFTs	Used in high resolution image devices.
MESFETs	MEtel Semiconductor FETs	Used in microwave and millimeter wave device and integrated circuits. GaAs MESFET exhibits higher speed with lower power consumption than comparable Si integrated circuits. Integration scale up to 10^5 transistors per chip.

Table 3-1 The most common transistors used in the RF circuit design.

CMOS Technology

The most common transistors used for RF integrated circuit design are Silicon BJT (Si BJT), GaAs MOSFET and Complementary Metal Oxide Semiconductor (CMOS) technologies [2] [7] [11] [30] [31] [33]. Since the year in 2000, much RF research has been devoted toward CMOS integration of RF circuits [26] [29]. The Table 3-2 shows the most common semiconductor technologies that have been used in RF component designs.

Wireless system	Power amplifier Switch	Transceiver (Mixers, Low Noise Amplifiers)	Base band Memory
Cellular Phone	GaAs, SiGe	Bipolar, Si BiCMOS SiGe	CMOS
WLAN	GaAs, SiGe, CMOS	Bipolar, Si BiCMOS CMOS	CMOS
Bluetooth	Si BiCMOS, CMOs	Si BiCMOS, CMOS	CMOS
GPS	-----	Bipolar, Si BiCMOS, CMOS	CMOS

Table 3-2 The most common semiconductor technologies used in RF component design.

CMOS technology has been a major development in digital applications because it can offer high yields and large wafer size of the products with many years of fabrications experiences. With those features and cheap raw material, CMOS has become the most popular and the fabrication technology is cheaper than any others [31]. Besides, due to the nature of its physical characteristics,

CMOS technology has very low quiescent power dissipation and good device isolation [19]. However, for making high frequency ICs in silicon by using CMOS technology, it may become a challenge to model a RF circuit simulation for RFIC designers. Some transistors such as bipolar transistors are applied for RF circuits because they can provide higher values of transconductance (g_m) [19].

Choice of Integration Technologies

To the RF designers, the choice of integration technologies can be based on many factors such as price, system requirement, performance and so forth. Besides, to the marketing world, the design and fabrication times are very critical for a RF system with high accuracy and performance. Therefore, the availability for an accurate simulation models is very important during a design processing. Both Bipolar Junction Transistors (BJTs) and MOS devices are adequate to predict accurately the performance of the RF circuits. Many modern RF receivers are implemented by using either CMOS or BiCMOS technologies [2] [11] [31] [32] [33]. For example, Gallium Nitride (GaN) and Silicon Carbide (SiC) are wide-bandgap materials that can handle high power density and provide a wide dynamic range. The Table 3-3 lists the comparison of properties to major semiconductors with their characteristics [22].

	Semiconductors				
Characteristics	SiC	GaN	Si	GaAs	InP
Band-Gap (eV)	3.26	3.49	1.12	1.42	1.35

Table 3-3 The comparison of properties of major semiconductors with their characteristics.

Characteristics	Semiconductors				
	SiC	GaN	Si	GaAs	InP
Breakdown Field (MV/cm)	2.2~3.0	3.0	0.3	0.4	0.5
Electron Mobility (cm^2/Vs)	700	1,000~2,000	1,500	8,500	5,400
Saturated Electron Velocity $(10^7 cm/s)$	2.0	1.3	1.0	1.3	1.0
Thermal Conductivity (W/cm.K)	3.0~4.5	> 1.5	1.5	0.5	0.7

Table 3-3 —Continued.

CHAPTER IV

TRANSCEIVER ARCHITECTURES

Introduction

The basic configuration of a radio frequency circuit is shown in Figure 4-1. The circuit combines transmitter (up) and receiver (down) conversions as a frond-end transceiver in the system. The down conversion (receiver) circuit is important because it needs many devices to translate a high frequency radio signal to a base band signal.

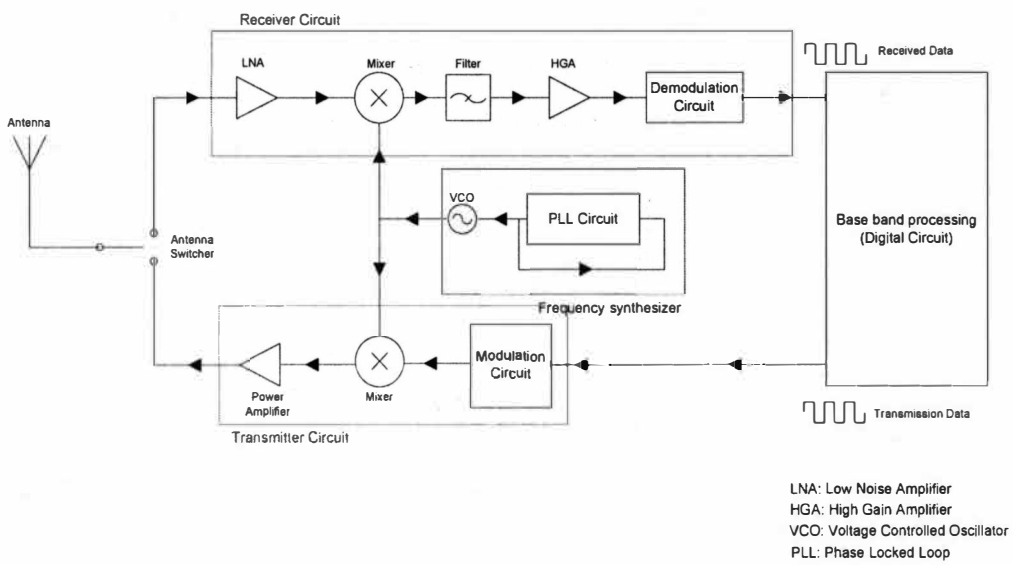


Figure 4-1 A basic configuration of radio frequency circuits.

The RF front-ended receivers can be classified into two different types of architectures. By associating with (Intermediate Frequency) the IF signal, they can be defined as Heterodyne or Homodyne receivers.

Heterodyne receivers are *widely used in current RF applications. They use*

a two-step down-converting process to bring signals from radio frequency to base band frequency by using IF signals. On the other hand, Homodyne receivers down-convert RF signals to base band frequency directly without using IF signals [1] [3] [14]. There are more and more research teams focusing on Homodyne receivers due to the less RF components needed in the receivers [23].

These receivers usually consist few essential components such as: a Low Noise Amplifier (LNA), mixers, filters, power amplifiers, and Voltage Controlled Oscillators (VCO). Depending on the requirements of each system, the RF components may be designed in varying ways. In this chapter, the RF components, which are mixers, the low noise amplifier, voltage controlled oscillator, will be discussed. In addition, two types of mixers are introduced in detail.

Heterodyne Receivers

The Heterodyne receiver has become a popular RF architecture because of the selectivity and sensitivity. Figure 4-2 shows a typical transceiver that consists a transmitting (up) and a receiving (down) conversions. The receiver (down) conversion in Figure 4-2 is called Heterodyne receiver. Typical methods of Heterodyne receiver implementation depend upon external, band-selective, Image-Reject (IR), and Intermediate Frequency (IF) filters.

The image signals need to be suppressed by proper Image-Reject (IR) filters in the receiver because they can be much higher than the desired signal. An image reject filter is designed to have a relatively small loss of the desired band and a large attenuation of the image band. The center frequency for the IF is typically fixed and is also a critical parameter. A high IF center frequency will

lead to substantial rejection of the image whereas a low IF frequency may allow great suppression of nearby interferers.

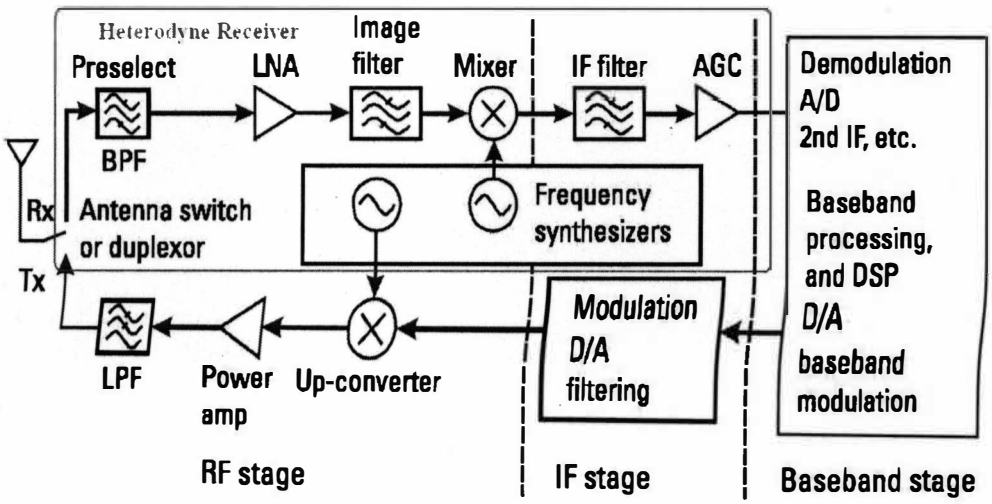


Figure 4-2 The block diagram of Heterodyne receivers. [19]

Therefore, the influencing factors in choosing the IF will rely on trade-offs among these parameters:

- The amount of image noise.
- The distance between the desired and image bands.
- The amount of loss of the IR filter.
- The availability.
- The physical sizes for different frequencies.

One phenomenon of the intermediate frequency is that the image appears far away from the desired signal band when the IF chosen is high. Then, the image band can easily be suppressed by a band-pass filter with typical cutoff characteristics. However, the channel selection filter now requires a very high Q-factor, which is defined as the ratio of the center frequency to the 3dB

bandwidth, and filters with very high Q are difficult to design. On the other hand, if the IF is low, the channel selection has a more relaxed requirement, but proper image suppression becomes harder to achieve.

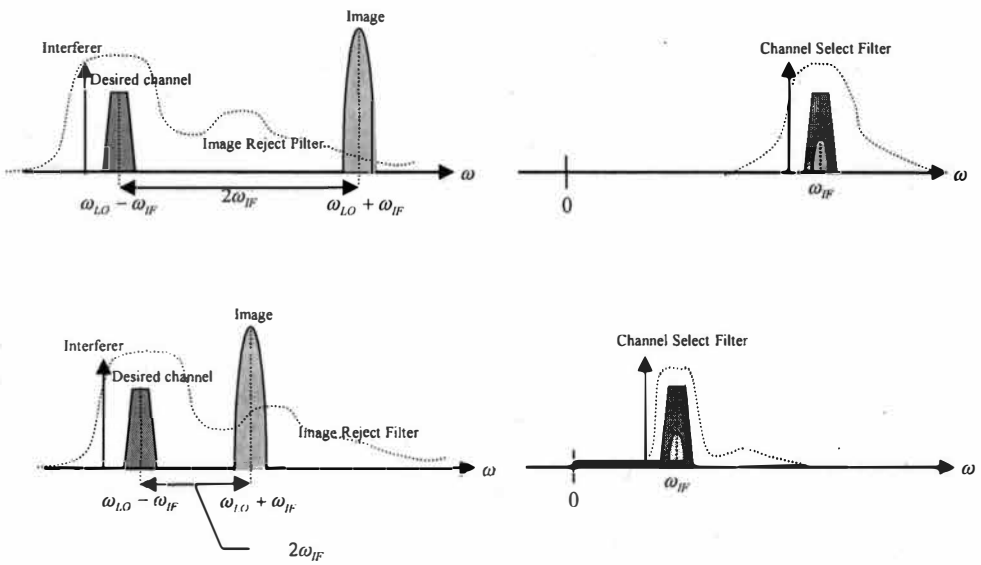


Figure 4-3 Rejection of image with suppression of interferers for high/low IF signals.

In practice, using more than one IF mixer, the receivers can be used to alleviate the conflict between sensitivity and selectivity. For example, in a dual-IF Heterodyne receiver, the RF signal is first down-converted to an IF that is high enough to allow easy suppression of the image. It is then down-converted to a second IF that is much lower than the first one to ease channel selection.

The image-reject filter is an important drawback of Heterodyne receivers because it is realized as a passive, external component. Because of the IR filter, the receiver is required to have a LNA as a preceding stage that drives the 50

ohms input impedance of the filter. It will inevitably bring more severe trade-offs between the gain, noise figure, stability, and power dissipation in the amplifier.

Homodyne Receivers: Direct Conversion

A receiver system, which translates the desired spectrum down to zero frequency (base band) in only one step by mixing with a Local Oscillator (LO) output of the same frequency, can be defined as "Homodyne" architectures. The architecture is shown in Figure 4-4.

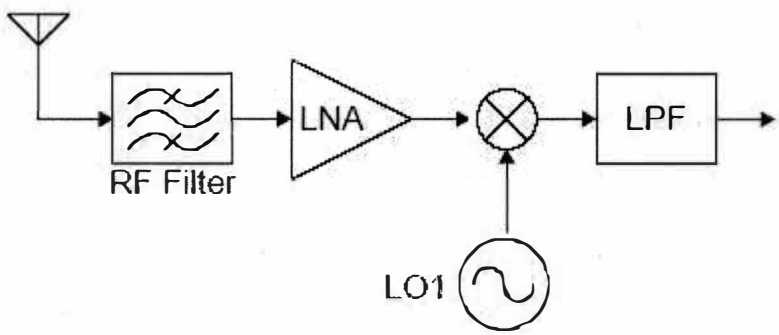


Figure 4-4 The block diagram of Homodyne receivers.

The Homodyne architecture provides two important advantages over a Heterodyne counterpart. First, the Homodyne receiver does not suffer the image problem as the incoming RF signal is down-converted directly to base-band without any IF stage. Another advantage of the Homodyne architecture is its simplicity [23] [25]. It does not require any high frequency band-pass filter, which is usually implemented off-chip in a super-Heterodyne receiver for appropriate selectivity. The principle of direct conversion is that the signal is first amplified at

a low noise stage and then directly converted to the base-band or even to a direct current signal. When the frequencies of the RF and the local oscillator signals are equal, the system works as a phase detector.

Although the Homodyne receivers have a fewer number of internal components than Heterodyne receivers, they still suffer from a number of implementation issues. The main problem with the Homodyne technique is an "offset" caused by the LO signal leakage to the RF port at the output of the mixer. The leakage of the LO signal is mixed with the local oscillator signal itself. This could saturate the following stages and affect the signal detection process. Also, since the mixer output is a base-band signal, it can easily be corrupted by the large flicker noise of the mixer [11], especially when the incoming RF signal is weak.

Image Reject Receivers

Although the image band can be suppressed by filtering the signal with an image-reject filter in a Heterodyne receiver, the image-reject filter must be sharp to operate on the RF signal, especially in systems having a low IF. The main idea of using image-reject receivers is to process the difference between the signal and the image by cancelling its negated replica of the image [4].

In order to process the cancellation in the image-reject receivers, one RF signal is required to be shifted by 90 degrees. A signal processed with an operation of "shift-by-90" means that the spectrum of a RF signal is multiplied by $G(\omega) = -j\,\mathrm{sgn}(\omega)$ [4].

There are two types of image-reject receivers. One type of image-reject

receiver is the Hartley architecture [4]. This architecture is shown in Figure 4-5.

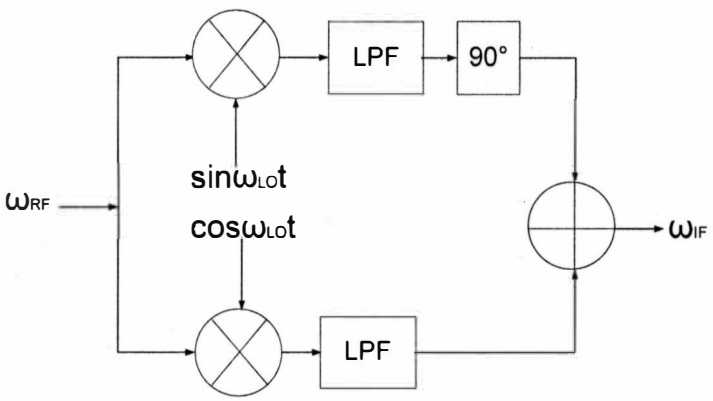


Figure 4-5 Hartley image reject receivers.

The RF signal is first mixed with quadrature phases of the local oscillator signal. After filtering both mixer output with a low-pass filter, one of the resulting signals is shifted by 90^o. Therefore, the sum of the two final signals cancels the image band to yield the desired signal, while the subtraction removes the desired band and selects the image. Also, in the typical implementation of the Hartley architecture as shown in Figure 4-6, mismatches of the R and C in the two signal paths due to process variations affect the image cancellation process.

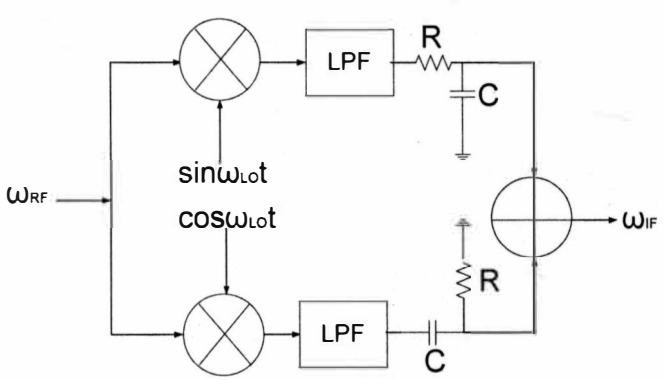


Figure 4-6 Image reject receiver with split phase shift stages.

Another type of image-reject receiver is the Weaver architecture. It has a similar structure to the Harley architecture except for a 90 degrees shift in one of the signals. The Weaver image-reject receiver also has a second set of mixing operation in both signal paths before the two signals are added to each other.

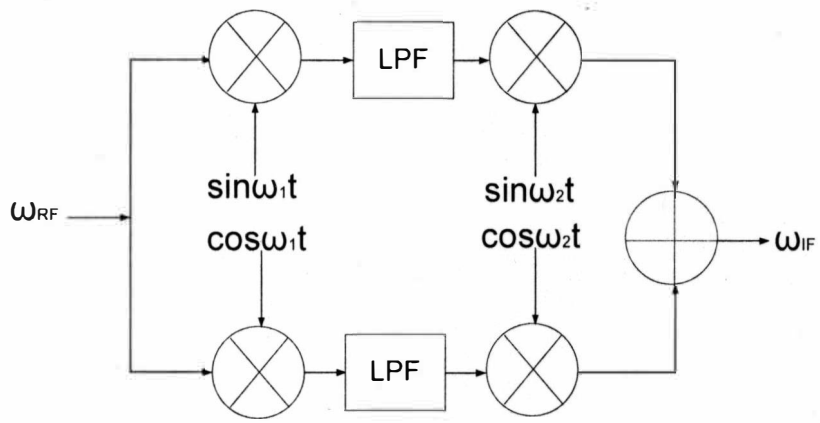


Figure 4-7 Weaver image reject receiver.

The Hartley and Weaver receivers both faced one critical issue. Both receivers are very sensitive to the phase errors of the local oscillator signals [4], which cause incomplete image cancellation.

RF Down-Conversion System Components

Mixer

Introduction

A mixer is an important structure of a radio transceiver. Many research teams have focused on mixer topologies in order to achieve better performance of RF frond-end transceivers for their design targets [7] [20] [32]. The main task of

a mixer is to translate a signal spectrum from one frequency to another by the multiplication of two signals. A lot of modern RF circuits require mixers for the frequency translating process. In a receiver, this translating process is used to convert from Radio Frequency (RF) to Intermediate Frequency (IF) or even to the base band frequency. The process of mixing frequencies requires a circuit designed with a nonlinear transfer function, because nonlinearity is fundamentally necessary to generate new frequencies. A Linear Time-Invariant (LTI) circuit can not perform frequency translation. Hence, mixers usually are either time-varying or nonlinear systems.

Mathematically, the following Figure 4-8 illustrates a signal translating process of a typical mixer.

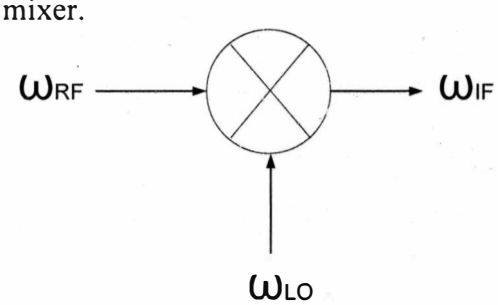


Figure 4-8 IF signal yielded a mixing from LO and RF signals.

$$V_{RF} = A\cos(\omega_{RF}t)$$

$$V_{LO} = B\cos(\omega_{LO}t)$$

$$V_{IF} = A\cos(\omega_{RF}t) \times B\cos(\omega_{LO}t)$$

$$V_{IF} = \frac{AB}{2}[\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})], \text{ where A and B are constants}$$

For most down-conversion mixers, the circuits of RF ports are linear, time-variant systems and the circuits of LO ports are usually nonlinear, time-

variant systems.

The signal applied to the RF port of a mixer is usually amplified by a Low Noise Amplifier (LNA) or filtered by an image-reject filter. Therefore, the RF port is required to provide a high linearity, low noise figure, and enough power conversion gain. The performance parameters of mixers in a typical down-conversion are listed in Table 4-1.

Noise Figure	12 dB
IIP3	+5dBm
Gain	10 dB
Input Impedance (as in Heterodyne)	50 Ω

Table 4-1 The performance parameters of mixers in a typical down-conversion.

In order to achieve a higher gain with better linearity, the mixers need to increase the bias current through the transconductance stage [27]. However, by increasing the bias current, the power consumption of mixers becomes excessive. Note that, in the mixers, the transistors in the switching stage mainly induce the flicker noise [12].

Mixers can be categorized into passive or active characteristic. Each characteristic can also be defined further into single-ended, single-balanced or double-balanced configurations. The major difference between passive and active class is the amount of conversion gain they provide. Further detailed descriptions of the mixer characteristic are discussed in the following sections.

Passive Mixers

Passive mixers do not usually provide high gain in a system. In addition, some simple passive mixers will even provide no gain at all. However, passive mixers can perform with a higher linearity and a better frequency response. Therefore, they are often used in microwave and base station circuits.

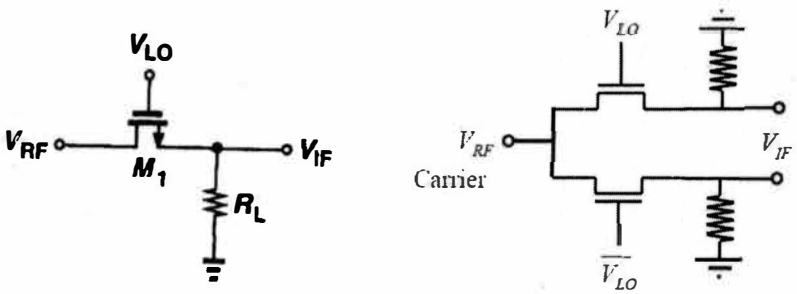


Figure 4-9 Two types of simple passive mixers.

Active Mixers

On the other hand, active mixers provide gain. In addition, the main advantage of the active mixers is that they can also diminish the noise produced and collected by sequence devices in a system. Based on this advantage, the active mixers are widely used in RF systems.

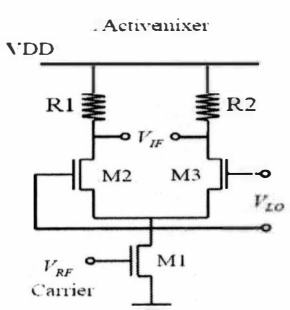


Figure 4-10 Active mixer.

Mixers with different characteristics and configurations may have varying performance results. For example, balanced-diode mixers can provide very linear signals in very high frequencies (more than 10GHz) but they do not have a conversion gain. On the other hand, active mixers can give a better conversion gain in order to reduce the noise contribution from the IF port.

Even though any nonlinear device can be used as a mixer in theory, there are only a few devices that can meet the practical requirement of mixer application. Any device that is going to be used as a RF mixer basically needs to have certain characteristics, such as strong nonlinearity, low noise, and adequate frequency response. In Table 4-2 lists the types of mixers with their characteristics.

Single Balanced Mixer

If a mixer accommodates a differential LO signal with one single ended RF signal, it can be called a "single balanced" mixer.

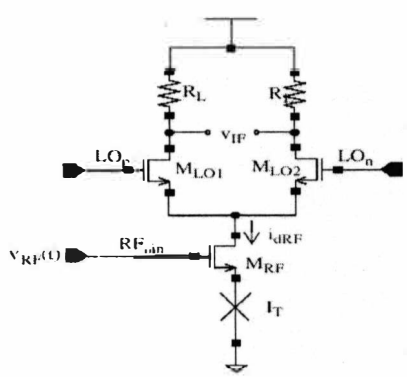


Figure 4-11 Single balanced mixer.

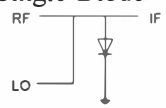
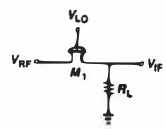
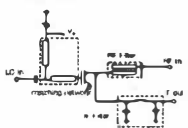
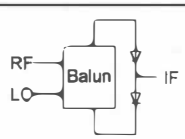
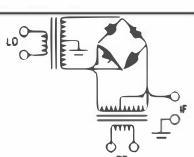
Mixers Types		Signal input and output methods	Characteristics	Comments and Application Devices
Passive	Single-ended	Single-Diode 	● Low conversion loss ~6dB ● Poor isolation ● Needs High LO power ~13 dB ● Needs 3 filters ● Poor spurious suppression ● Poor linearity	● Can be used for very high frequencies.
		Sampling 	● Good linearity ● Poor noise figure ● Low conversion loss ● Needs high LO power	● Can be integrated on GaAs MosFET, Si BiCMOS, and Si CMOS.
		Resistive 	● Excellent linearity ● Fair noise ● Low conversion loss ~6dB ● Needs 3 filters ● Needs high LO power	● Can be integrated on GaAs MosFET, Si BiCMOS, and Si CMOS.
	Singly-balanced		● Low conversion loss ● Fair isolation ● Needs Balun ● Needs 3dB higher LO power than single diode ● Good linearity	● Hard to integrate in a VLSI technology because fast diodes with low on-resistance are not available.
	Double-Balanced		● Very low conversion loss ● Good isolation ● Good spurious suppression ● Needs 6 dB higher LO power than single diode ● Good linearity	● Difficult to integrate in a VLSI technology

Table 4-2 The types of mixers with its characteristics. [33]

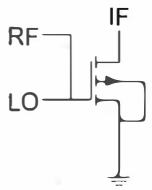
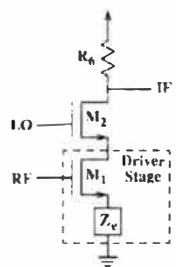
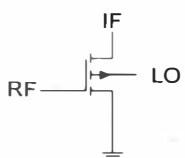
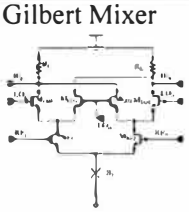
Active	Single-ended	Single-Gate 	• Low conversion gain • Low noise figure • Low distortion • Poor isolation • Needs diplexer and filter • Moderate LO power	• Down-converter in receiver • GaAs MosFET, Si BiCMOS, and SiCMOS.
		Dual-Gate 	• Good isolation without filters • Moderate conversion gain • Moderate noise figure • Low distortion • Low LO power	• Low cost integration. • Widely used in commercial applications. • GaAs MosFET, Si BiCMOS, and Si CMOS.
		Back-Gate 	• Very low power consumption • High linearity • High conversion gain • Good isolation • Low LO power	• Si CMOS.
	Single-balanced	Gilbert Mixer 	• Has same characteristics as single ended mixer • 3 dB higher LO power • 3 dB better IP3 • Needs Balun	• High performance IC applications where many transistors and the size of Baluns is acceptable.
	Double-balanced	Gilbert Mixer 	• Has same characteristics as single ended mixer • 6 dB higher LO power • 6 dB better IP3 • Needs Baluns	• Essentially the same as singly balanced mixer. • Has better inter-modulation rejection provided the extra complexity and LO power. • GaAs MosFET, Si BiCMOS, and Si CMOS, Si BJT.

Table 4-2 — Continued.

If the LO signal is assumed to be an ideal square wave in the mixer, the signal on the IF port then can be expressed as the following equation.

$$V_{if}(t) = A_{rf}\cos\omega_{rf}t \times 2G\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos n\omega_0 t$$

The single balanced mixer is basically an improvement over the unbalanced mixer. In addition, it exhibits less input-referred noise for a given power dissipation based on its circuit configuration [4]. However, it has its own drawbacks too. The first drawback of the mixer is that there is more noise on LO signal because of its susceptible circuit [4]. Another drawback of the mixer is called the "LO-IF feedthrough". Since the LO signal is amplified because of transistors M_{LO1} and M_{LO2} formed as a differential pair, it causes problems to the following signal translating stages. If the IF signal is not lower than the LO signal, a first-order low-pass filter following the mixer may not be able to adequately suppress the LO feedthrough without attenuating the IF signal [4].

Double Balanced Gilbert Mixer

The Gilbert Mixer, which was proposed in the 1960s [10], is the most common of topologies in the double balanced mixer. The design is often chosen over the simple single balanced configuration because it has well LO feedthrough isolation properties. Double balanced mixers use symmetry to cancel unwanted LO components while enhancing desired mixing components at the output [18]. The advantages and disadvantages of the double balanced mixer are listed in following:

Advantages:

- Both LO and RF are balanced, this means that the mixers provide LO and RF image rejection at the IF output port.
- Inherently provide great isolations at all ports of mixers.
- Have better linearity than single balanced mixers.
- High intercept points.

Disadvantages:

- Require a higher LO drive level.
- Have higher noise figure than single balanced mixers due to a number of transistors.

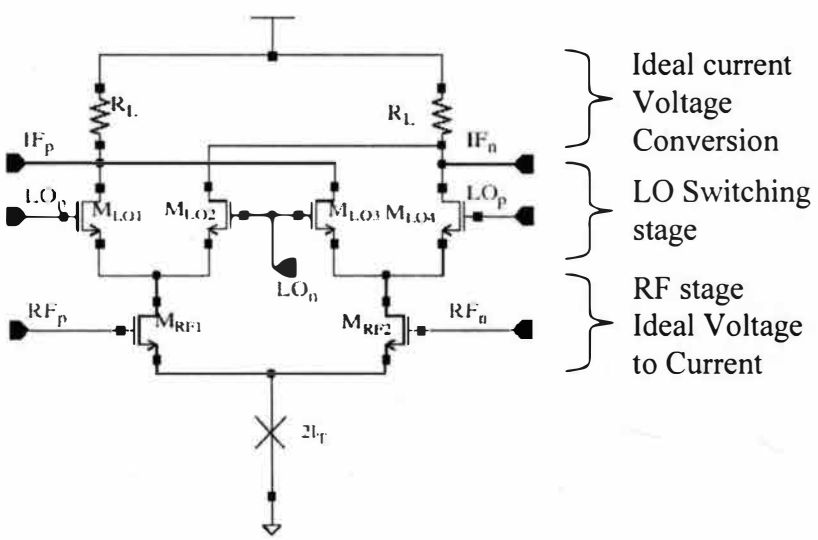


Figure 4-12 A basic type of Gilbert doubled balanced mixer.

Figure 4-11 show the basic circuit of a double balanced Gilbert mixer. The RF signal is applied to the transistors M_{RF1} and M_{RF2} that perform a voltage to

current conversion. The switching stage includes transistors from M_{LO1} to M_{LO4}. If the voltage of LO is sufficiently large, it functions as a current steering circuit which steers the current from one side to the other side of the differential pairs. The LO signal is commonly a square wave with high frequency to translate the RF signal even though the square wave may introduce a lot of odd harmonics.

Conversion Gain

The ratio of the rms voltages between the IF signal and the RF signal can be defined as a "voltage conversion gain" ($G_{c,voltage}$) of mixers. The ratio of a voltage conversion gain is usually measured a sinusoid at ω_{RF} and calculated at amplitude of the down-converted component at ω_{IF} [4].

The equations of conversion gains can be expressed in the following as:

$$G_{c,voltage} = \left(\frac{V_{RF}}{V_{IF}}\right) \quad G_{c,power} = \left(\frac{P_{RF}}{P_{IF}}\right)$$

Conversion gain is usually presented in decibel as:

$$(G_c)_{dB} = 10\log\left(\frac{P_{RF}}{P_{IF}}\right) = 10\log\left(\frac{\frac{V_{RF}^2}{R_{RF}}}{\frac{V_{IF}^2}{R_{IF}}}\right) = 20\log\left|\frac{V_{RF}}{V_{IF}}\right| (if\ R_{RF} = R_{IF})$$

Port to Port Isolation

The isolation between two ports of a mixer is an important issue for RF designers. Port isolation is a measure of frequency component suppression among different ports. It is generally desirable to minimize interaction among RF,

IF, and LO ports. Port isolation is important in determining the amount of filtering required before and after the mixer. Since LO signal is quite large as compared to the RF signal, any LO-RF feed through or leakage, if not filtered out, may cause problem in the subsequent stage of the signal processing chain. In addition, large RF and LO feed through signal at the IF output may saturate the IF port and decrease the P_{1-dB} of the mixers.

LNA (Low Noise Amplifier)

A Low Noise Amplifier (LNA) is usually the first device that starts processing the radio signals. It is placed in most front ends in the receive path. The LNA needs to be highly sensitive to the incoming signal strength, as well as be able to attenuate small amounts of noise to the system. The Noise Figure (NF) is a measure of an LNA and is based on the ratio of Signal-to-Noise (SNR) between the input and output ports.

LNA can be built from a technology based on either BJTs or MOSFETs. In each technology, there are three possible ways to construct an amplifier based on three terminals from a transistor. For example, the BJTs technology can be built as common-emitter, common-collector, and the common-base amplifiers shown as the following Figure 4-13.

Each one of these basic amplifiers can be employed in many common uses and can also be suited to some particular tasks which may not be performed by the others. The common-emitter amplifier is mostly used as a driver for a LNA. The common-collector provides a great buffer which can be placed between stages or before the output driver due to its high input and low output

impedances. On the other hand, the common-base is often used as a cascade in combination with the common-emitter to create an LNA stage with gain using in high frequency [19].

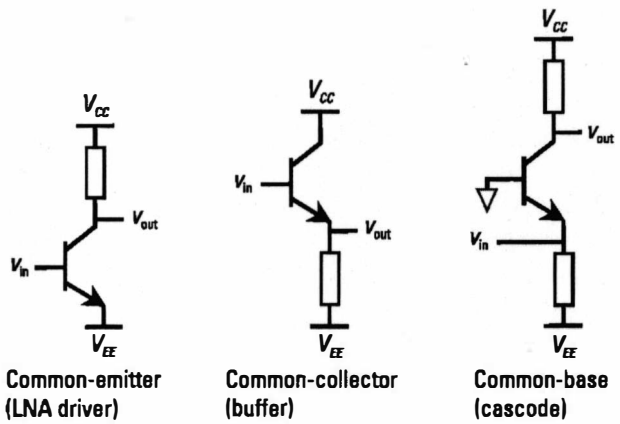


Figure 4-13 Three types of BJT circuits of LNA. [19]

The small signal model is the most important method to analyze the low noise amplifier. In order to analysis LNA in detail, the common-emitter amplifier is chosen to do the small signal model analysis since it is the most common used amplifier as a LNA in the BJT technology. The Figure 4-14 shows the small signal model of a transistor from the BJT common-emitter amplifier. The amplifier is driving the load, Z_L .

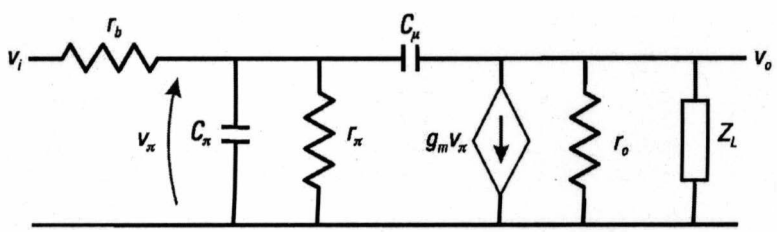


Figure 4-14 The small signal model of transistor from common-emitter amplifier. [19]

According to the model, the voltage gain of the amplifier can be expressed as the following equation at low frequency.

$$A_{VO} = \frac{v_o}{v_i} = -\frac{r_\pi}{r_b + r_\pi} g_m Z_L$$

The radio frequency, C_π will introduce a low impendence across r_π, and C_μ will also provide a feed forward path. The capacitors may need to be replaced with other values of capacitors in order to analyze the low frequency gain. Two replaced values of capacitors are expressed in the following equations with the replaced small signal model shown in Figure 4-14.

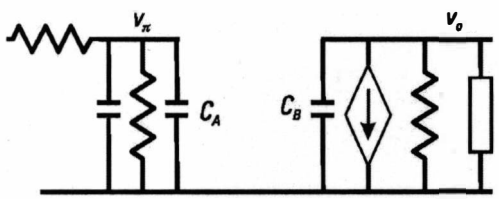


Figure 4-15 The replaced small signal model.

$$C_A = C_\mu \left(1 - \frac{v_o}{v_\pi}\right) = C_\mu (1 + g_m Z_L)$$

$$C_B = C_\mu \left(1 - \frac{v_\pi}{v_o}\right) = C_\mu (1 + \frac{1}{g_m Z_L}) \approx C_\mu$$

The whole small signal model has become two RC time constants or two poles in the system. The main pole relies on C_A and C_π which forms a frequency of:

$$f_{P1} = \frac{1}{2\pi [r_\pi \parallel (r_b + R_S)][C_\pi + C_A]}$$

Where R_S is the resistance of the source driving the amplifier.

According to the equation, decreasing load impedance causes the C_A to become smaller and the values of f_{P1} to increase.

Another frequency of the system is expressed in the following equation:

$$f_\beta = \frac{1}{2\pi \times r_\pi [C_\pi + C_\mu]}$$

The unity current gain frequency can be expressed by noting that with a first-order roll-off, the ratio of f_T to f_β is equal to the low frequency current gain β [19]. The equation of f_T can be expressed as:

$$f_\beta = \frac{g_m}{2\pi [C_\pi + C_\mu]}$$

By knowing the f_{P1}, the gain at the higher frequencies can be estimated and expressed in the following equation:

$$A_v(f) = \frac{A_{VO}}{1 + j\frac{f}{f_{P1}}}$$

In a Heterodyne receiver, the minimum gain of a LNA is defined by three parameters: the loss of the image rejects filter, the noise Figure, and the IP3 of the mixer.

VCO (Voltage Controlled Oscillator)

For up and down conversion systems, the frequency needs to be changed at different times in order to target the channel that carries a desired signal from

many channels on carrier frequencies [4]. If the output frequency of an oscillator can be varied by a voltage or current, the circuit can then be called a "Voltage-Controlled-Oscillator" (VCO) or "Current-Control-Oscillator" (CCO). The CCO is seldom used in RF system because it has difficulties in varying the value of high-Q storage elements by means of a current [4].

In order to select the desired frequency from varying carrier frequencies, A VCO always needs to have passive components such as inductors and capacitors integrated in a RF system. Those passive components need to have a proper design on a mixed-signals chip.

CHAPTER V

ELECTRONIC DESIGN AUTOMATION TOOLS

Introduction

A RF design system basically provides a comprehensive set of tools, design and simulation environment, integrity of libraries, and methodologies that cover an entire design flow for designers. In addition, in a design framework, it includes with process developers, device modeling people, IC designers, package developers and layout designers together. The developing software provides an environment that helps each team of designers to be able to exchange information and interact with one to another in order to reach the common goal of minimizing the power consumption and time to market of each RFIC design.

There are hundreds of Automation Computed Aided Design (CAD) and Electronic Design Automation (EDA) tools being applied in Integrated Circuit (IC) design markets. Based on the requirement of each RFIC design, designers need to appropriately choose the right set of EDA tools in order to achieve the product development timeline. The design process for digital integrated circuits is extremely complex. Besides, the EDA and CAD developing tools are essential to this design process and are also extremely complex too. Because this thesis study targets on designing a RF integrated circuit with results of evaluations, it is found that the Cadence Virtuoso custom design platform may meet the needs of the requirement. In the following sections of this chapter, descriptions of design system and Cadence Virtuoso custom design platform will be discussed in detail.

Description of System Design

A design system includes in three main components which are design environment, design kits, and design methodology associated with a tool flow. For example, Figure 5-1 shows a super-Hetherodyne transceiver is combination of several circuits that are built by using different technologies: bipolar, GaAs, and CMOS.

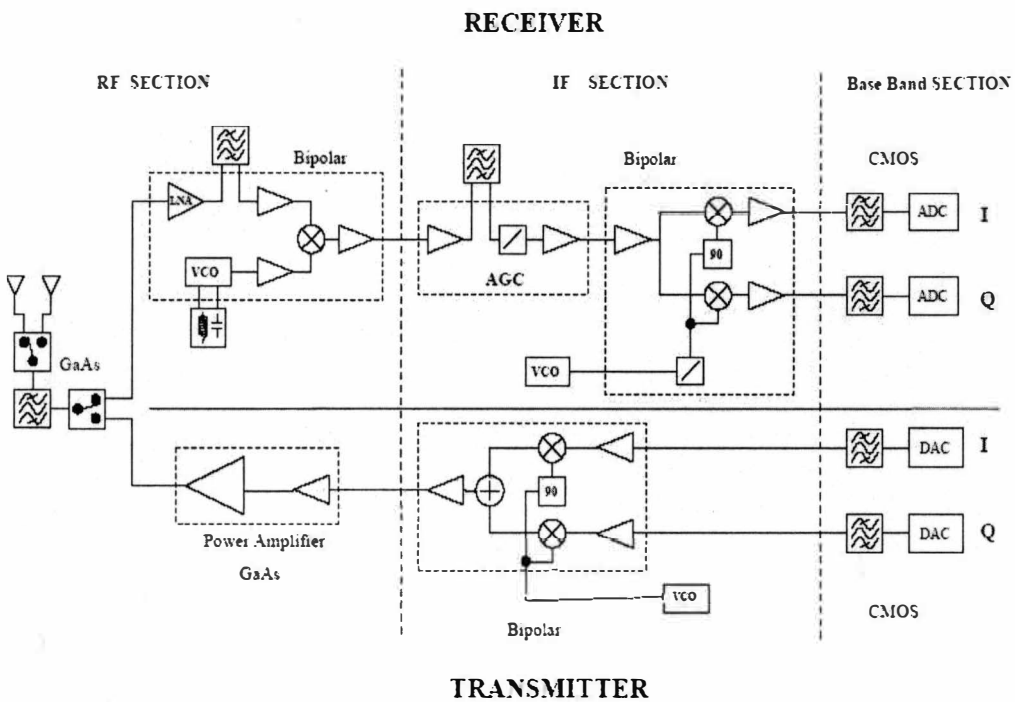


Figure 5-1 The super-Heterodyne transceiver.

Hence, many processes need to be managed at different stages of their development. In order to developing these technologies concurrently successful, it is very important to have synchronization mechanisms in place between contributors. This factor may be the key to accomplish a design success or not.

Description of Design Environment

Cadence is a large company that offers a dizzying array of software for Electronic Design Automation (EDA) applications. One of Cadence EDA software called Virtuoso Custom Design is generally targeted at the design of electrical circuits, both digital and analog, and allowing to support extending from extremely low-level VLSI design to the design of circuit boards for large systems. The Cadence Virtuoso Custom Design environment, which is one of IC design platforms, provides an IC design environment that mainly targets on the diverse domains of analog custom digital, RF, and memory / array design. It supports the work of logic and circuit design engineers, including drafters. Physical layout designers and printed circuit board designers can use the information as background material to support their works.

Description of Design Kits

The Cadence EDA tools support different fabrication technologies by using sets of files, sets of configurations, and design kits related files preloaded in the libraries of tools. The design kits are the core of the design system. It has sets of libraries that contain all the primitive parts of design components allowing designers to use in a specific process. Each component supported evaluations is fully characterized both electrically and physically. From the electrical point of view, all models do have characteristics based on the physical nature of device available to be able to simulate with whole system in the design environment. On the other hand, based on the electrical values requested by the users, a set of routines are written to calculate the appropriate physical layout features of a

integrated circuit chip. The fabrication processes can provide a characteristic of device from electrical way to physical one or on the other way around based on what methodology and tool flow. From available fabrication processes, the results of evaluations can be more accuracy to system requirement and also save time for product marketing. Those libraries and design kit can usually be provided from fabrication service vendors or organizations such as MOSIS (Metal Oxide Semiconductor Implementation Service).

Description of Design Methodology

The way of design methodology can be either top-down or bottom-up depending on RF system requirements. In the Figure 5-2, it shows the predictability that is the driving force behind the design methodology.

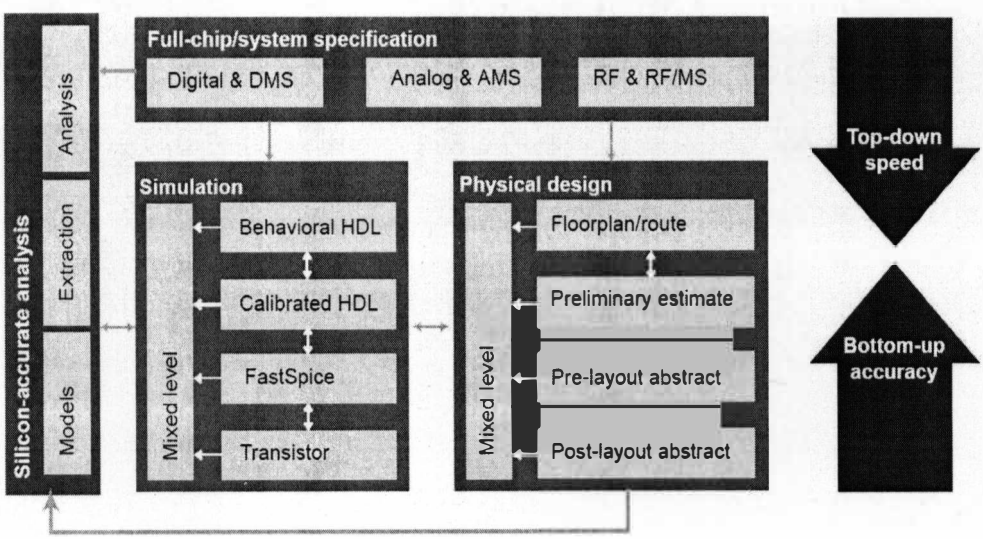


Figure 5-2 The advanced custom design methodology.

Predictability is a way to evaluate a system from either the beginning of the design process (necessitating a fast path to tapeout) or the component requirements that achieve first-pass success (requiring silicon accuracy) [6].

The Figure 5-3 shows a design flow as a top-down design methodology. At the top of the block diagram, a circuit system is designed in schematic entry based on system requirements by using Composer tool. Spectre RF is the tool to verify and evaluate the system performance with respect to specifications. Once the performance has met the requirement, the integration of layout and verification tools take the place for quickly checking the correctness of the layout interaction. When layout is completed, a post-layout is performed to ensure that the layout conforms to all manufacturing specifications. In the last step of RF design, a format conversion is performed to transfer the layout result into mask-level of fabrication between organizations and design tools. The format may be varied depend on mask-level of fabrication [17].

Note that Virtuoso Custom Design platform is only operated on UNIX terminals, PCs loaded with Linux, or UNIX terminal emulators. It is necessary to set up well related configurations in each tool of Design platform in order to have proper functional simulations.

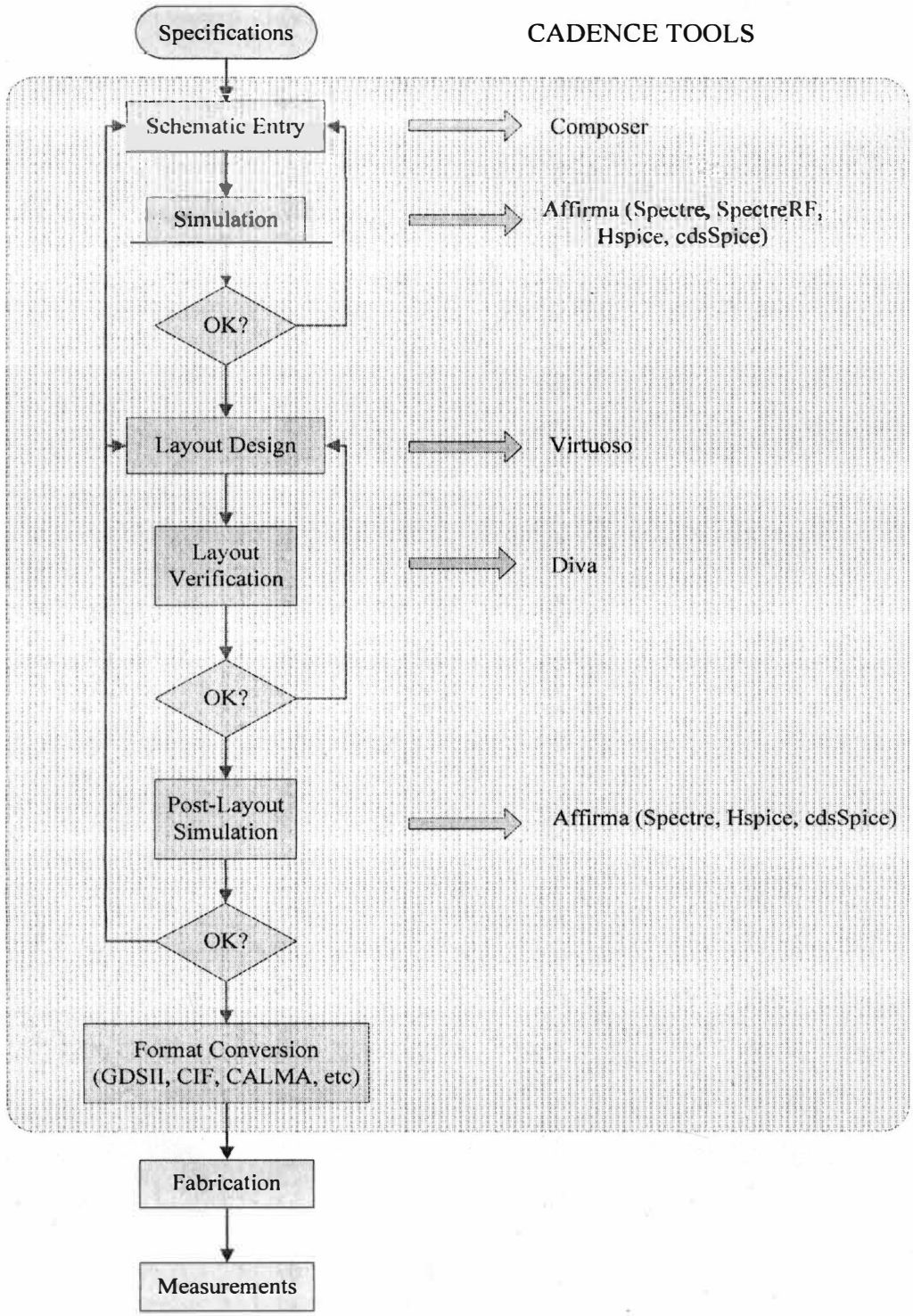


Figure 5-3 A design flow as a top-down design methodology.

CHAPTER VI

EVALUATION RESULTS

Any circuit design is always needs to be tested and evaluated before it starts going to next step processing. The SpectreRF Simulation Analysis (version 5.1.41) is one of the circuit analyzing tools for Cadence Virtuoso to test the RF circuit and shows the results wherever will meet the system specification. If the simulation results seem to meet the system requirement, it will be sent to the layout processing and having a packaging process later.

In this thesis, the simulation has designed in two parts of RF systems which illustrate how a frond-end receiver and mixers functioning. The first part of simulation design used a Heterodyne receiver to form a system of basic frond end receiver. This evaluation system consists some essential components of a Heterodyne receiver such as: a LNA, mixers, band-pass and low-pass filters. Based on the simulation design, a process of signal translation from a RF signal through IF to the base band signal can clearly be shown. The results of the simulation are illustrated and discussed in the following sections.

In the first part of evaluation, it is clear that mixers are the key to translate a high frequency to a base band frequency. Therefore, in the second part of evaluation, two types of mixers are targeted and chosen to have a further research and present some results. The focus of this evaluation is going to be a comparison the performance of these mixers in different configuration but having same specifications. The two types of mixers are active single balanced and double balanced mixers. Both mixers have also described and shown the circuit configuration in detail in the following sections.

All of the components and model files which is the model behavior of the transistors were provided from the Cadence libraries.

Heterodyne Receiver

Figure 6-1 is a simplified block diagram of Heterodyne receiver.

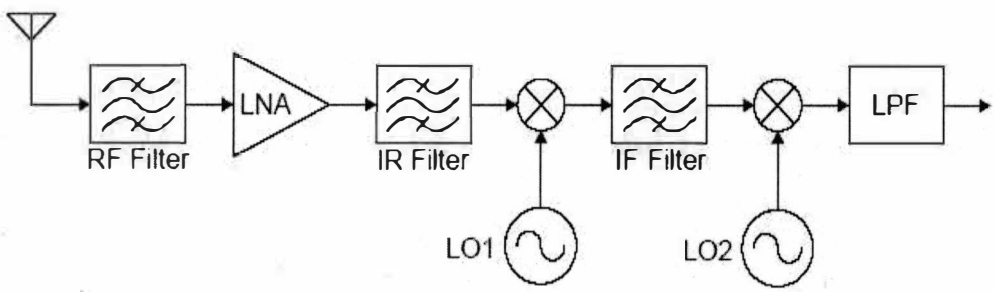


Figure 6-1 A block diagram of Heterodyne receiver.

By imitating Figure 6-1, a basic Heterodyne, front-end receiver system, has been designed and is shown in the corresponding block diagram in Figure 6-2.

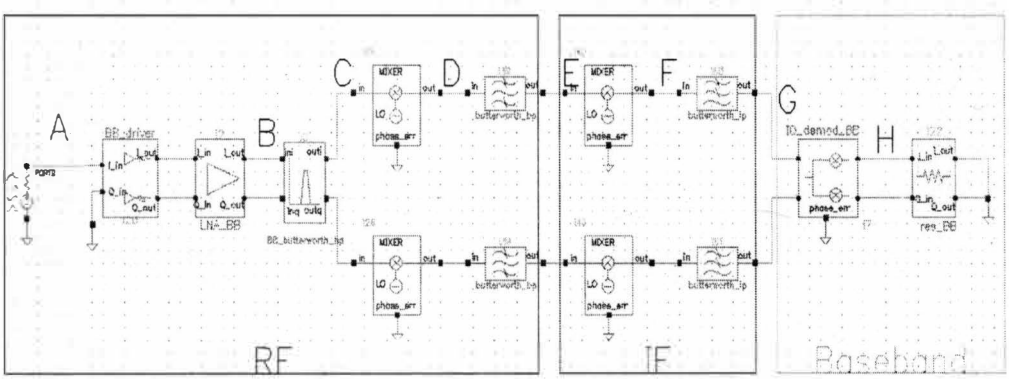


Figure 6-2 A block diagram of designing Heterodyne receiver.

Based on the typical structure of a Heterodyne receiver, the evaluation system is divided into three major stages: RF Stage (contained in the blue block), IF Stage (contained in the brown block), and base band Stage (contained in the orange block). Each stage consists of a few or more RF component blocks that perform a proper stage task. In addition, each block diagram was appropriately designed by using Verilog-A language to represent each RF component functioning in the receiver.

In the first stage of the simulation, the source signal was setup as a frequency of 920MHz with amplitude of -20dB to imitate a RF signal in the system. The rest of RF components were also appropriately setups in order to achieve the best performance of the system.

All the results of frequency translating has listed and discussed in the following pages. In the following pages, the job of the components at each individual point (from A to H) shown in Figure 6-2, are explained in the following pages.

The RF Source Signal (Point A)

Figure 6-3 is clearly shown the source signal that fell on 920MHz with the amplitude of -20.3dB in the frequency domain at Point A in the system. This source signal is setup to imitate a RF signal for this frond-end receiver design system.

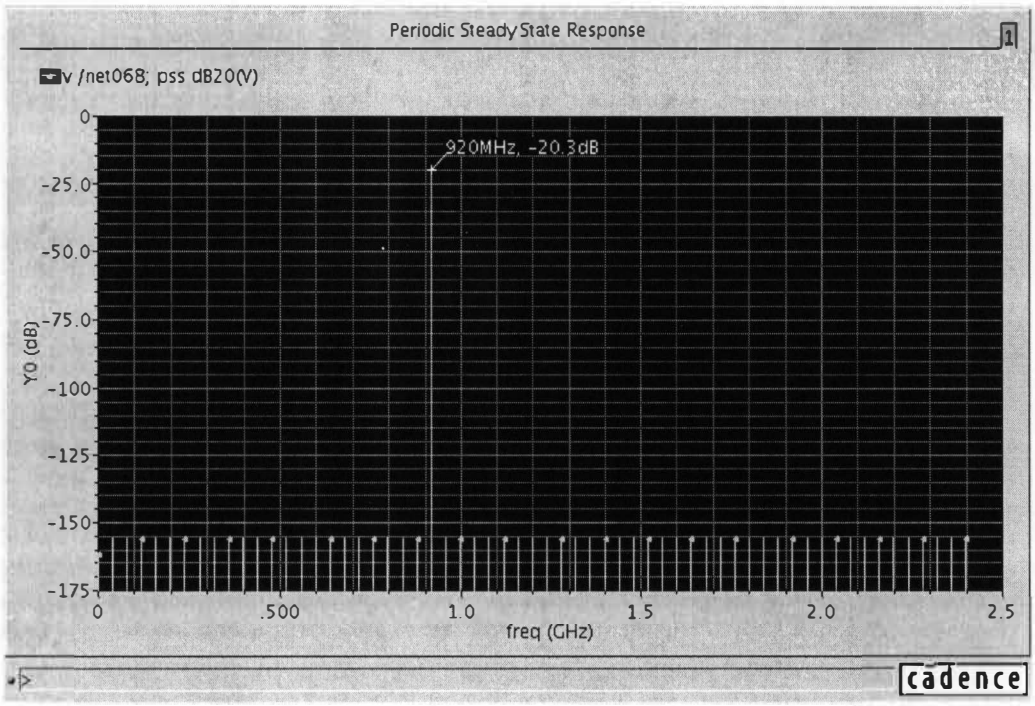


Figure 6-3 The simulation RF source signal.

Low Noise Amplifier in First Stage (RF) Block (Point B)

The Figure 6-4 represents a signal that has been processed by a Low Noise Amplifier (LNA) in the first stage of the receiver. A LNA component is usually placed at the very front end of a receiver in order to amplifier the coming targeted RF within low noise conditions. The Figure 6-4 shows that the RF signal has an increasing value from -20.3dB to 5.28dB. Meanwhile, the rest of the undesired signal spectrums have also been amplified from -155dB to above -95dB.

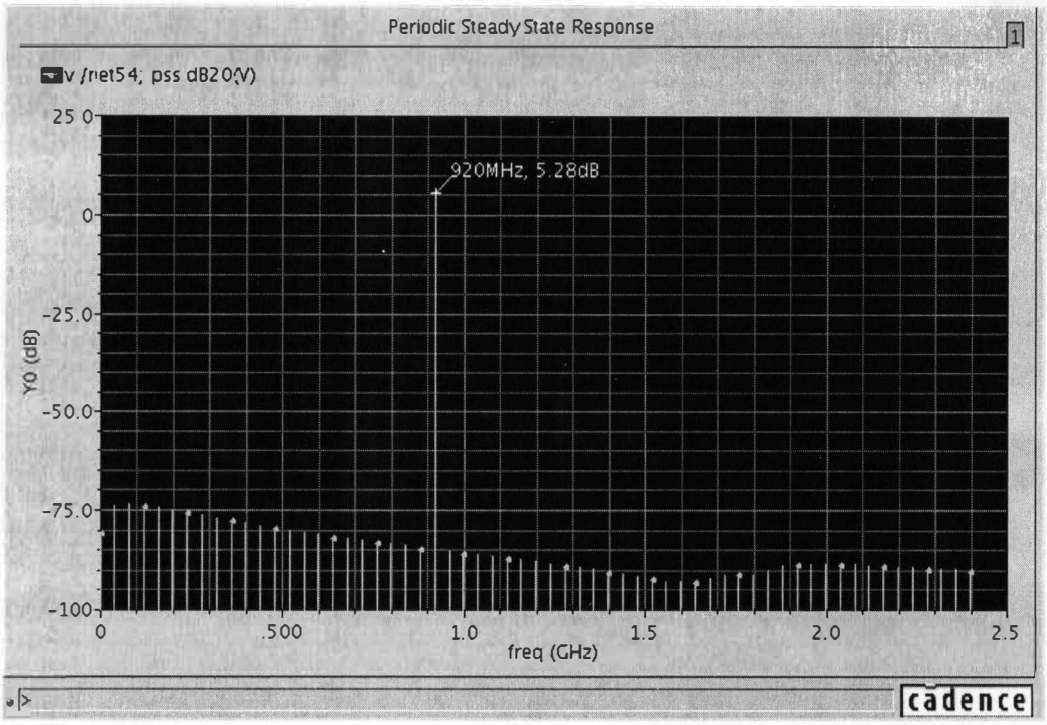


Figure 6-4 The signal spectrum processed after the LNA.

Band-Pass Filter in First Stage (RF) Block (Point C)

In the real RF world, there are tremendous amounts of un-wanted signal mixed with other frequencies that have to be eliminated out in order to target the desired RF signal. Therefore, a band-pass filter is needed to achieve the channel targeting in the first stage of the receiver. Figure 6-5 shows that the desired RF signal is targeted and processed through a band-pass filter.

Note that it is not an easy task for the SpectreRF circuit simulator to process frequency domain data that are specified for filter properties. SpectreRF simulation requires a large signal, time-domain model to simulate those behaviors of filters.

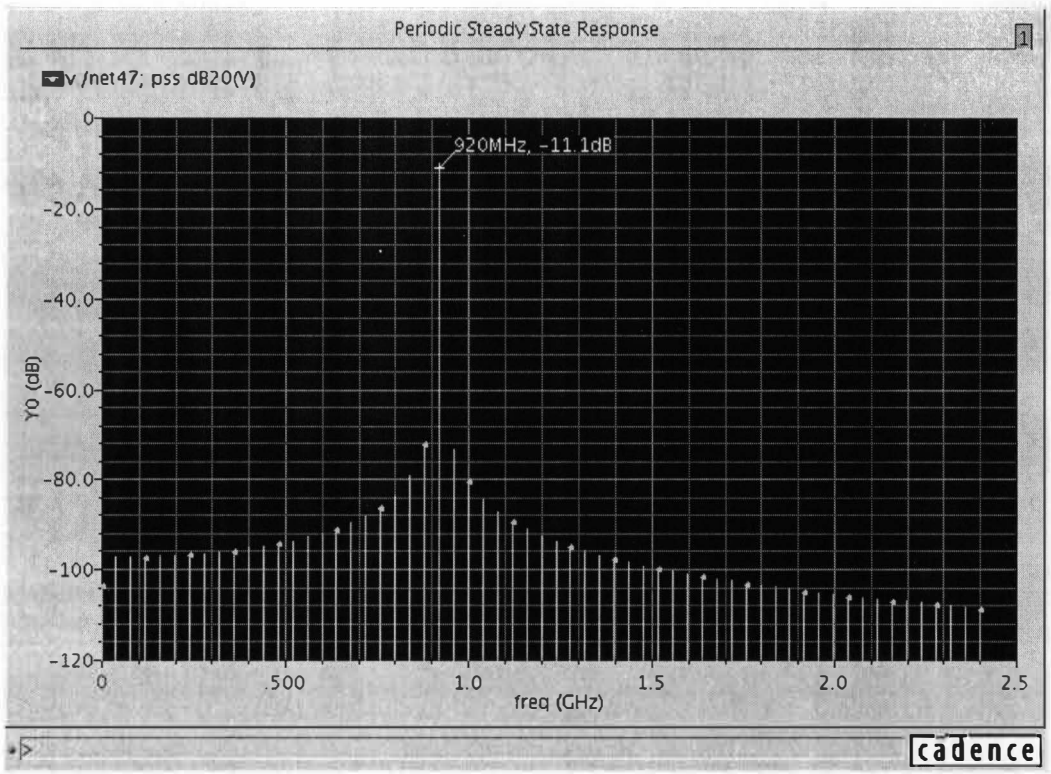


Figure 6-5 The signal spectrum processed after the band-pass filter.

In order to be capable of simulating filters in frequency domain, SpectreRF uses a network synthesis technique which contains many descriptions written by Verilog- A language for inductors and capacitors to implement filters. Then, using S-parameter analysis measurement tests the filters.

Mixer in First Stage (RF) Block (Point D)

The main task of mixers is to perform frequency translation by multiplying the desired RF signal with LO signal in order to output IF signal in lower frequency for further processes. Figure 6-6 shows an IF signal at 80.6MHz with amplitude of -8.12 dB that is constructed by multiplying the RF signal

920MHz with LO signal 1GHz.

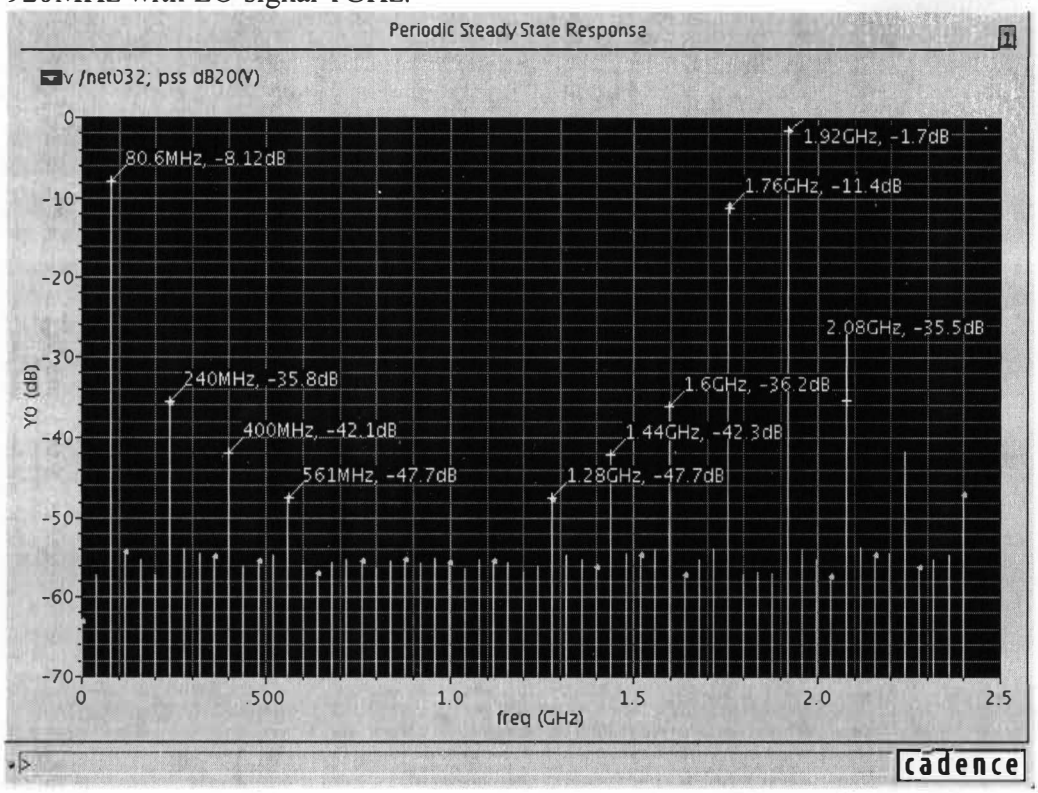


Figure 6-6 The signal spectrum processed after the RF mixer.

Note that a few distinct inter-modulation signals occurred after the mixer translated the RF and LO signals. In the Figure 6-6, there are few distinct inter-modulation signals that occurred. According to the basic concepts of mixers, the inter-modulation signal that appeared at 1.92GHz ($f_{RF} + f_{LO} = 920MHz + 1GHz$) is so called an image signal. It is one of the major un-wanted inter-modulation and harmonic signals that can be easily suppressed in the next stage (IF stage) by a band-pass filter with typical cutoff characteristics. Another un-wanted signal occurred at 1.76GHz. It was the result produced by the second order inter-modulation IF signal mixing with the image signal. It can also be filtered out by a band-pass filter as well.

Image Reject Filter in First Stage (RF) Block (Point E)

The Figure 6-7 shows the signal spectrum results at Point E in the system. The figure absolutely illustrated all the most un-wanted inter-modulation signals had been filtered out, except the desired IF signal, by a band-pass filter. Since this filter can attenuate the distinct image signal and allow the targeted signal to go through, it is sometimes called an image rejected filter.

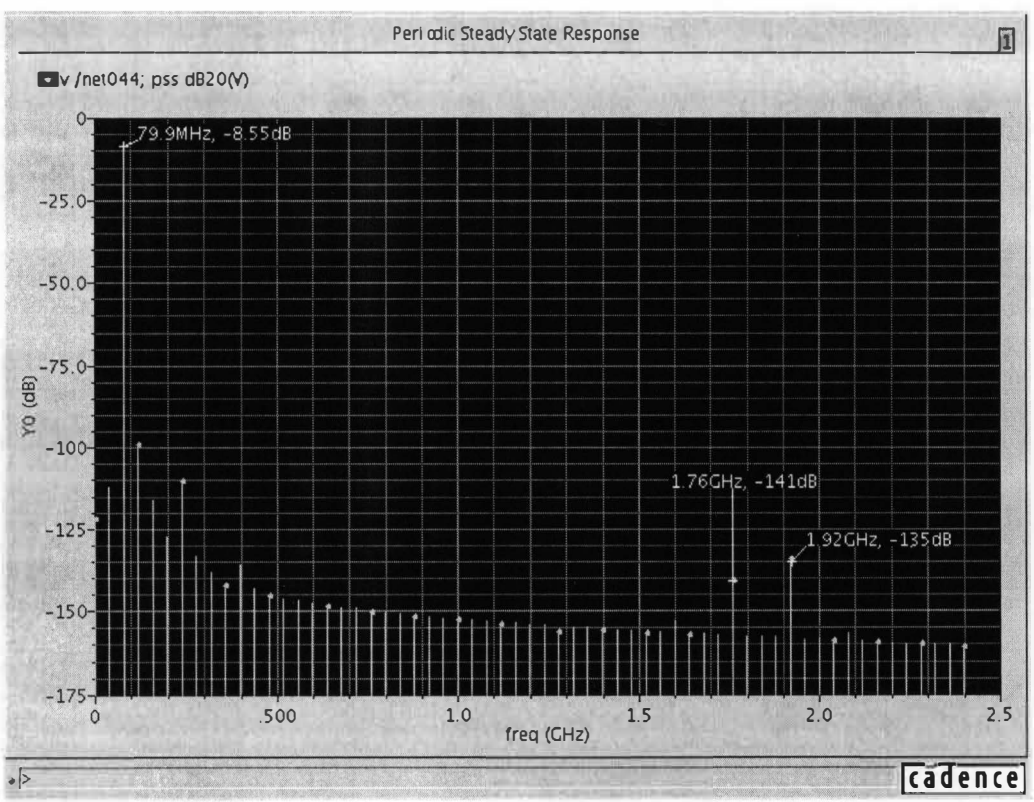


Figure 6-7 The signal spectrum processed after the image reject filter.

Mixer in Second Stage (IF) Block (Point F)

Since the source signal has been traveling through the whole RF stage, it is translated from radio frequency to intermediate frequency at Point F of the system. In order to bring the desired signal to base band, the Heterodyne receiver needs another intermediate stage to process the signal. The Figure 6-8 shows that the mixer has converted the IF signal from 79.9MHz shown in the previous stage to the base band frequency. The base band frequency occurred at 0 Hz with amplitude of -3.97 dB. During the signal down-converting to the base band frequency, the mixer also created a lot of un-wanted inter-modulation and harmonic signals such as first-order, second-order, and to n-th order inter-modulation signals. The resulting signal spectrums have shown in the Figure 6-8 of the simulation.

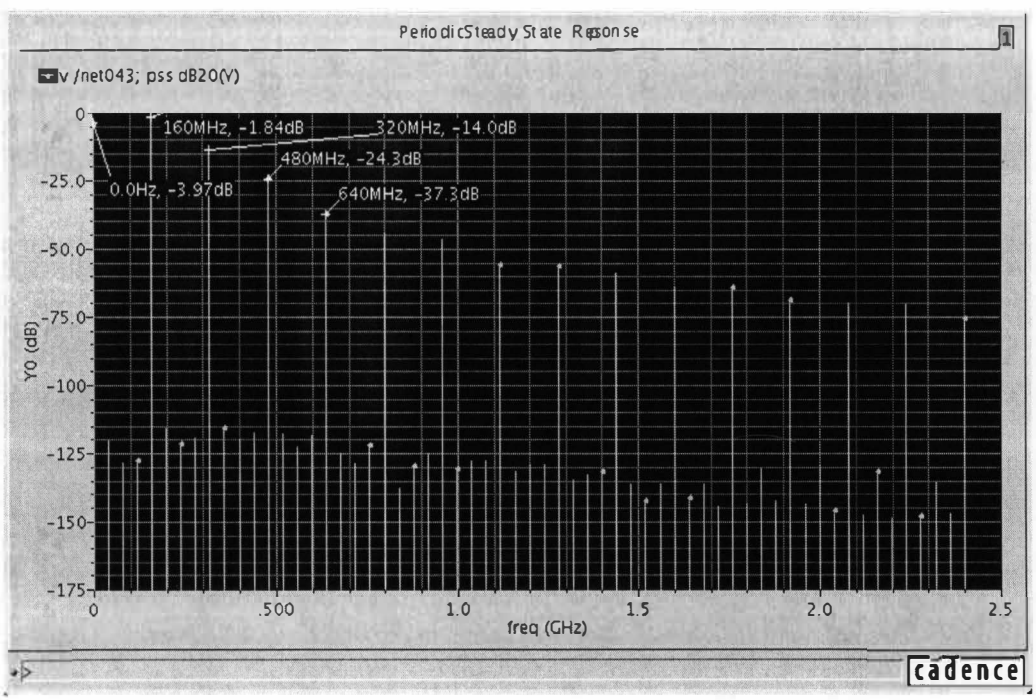


Figure 6-8 The signal spectrum processed the second stage of IF mixer.

Low Pass Filter in Second Stage (IF) Block (Point G)

In this stage, a low pass, or so called channel selected filter, is needed to eliminate those un-wanted inter-modulation signals that were created at the IF mixer stage. The Figure 6-9 shows that all of the undesired inter-modulation signals have been attenuated except the base band signal at 0Hz with amplitude of -9.99dB.

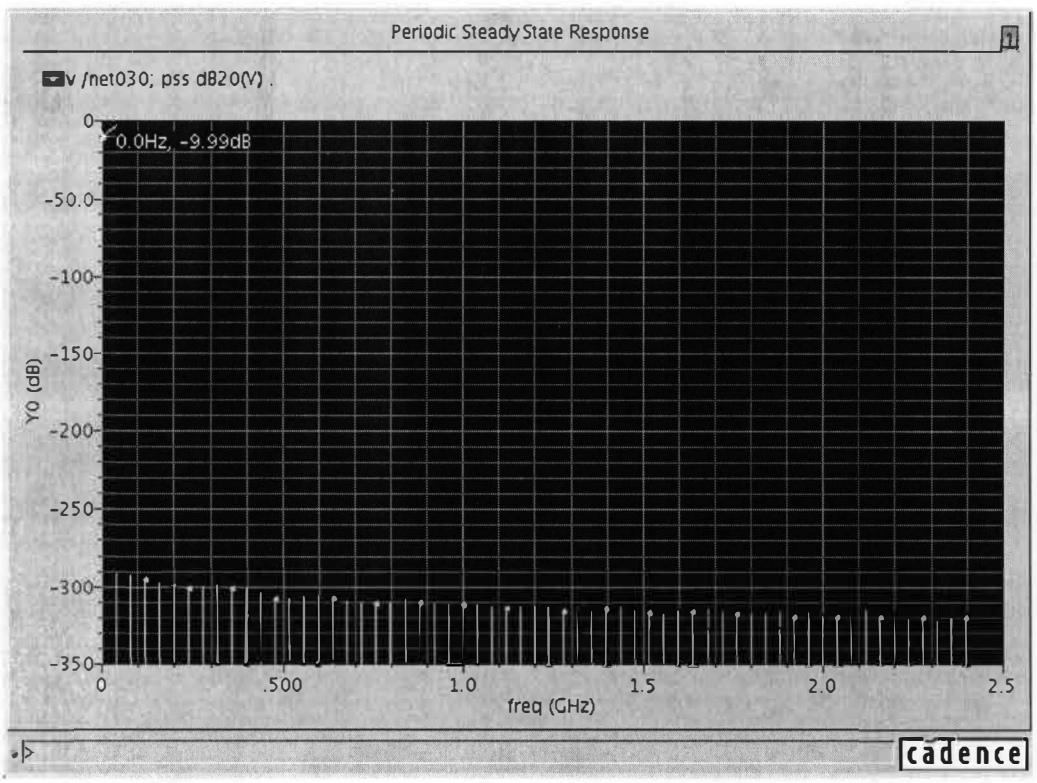


Figure 6-9 The signal spectrum shown after the low pass filter in second stage.

I / Q Demodulation in Third Stage (base band) Block (Point H)

In this stage, the source signal has been totally converted into base band

frequency in the RF level of signal processing. The Figure 6-10 shows the base band signal that occurred at 0Hz with amplitude of -13dB (0.223872 volts) in this final stage of the system. The result signal is usually amplified to a specific amplitude level by Automatic Gain Control (AGC) before it needs to be demodulated in digital signal processing (DSP) world.

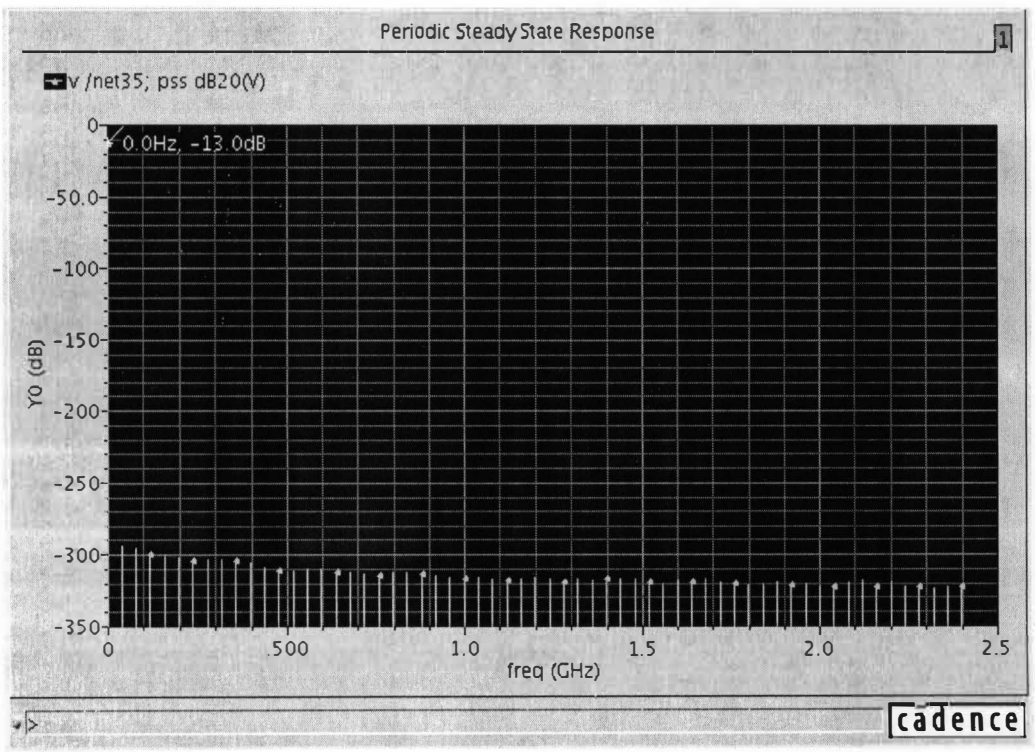


Figure 6-10 The base band signal in the final stage.

Active Single Balanced Mixer

From the first part of evaluation, it clearly showed that mixers are the key components to translate a desired high frequency to the base band frequency. Therefore, in this section, two types of mixers are designed and discussed with

results of evaluations. The first mixer is called single balanced active mixer that shows in Figure 6-11.

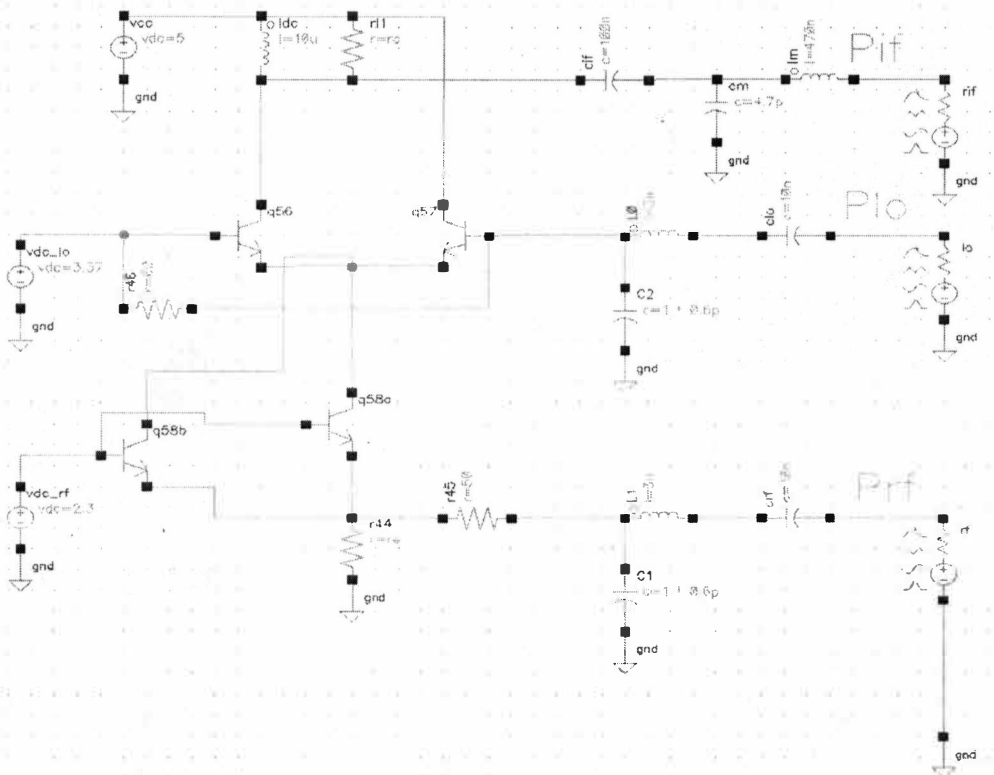


Figure 6-11 Schematic for the single balanced mixer circuit.

The SpectreRF Simulation Analysis provides circuit simulating measurements that can be used for analyzing circuits such as mixers. The evaluation is able to presents different analysis results depending on types of analysis measurements. In order to analyze both mixers in detail, few analysis measurements are described with the results of evaluations.

Frequency Spectrum Analysis (Periodic Steady State (PSS) Analysis)

The PSS analysis is one of analysis used for a large signal which can directly compute the periodic steady state response of a circuit. Basically, the PSS analysis simulations are calculated by first performing a transient analysis until the circuit has settled. Then, the simulator performs a Fourier analysis on one period of the transient signal. The result generates a frequency spectrum of that signal. Figure 6-12 shows a result of frequency spectrum of the output signals. The figure clearly indicates the low voltage circuit with the IF signal presence at 79.9MHz with voltage gain -47.8dB which is mixed from the RF signal 921MHz (-40.5dB) with the LO signal 1GHz (-62.3dB). Most un-wanted and inter-modulation and harmonic signal is attenuated in 50dB away from the IF signal.

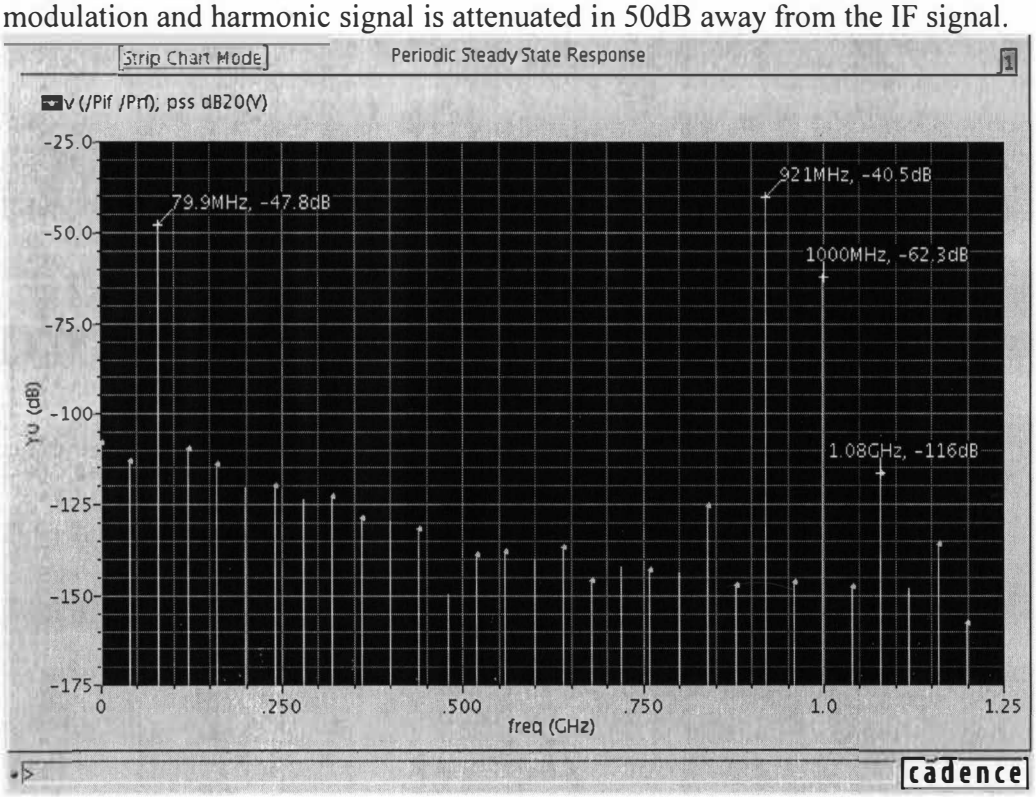


Figure 6-12 Output frequency spectrum.

1-dB Compression Point (Swept PSS Analysis)

The Swept PSS analysis is used to determine the 1-dB compression point of the mixer. The Swept PSS simulation is functioned similar to PSS simulation except the RF input power sweeping between -5 dBm to -40dBm. The Figure6-13 shows that the 1-dB compression point or P1dB occurs when the mixer receivers an input of -8.4993 dBm.

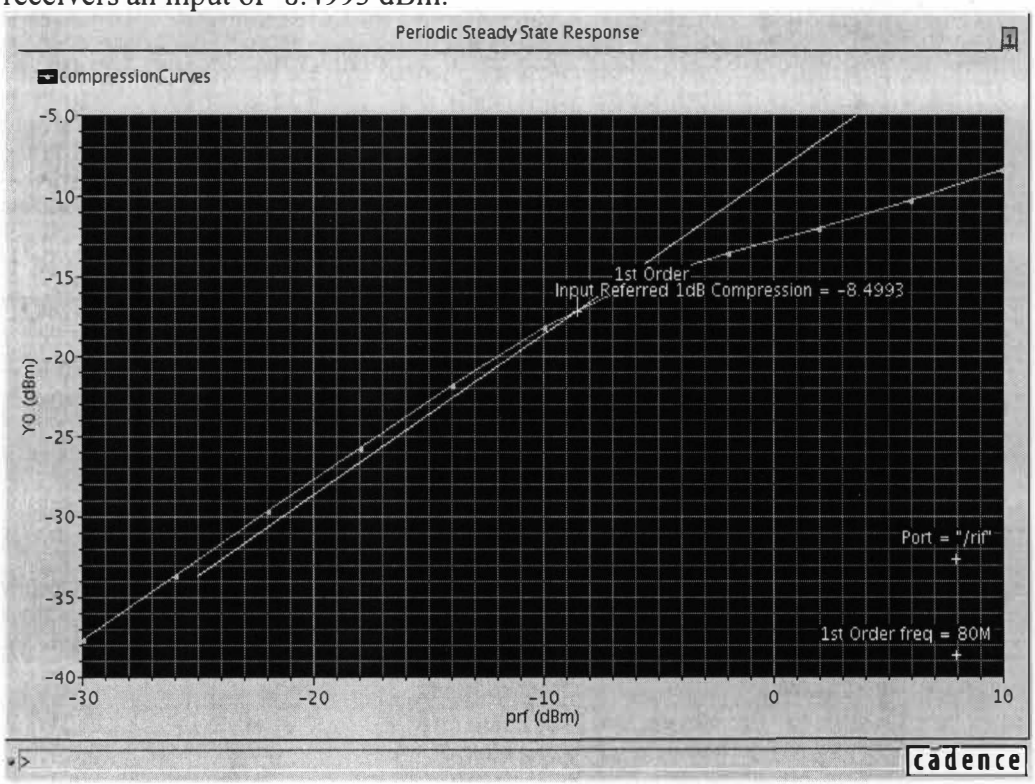


Figure 6-13 1-dB compression point.

IIP3 Intercept Point (Swept PSS Analysis)

To determine the third order inter-modulation point, the analysis is needed to use the Swept PSS with a periodic AC analysis simultaneously. The

third order inter-modulation (IM3) products will appear at 80 MHz. According to the simulation in Figure 6-14, the IP3 has showed 1.17236dB. A common approximate measure of IIP3 can be calculated in the following equation:

$$IIP3 = (P1dBm + 9.6dBm) = (-8.4993 + 9.6) = 1.1007(dBm)$$

The values between approximation and simulation are very accurate to each other.

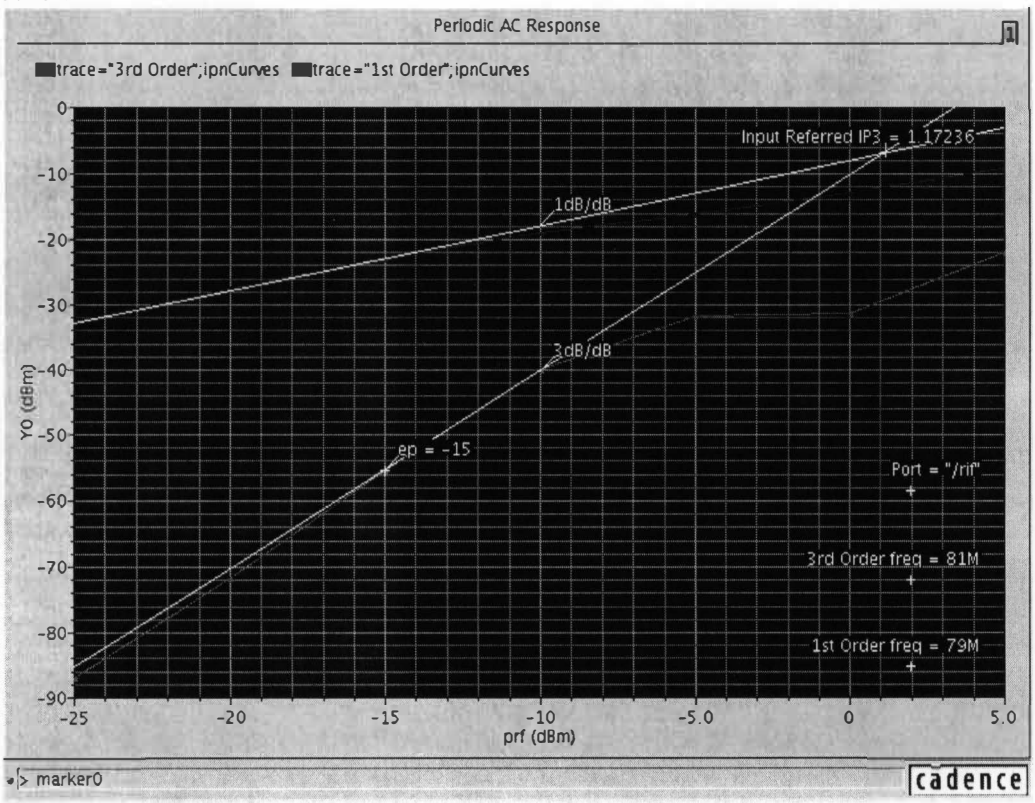


Figure 6-14 The IIP3 intercept point.

Noise Figure (Pnoise Analysis)

The Single SideBand Noise Figure (SSB NF) of the mixer was measured by using PSS analysis followed with a Periodic Noise (Pnoise) analysis. The

Pnoise analysis computes the total noise contribution to the input signal from the circuit. Noise can be picked up and contributed to the mixer from components such as resistors and transistors, input and output sources, and frequency translation in a circuit system. As seen in the Figure 6-15, the single sideband noise Figure is 16.7dB.

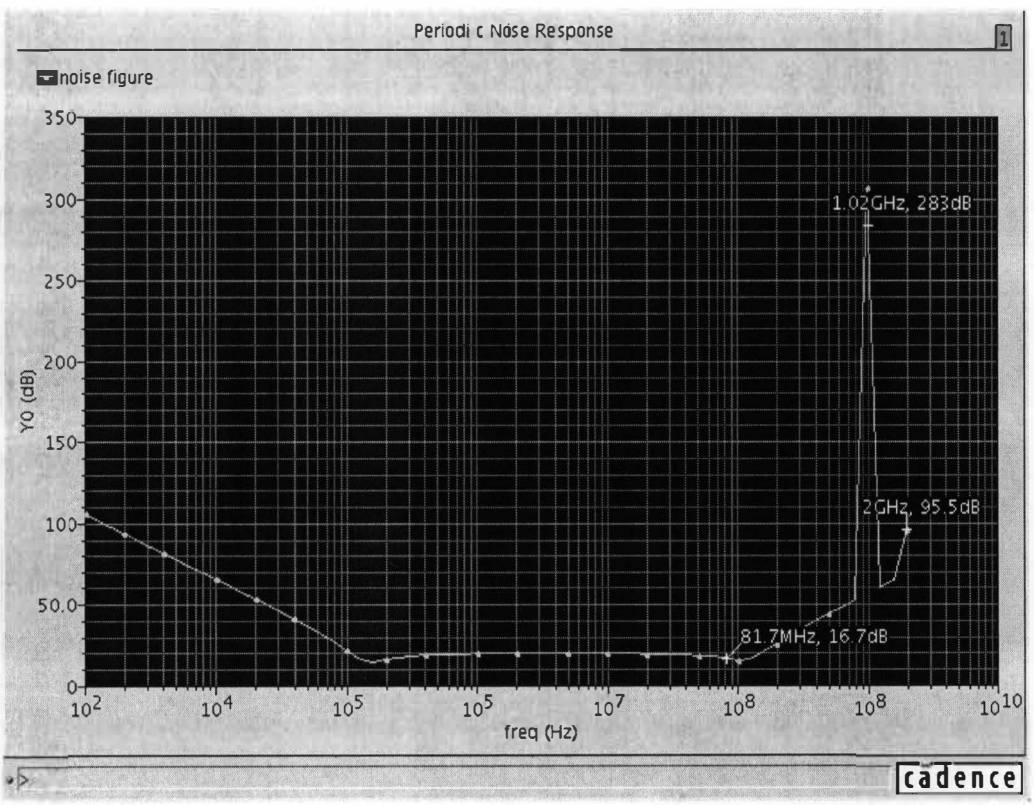


Figure 6-15 Noise figure in dB scale.

Note that there is a rapid noise pulse occurred at 1GHz in the Figure 6-15. The rapid noise is due to the Pnoise analysis picked up the LO signal as another noise contribution to the input signal from the circuit. Figure 6-16 shows the noise factor that LO signal occurs at 1GHz.

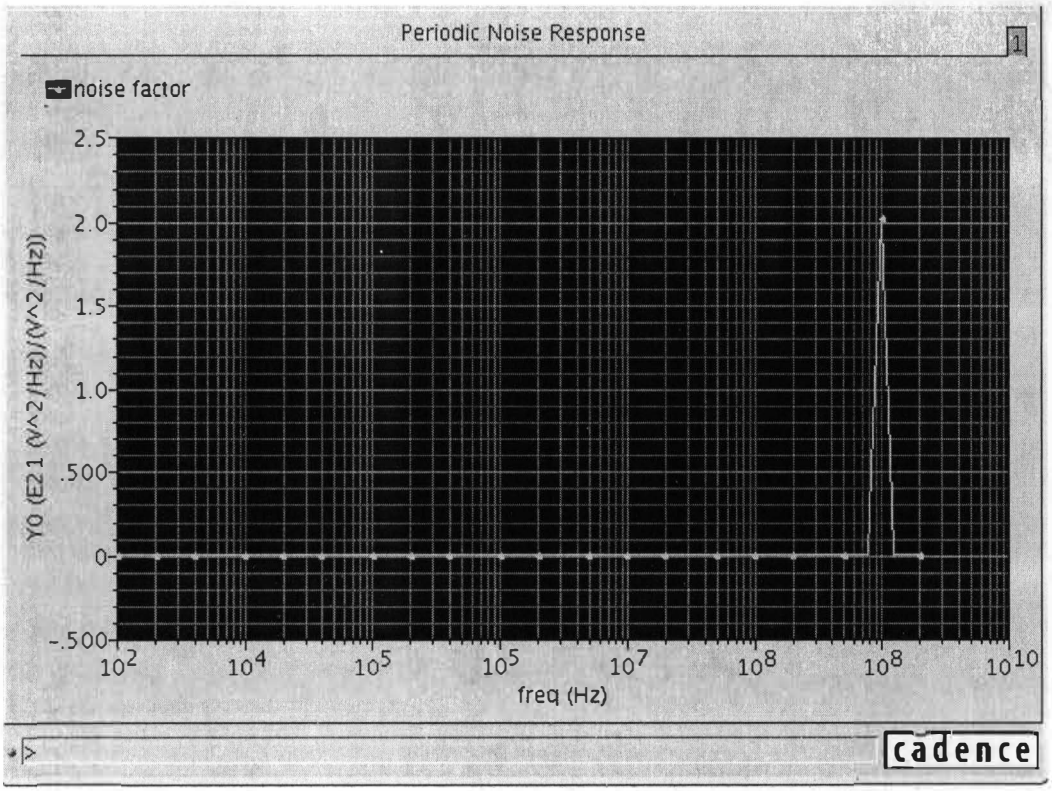


Figure 6-16 Noise factor.

IF Feedthrough Analysis (Periodic Transfer Function (PXF) Analysis)

The Periodic Transfer Function (PXF) analysis computes the transfer functions from any source at any frequency of the system to a single output at a single frequency. The PXF analysis is similar to PAC analysis which also includes frequency conversion effects. Based on the simulating of PXF analysis, Figure 6-17 shows the result of LO feedthrough for this type of mixer.

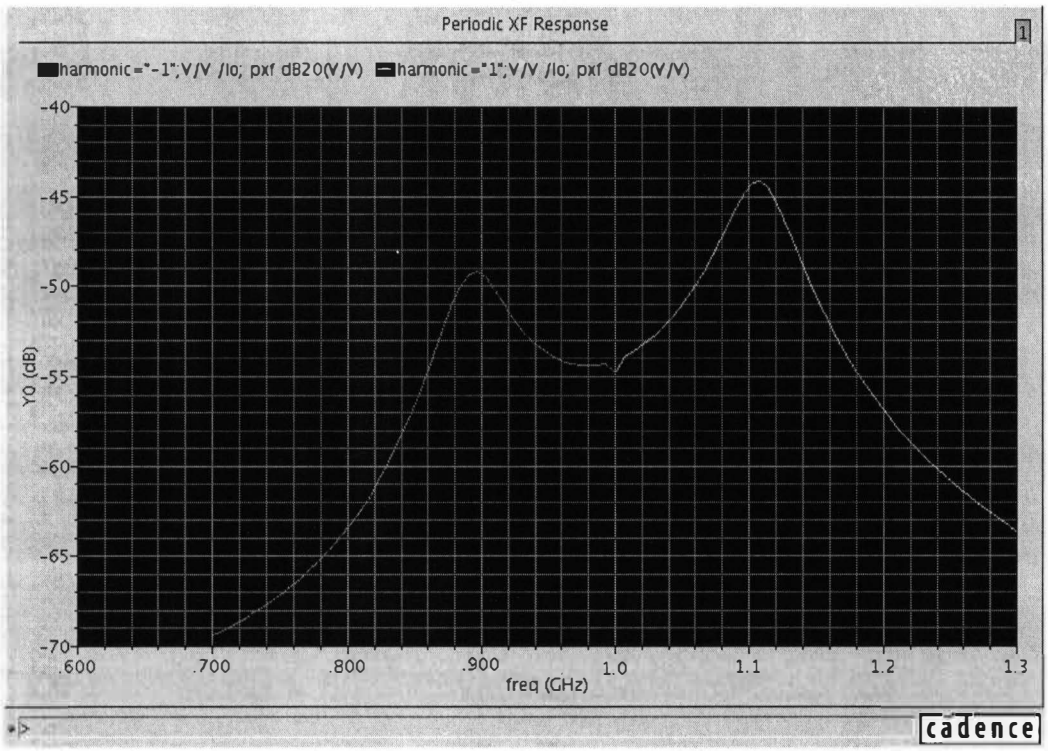


Figure 6-17 LO feedthrough.

Active Doubled Balanced Mixer

In previous chapters, one of major advantage of doubled balanced over a single balanced mixer is the LO feedthrough. Therefore, in this simulation, a doubled balanced mixer is designed and modified from the single balanced mixer to compare the difference with each other. In Figure 6-18, it is a schematic circuit for the doubled balanced mixer.

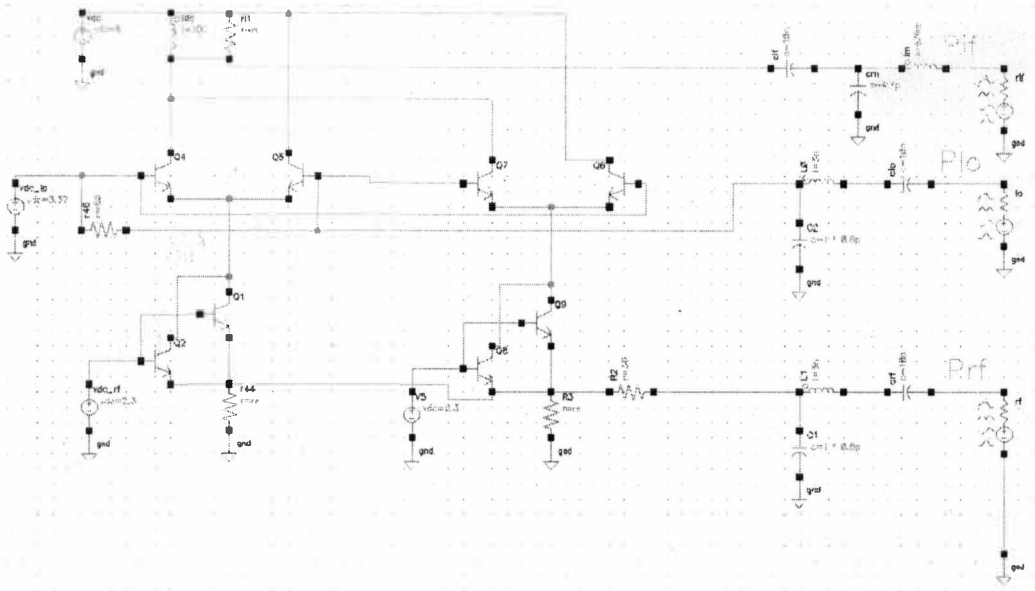


Figure 6-18 Schematic for the doubled balanced mixer circuit.

Frequency Spectrum Analysis (Periodic Steady State (PSS) Analysis)

Figure 6-19 shows the result of frequency spectrums generated from the singles. The figure indicates the IF signal located at 80.4MHz with voltage gain at -72.1dB that translated from the RF signal 918 MHz (-43.2dB) with the LO signal 1GHz (-65.3 dB). Note that the most un-wanted inter-modulation and harmonic signal is not attenuated enough away from the IF signal.

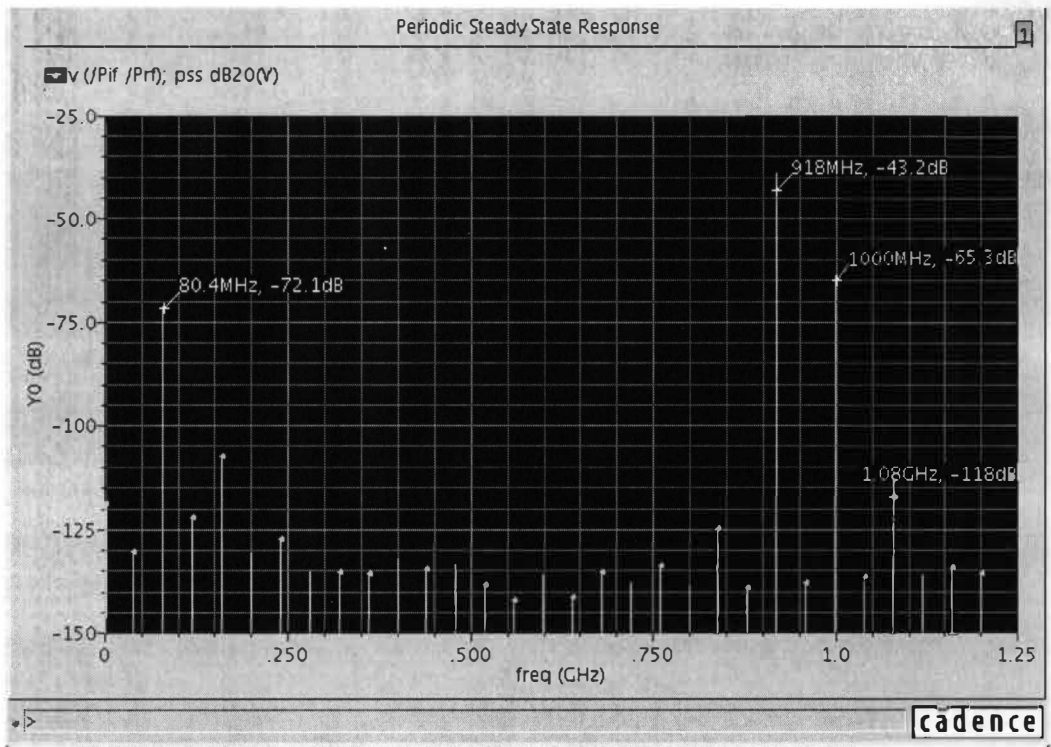


Figure 6-19 Output frequency spectrum.

Noise Figure (Pnoise Analysis)

As mentioning earlier, the Pnoise analysis can calculate how the total noise is contributed from components or the input signals in the circuit. In the Figure 6-20, the noise figure happened at the IF signal is 37.9dB which means that there were a lot of noise generated during the signals mixing.

Due to high noise figure of the system, most un-want inter-modulation and harmonic signals had increase and also interfere with the IF signal. In the Figure 6-19, it has showed those un-wanted inter-modulation and harmonic signals is increased and closed to the IF signal due to the noise contribution.

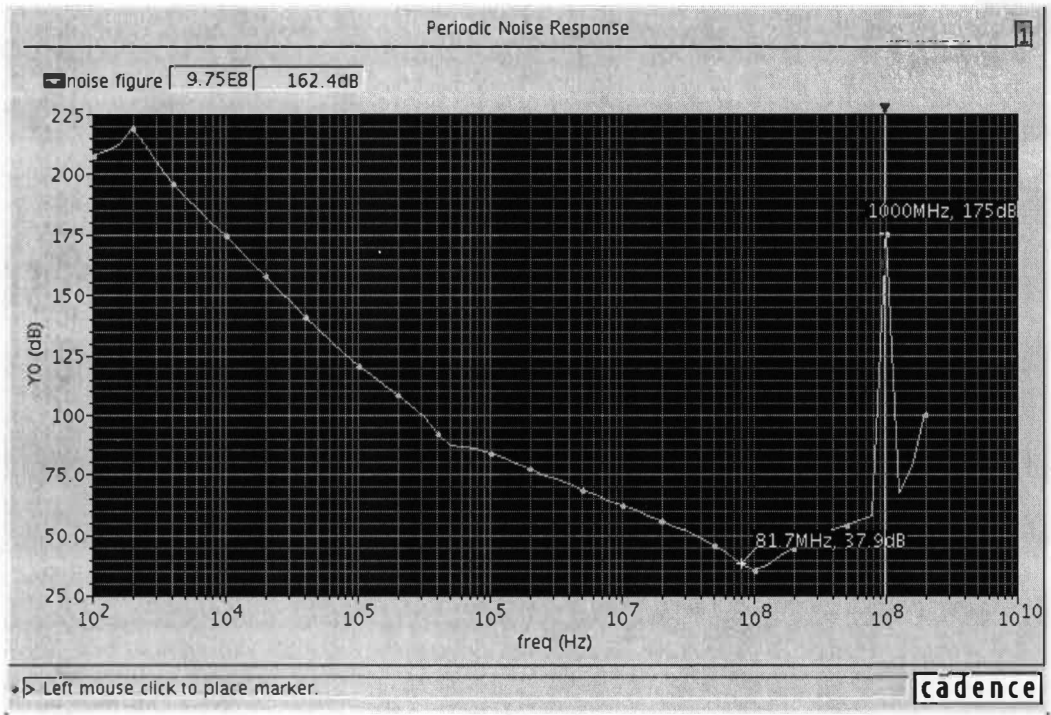


Figure 6-20 Noise figure in dB scale.

1-dB Compression Point (Swept PSS Analysis)

The Figure6-21 shows that the 1-dB compression point or P1dB occurs when the mixer receivers an input of -1.16358 dBm.

IIP3 Intercept Point (Swept PSS Analysis)

The simulations are combined to analyze two small signal input tones at the RF input port. These tones occur at the expected input RF signal of 920MHz and at an interfering signal or a neighboring channel frequency. The third order inter-modulation (IM3) products will appear at 80 MHz.

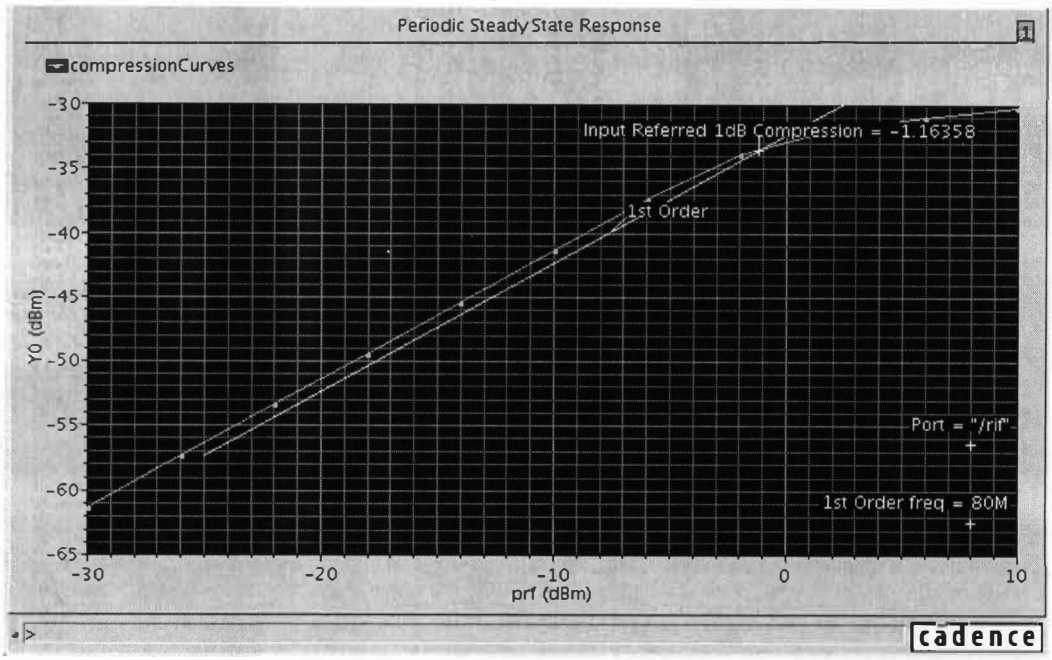


Figure 6-21 1-dB compression point.

According to the simulation shown in Figure 6-22, the IP3 has happened to be 7.4026dBm. Using a common approximate measure of IIP3, the value can be calculated in the following equation:

$$IIP3 = (P1dBm + 9.6dBm) = (-1.16358 + 9.6) = 8.43642(dBm)$$

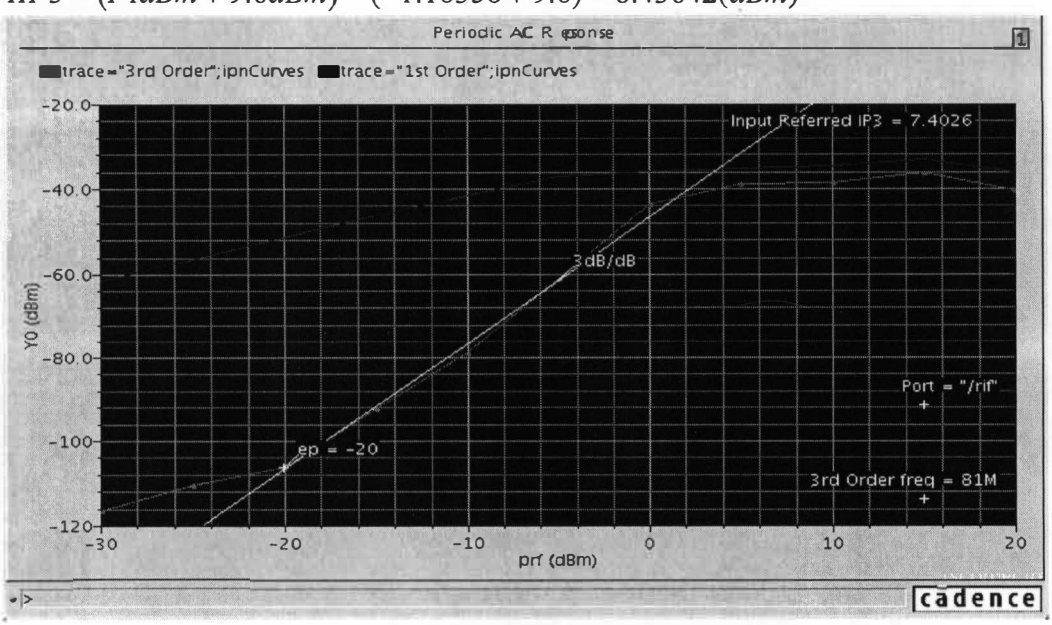


Figure 6-22 The IIP3 intercept point.

IF Feedthrough Analysis (Periodic Transfer Function (PXF) Analysis)

The Periodic Transfer Function (PXF) provides the measurement to analyze an issue of the LO feedthrough occurring in double balanced mixers. According to the result shown in Figure 6-23, the LO feedthrough occurring on 1GHz was cancelled and caused the result of the simulation to dramatically drop to -120dB.

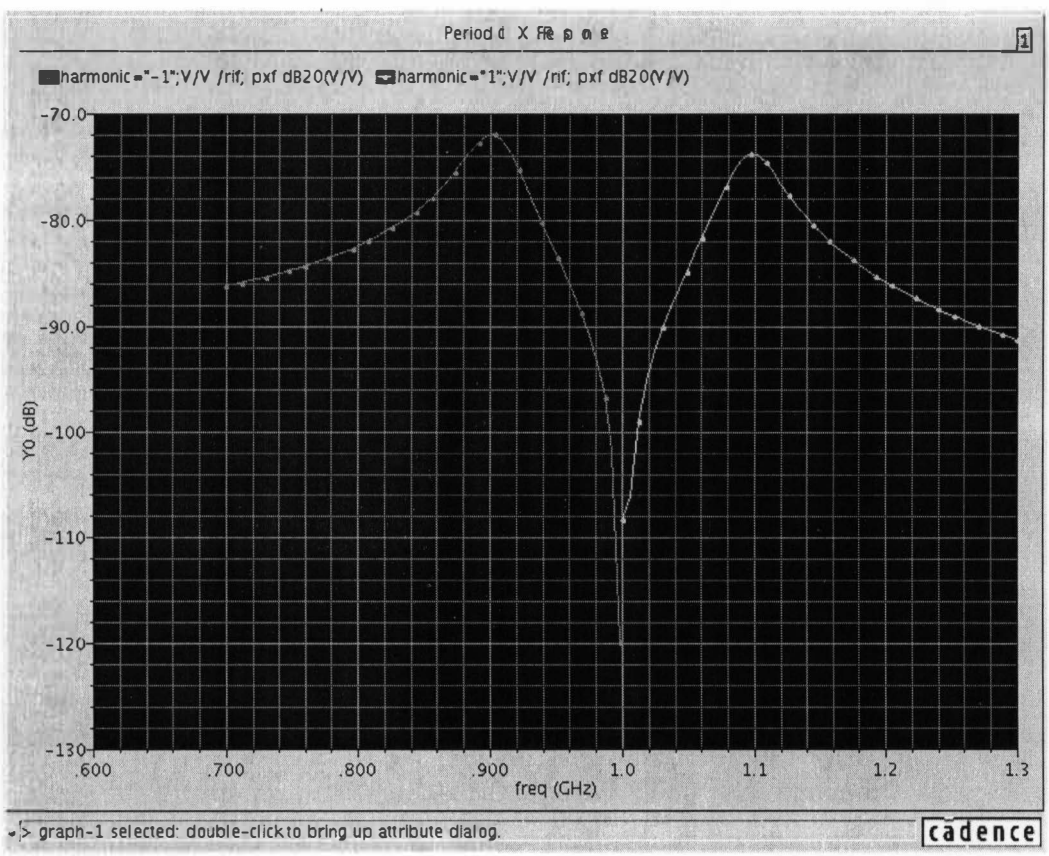


Figure 6-23 The result of LO feedthrough from double balanced mixers.

CHAPTER VII

CONCLUSIONS AND FUTURE WORK

In this thesis, the basic concepts of RFIC design are presented. Based on the studies of RF concepts, the system of a Heterodyne receiver and component tests with two types of active mixers are simulated at the end of this thesis. The results of simulations from the RF receiver and mixers can be compared and verified accordingly to the concepts and theories of RFIC technologies. In addition, the study of RF down-conversion receiver and mixers designs also shows how EDA simulation tools can help us to evaluate the performance of a circuit or system and determine ways to improve them.

From the first part of the evaluation, a design of the Heterodyne receiver was made to analyze how each RF component performed with high radio frequency in each stage. The receiver was meant to divide into three major stages: RF, IF, and base-band. By having three stages of signal processing in the receiver, it would be easy to reveal how the RF signal is translated to the base-band frequency.

The results showed that the most un-wanted inter-modulation and harmonic signals were generated by mixers during the RF signal down-converting. In RF stage, the LO signal can be chosen to be large so that those distinct image signals can appear far away from the targeted IF signal. However, in IF stage, LO signal has to be a matching or close frequency to the intermediate signal in order to bring the desired signal to the base-band. A close or matching frequencies, between LO and IF, may cause inter-modulation signals too close to eliminate them out for the next filtering component.

The second part of evaluation, the result from the double balanced mixer does improve the problem of LO feedthrough happened in the single balanced mixer. However, due to the switching transistors increase in the mixer, they increase noise contribution from the interval of time in which both transistors conduct current. Hence, the double balanced mixers generate more noise than single balanced mixers.

One way to reduce this degradation is to minimize the simultaneous condition interval of time. The LO signal must be sufficient and be provided to make the differential pair ideal for fastest switching operations. It is needed to be a square wave in a suitable level of magnitude. By meaning a "suitable" level of magnitude is that a large LO signal is better for the switching transistors but too big of LO signal may cause the transistors working out of saturation region.

Another way to reduce the noise that contributes from the switching transistor is to have a different semiconductor device called High Electron Mobile Transistor (HEMT) device as a switching component. InP-based HEMT devices have an excellent superior performance, demonstrated superior millimeter-wave, and low-noise performance compared to the InGaAs / AlGaAs pseudomorphic HEMTs on GaAs substrates [5] [21] [24].

RF design is a majority study in telecommunication territory. According to Cadence Corporation, there are so many branches by just talking about "RF design". They can broadly classify into such as: RF & microwave board design, communication system design, silicon RFIC design, signal integrity analysis, monolithic microwave integrated circuit (MMIC) design with different types of semiconductors (CMOS, GaAs, BiCMOS and so forth) , RF system-in-package (SIP) design, RF system-on-chip (SOP) design, device modeling design, and 3

dimension (3D) component design. Each branch of RF design also has a proper simulation tool to help designers verifying the performance of each system design. Since this thesis focused on analysis a mixing analog and digital signal system, the choice of the proper evaluation tools then is Virtuoso Custom IC design platform which is part of RF Design Environment (RFDE) from Cadence. The research trend of this thesis is dilatorily developed due to the deficiently technical support to the simulation tools. The Virtuoso Custom IC design platform was built up from ground zero in the lab. Without having a proper installation and configuration, the design environment with simulation tools would not function appropriately at all. It is necessary to have properly working evaluation tools to analyze the mixer circuits at the end of this study.

As future works, there are a lot of improvement to make this simulation results better regarding as the simulation tools and the circuits. They can be concluded in two parts. First, the Cadence Virtuoso platform has only provided an elementary amount of libraries and behavioral modeling. In order to have an accuracy analysis of RF circuit simulation, design kits are necessary to obtain from fabrication service vendors or organizations such as MOSIS. By have proper design kits including MOS and BJ transistors libraries and behavioral modeling, the circuits may re-design to obtain a better performance. In the final of this work, the re-design circuit can then be layout and packaged into an integrated circuit chip.

APPENDIX

The list of executable tool commands

This is the list of executable tool commands by having different simulation environments from Cadence Virtuoso design platform.

	Executable Tools Command	Size	Description
Front End	icde	S	Basic digitally and analog design entry
	icds	S	Front-end design (icde plus digital design environment)
	icms	M	Front-end analog, mixed signal, and microwave design (icds plus analog, mixed signal, and microwave environment and Diva LVS)
	icca	XL	Front-end design with floorplanning (icds)
Layout	layout	S	Basic layout design with interactive DRC
	layoutPlus	M	Basic layout design with automated design tools and interactive verification (Virtuoso, Virtuosos XL, Virtuoso Compactor, Diva)
Place and Route Systems	icca	L	Cell-based chip assembly
	msfb	L	Mixed-signal IC design, Exclude Place and Route software)
	icfb	XL	Front-to-back design (include most Cadence tools; no Dracula)
Chip Finishing	vce	S	Chip finishing for custom and digital designs using SoC Encounter and the Virtuoso Chip Editor on Open Access.

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