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A PERFORMANCE-DRIVEN ROUTING APPROACH FOR MCM-C

by

Qiong Yu

A Thesis
Submitted to the
Faculty of The Graduate College
in partial fulfillment of the
requirements for the
Degree of Master of Science
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Western Michigan University
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To
My wife
Lihong Ma

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Qiong Yu

A PERFORMANCE-DRIVEN ROUTING APPROACH FOR MCM-C

Qiong Yu, M.S.

Western Michigan University, 1994

In this paper, a new routing methodology for Ceramic MultiChip Module (MCM-C) is presented. In the proposed approach, the routing space is partitioned into several towers and the routing process is decomposed into three phases, namely, routing distribution, terminal assignment, and tower routing. During the routing distribution phase, the routing is uniformly distributed among towers. The locations of nets on the faces of each tower are assigned during the terminal assignment phase whereas the exact paths for the nets in each tower are determined during the tower routing phase.

The existing approaches to MCM routing are extensions of two-dimensional approaches to Printed Circuit Board (PCB) or Very Large Scale Integration (VLSI) routing problems. However, MCM is a truly three-dimensional routing environment and must satisfy delay, noise, and fabrication constraints. As a result, existing approaches may not be suitable for high performance MCM's.

Unlike existing approaches, the proposed approach is truly 3-dimensional and can satisfy delay, noise, and fabrication constraints. The proposed approach is also inherently parallel approach which makes it very effective for large MCM routing problems.

The routing approach proposed in this paper has been implemented and tested on MCC1 and MCC2 benchmarks as well as several randomly generated examples. Experimental evaluation confirms the validity of the methodology.

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CHAPTER I

INTRODUCTION

As VLSI technology advances, the traditional Printed Circuit Board (PCB) technology can no longer satisfy the increasing demand for higher packaging performance and higher interconnect capacity. MultiChip Module (MCM) technology in which bare dies are mounted and interconnected on a common substrate with high interconnect capacity promises to meet such demand as MCM technology eliminates a package level and provides shorter interconnect distance and higher interconnect capacity than the PCB technology [8, 25]. MCMs are generally categorized as three types, MCM-C, MCM-L, and MCM-D. MCM-L describes high density, laminated printed circuit boards. MCM-D covers modules with deposited metallic wiring on silicon or ceramic support substrates. MCM-C refers to the ceramic substrates, either cofired or low-dielectric constant ceramics [2, 10, 17]. MCM-C is also called thick film MCM since the layers formed in the cofiring process are relatively thick (typically 0.001 *inch* thick [22]). MCM-D allows only limited number of layers, typically 3 or 4 layers whereas there are large number of layers available in MCM-C and MCM-L. MCM-L, on the other hand, has smaller grid size and less number of nets than MCM-C. With advances in MCM-C technology, the number of layers in MCM-C has increased significantly. Recently a thick film MCM with 63 layers has been reported [24]. In addition, the number of nets to be interconnected on the substrate and the size of the substrate of a thick film MCM have also increased significantly. A thick film MCM with over 7000 nets and grid size of over 2000×2000 has been reported in [12]. The complexities of MCM-C routing problems are so large that it is virtually impossible to manually route the nets. After most nets are routed, it is impossible to route even the last few nets due to highly complicated routing patterns that have been

created. An autorouter which can completely route the nets for MCM-C needs to be developed.

An effective autorouter for MCM-C is not easy to develop due to the constraints that need be satisfied. As the clock frequency and the interconnect density in MCM-C increase, the delay and crosstalk noise concerns become critical in the routing problems [8, 23]. As a result, the delay and crosstalk constraints must be satisfied to guarantee the performance of the MCM. Due to the large number of layers that are present, the routing environment for MCM-C can be characterized as a three-dimensional routing medium. The number of layers is no longer the dominant factor in the routing problems of thick film MCMs. Instead, the delay, crosstalk, and fabrication constraints become critical factors. Another important characteristics of the routing problem for MCM-C is the high complexity. It is expected that the number of layers, number of chips mounted on a substrate, number of nets and grid size will continue to increase with the fabrication technology of thick film MCMs advances. As the complexity of the routing problems of MCM-C increases, uniprocessor approaches may not be suitable anymore and parallel approaches must be adopted for these problems. Therefore, an effective autorouter for MCM-C should be a three-dimensional router and should satisfy the delay, crosstalk, and fabrication constraints as well as amiable to parallel processing.

The routing environment for MCM-C is distinctly different from VLSI routing environment where there are typically two or three layers. As a result, most VLSI routing algorithms cannot be directly used for the routing of MCM-C. On the other hand, the routing of MCM-C is also significantly different from the routing of PCBs due to the higher complexities of MCM-C routing. The PCB routing algorithms with high time-complexity or space-complexity, therefore, cannot be used for the routing of MCM-C.

Several routing algorithms for MCMs have been developed [7, 11, 12, 13, 18]. In [7, 11, 18], the routing phase is decomposed into a pin redistribution phase,

layer assignment phase, and the detailed routing phase. An MCM SLICE router integrated pin redistribution and routing [12]. The basic idea of the SLICE router is to perform planar routing one layer at a time. The latest development in MCM routing is the V4R router [13]. The V4R router has reduced the time complexity and the number of layers used for routing as compared to the SLICE router. The V4R router uses two adjacent layers and routes one column at a time from left to right using four vias for most nets.

All the existing MCM routing approaches either route one layer or two adjacent layers successfully, thus converting a complex three-dimensional MCM routing problem into a set of conceptually simpler and well understood two-dimensional single-layer routing problems or two-layer routing problems. As a result these routing algorithms are time and space efficient. However, these approaches do not capitalize the full potential of the three-dimensional routing space. The two-dimensional perspective of a three-dimensional problem may lead to high local congestion, which may not be able to satisfy the crosstalk constraints or may lead to excessive number of layers thereby may violate the via constraints for very dense problems. In addition, most of the existing approaches aim to minimize the number of layers for routing while paying little attention to the delay and noise concerns.

In this paper, a new routing methodology for MCM-C is presented. In the proposed approach, the delay, crosstalk, and fabrication constraints have been converted into net-length, parallel-path-length, path-separation, and via constraints. The routing method is three-dimensional in nature and route all the nets while satisfying the constraints. In the proposed approach, the routing process is decomposed into several phases. First the routing density is uniformly distributed in two-dimensional XY plane as well as in the Z dimension. This distribution ensures that no specific region of the MCM routing space is over-congested. The routing distribution also allows us to partition the routing problem of the entire

routing space into the routing problems of several smaller regions called “towers”. At the end of this phase, the number of layers required for routing is known. After the completion of routing distribution, the exact positions for the terminals of the nets on the faces of each tower are assigned. The number of planar nets in each tower is maximized during the terminal assignment phase. After the terminal assignment phase, an estimate of the length of each net can be obtained. This characteristics of being able to estimate the routing resources (e.g. the number of layers and the length of the nets) before actually carrying out the routing itself which may be expensive in terms of time and memory requirements allows the proposed routing approach to be also used to judge the quality of the placement. At the end of this phase, the original three-dimensional routing problem has been converted to the routing of several smaller towers. As the routing problem in each tower is independent of the rest, all the towers can be processed in parallel. A tower can be partitioned recursively if necessary. Thus, the approach allocates more computing resources to the regions which require them. During the tower routing phase, we find a maximum set of planar nets for each layer which can be directly routed on the layer using an approximation algorithm which guarantees 0.60 of the optimal solution. This reduces the running time of the tower routing. The proposed approach differs from all the existing approaches primarily because the division of the problem in the proposed approach maintains the characteristics of the three-dimensional routing problem while the others convert the three-dimensional problem into a two-dimensional or two-layer routing problem. As a result, the approach can achieve better utilization of the three-dimensional routing space. Figure 1 illustrates the difference between the proposed approach and the existing approaches. In the approach shown in Figure 1(a), the routing is carried out on a layer at a time and continues to be carried out on the next layer if there remains any net to be completed. The SLICE router is an example of this approach. Instead of routing one layer at a time, the approach shown in

Figure 1(b) routes a pair of layers each time. The V4R router is an example of the second approach. Our approach divides the entire routing space into towers of which each contains all the layers (six layers in the figure) and the routing is carried out in all the layers (refer to Figure 1(c)). Though the proposed approach is intended for thick film MCMs, it can also be used for the routing of PCBs or laminated MCMs since the only difference between PCBs or laminated MCMs and thick film MCMs is that there are less number of nets and smaller grid size in the former cases.

The proposed approach has been implemented and tested on MCC1, MCC2 and various other randomly generated examples. Experimental results show that the proposed approach can complete the routing while satisfying the constraints. In addition, the approach provides a smooth trade-off between number of layers and constraints on the problem. Generally speaking, if a problem has less constraints, it can be routed in fewer number of layers. For example, MCC1 can be routed in 8 layers if the minimum path-separation is set to 2 whereas it can be routed in 12 layers if the minimum path-separation is set to 4. The rest

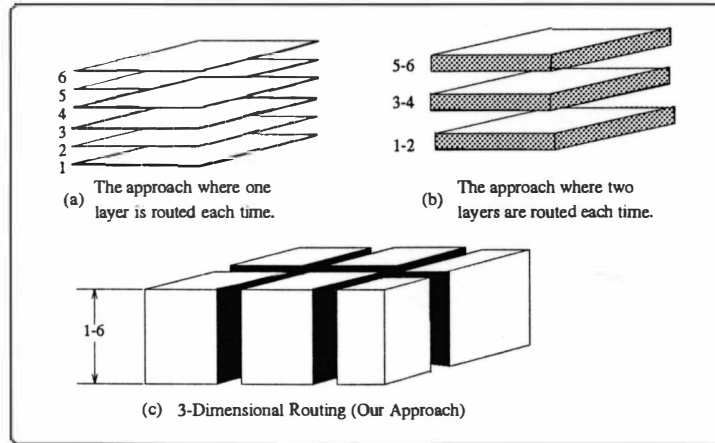


Figure 1. Different Strategies of Problem Division for a Six-Layer Routing Problem.

of this thesis is organized as follows: Chapter II introduces the basic concepts whereas Chapter III discusses the constraints. An outline of the approach is given in Chapter IV. Chapter V and Chapter VI contain the description of the terminal assignment and tower routing phases of the proposed methodology. The experimental results for an implementation of the methodology are discussed in Chapter VII. Conclusions are given in Chapter VIII.

CHAPTER II

NOTATIONS

A routing problem for a thick film MCM is specified by a set of nets to be routed over the substrate of the MCM, which is called a *netlist* and is denoted as \mathcal{N} . A *net* is a set of terminals which are to be made electrically equivalent. To *route* a net is to interconnect its terminals by electric wires. The maximum length of an electric wire between any pair of source and sink terminals of a net is the *length* of the net. There are two kinds of terminals of the nets. The electrical connections between the chips and substrate are made by attaching wires from the I/O pads on the device side of the chip to the appropriate points on the bottommost layer on the substrate called the *chip layer*. These points are called *die terminals*. The die terminals are used to make interconnections from bare dies to bare dies or from bare dies to the MCM. The terminals which are located at the periphery area of the chip layer are used to make interconnections from the MCM to the outside world and are called *I/O terminals*. The fabrication process requires the signal wires to be separated by a minimum distance. A 3-dimensional grid is superimposed upon the chip layer and routing layers in an MCM such that the signal wires can only be laid out along the grid lines to meet the minimum distance requirement (refer to Figure 2(a)). A XYZ Cartesian coordinate system is set up such that Z axis is perpendicular to the chip layer, X and Y axes are parallel to the boundaries of the substrate, and the origin is at a corner of the MCM on the chip layer (see Figure 2(a)). A *point* is an intersection between grid lines. We assume that each terminal of a net is located at a point on the chip layer.

Let the size of the substrate be $l \times w$ and the number of routing layers be k . Then, the cube on top of the substrate, in which the signal wires are to be laid

out, is called *routing space*. The dimensions of the routing space are then $l \times w \times k$. The substrate is partitioned into a set of tiles. Each *tile* is a rectangular area of the substrate. The cube on top of a tile is called a *tower*. The partitioning of the substrate into tiles is equivalent to the partitioning of the routing space into towers. In this paper, we use tiles and towers interchangeably. A boundary plane of a tower is called a *face* of the tower while a boundary of a tile is referred to an *edge* of the tile. A vertical line in a tower is called a *pillar* whereas a horizontal line in a tower is called a *column*. The terminologies associated with a tower are shown in Figure 2(b).

Given a net $n = (t_1, t_2, \dots, t_k)$ consisting of terminals t_1, t_2, \dots and t_k , we define a 3-dimensional Steiner tree for n as a tree in the 3-dimensional grid, interconnecting t_1, t_2, \dots and t_k , which are called *demand points*, and some arbitrary points which are called *Steiner points* (see Figure 2(a)). The MCM routing problem can be formally defined as finding a 3-dimensional Steiner tree for each net in the netlist such that no 3-dimensional Steiner trees of two different nets overlap or intersect. The 3-dimensional Steiner tree for a net n is also called the interconnection of n . A part of the 3-dimensional Steiner tree for n which interconnects two terminals of n is called a *path* of n . A point that is on both the route of a net and the face of a tower is called a *terminal* of the net in the tower. The routing of

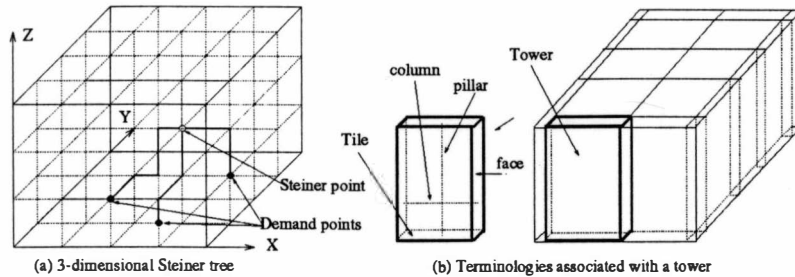


Figure 2. Routing Environment for a Thick Film MCM.

a net can be decomposed into two steps. The first step is to find out the towers that the net passes through and the location of the terminals in these towers. The second step is to route the net within each of these towers that the net passes through. The routing of a net within a tower is to find a 3-dimensional Steiner tree, interconnecting all the terminals of the net in that tower.

CHAPTER III

CONSTRAINTS

The primary requirements for the MCM routing are to satisfy the delay, noise, and fabrication constraints. The delay constraints are introduced to ensure that the MCM operates correctly for the designed clock frequency. The noise constraints must be met so as to avoid the inadvertent logic transitions caused by excessive noise. The fabrication constraints should be satisfied so that the resulting MCM can be manufactured with high yield. These constraints, however, cannot be handled directly by a router. They must be converted into geometric constraints which are then satisfied in the routing. The geometric constraints include the net-length, path-separation, and parallel-length constraints. In the following, we discuss how the delay, noise, and fabrication constraints are converted into the geometric constraints.

1. Delay constraints are converted into net-length constraints:

The maximum clock frequency for which a system can operate correctly is limited by the delay of critical paths. For example, in the case that two flip flops are driven by the same clock source and are on a critical path, the total delay between the flip flops must be less than the clock period to ensure that the MCM can operate correctly. The total delay between the flip flops is determined by the equation [8]: $t_{total} = t_s + t_{prop} + t_{settle} + t_r + t_{skew}$ where t_s is the total internal delay inside the devices on the source end, t_s is the corresponding delay on the receiving end, and t_{skew} the clock skew. t_s , t_r , and t_{skew} are determined independent of the routing. t_{prop} and t_{settle} are the delays affected by interconnections. t_{prop} is the delay between the time when the output at the source end reaches the 50% point of its logic swing and the time when the input at the receiving end reaches the 50% point of its logic swing and t_{settle} is the time for the noise of the signal

to settle down so that the signal can be safely sampled. The propagation delay t_{prop} can be further partitioned as the sum of t_{flight} and $t_{rise-time-degradation}$ where t_{flight} is the time-of-flight delay and $t_{rise-time-degradation}$ is the delay caused by the increase in rise time between the source end and receiving end of the line due to the line losses. When the line losses are controlled, e.g. in the case of first incidence switching, the time-of-flight becomes the dominating factor. However, if the first incidence switching is not achieved, the propagation delay might be significantly increased, to as much as five times as the time-of-flight delay. The first signal arrive at the receiving end of the line must have sufficient voltage to switch the receiver. (The voltage should exceed V_{IH} on a $0 \rightarrow 1$ transition or V_{IL} on a $1 \leftarrow 0$ transition). The situation in which there is sufficient voltage is called *first incidence switching* [8].

The first incidence voltage at the end of a matched terminated line is calculated by the following equation: [8]

$$V_{first} = V_{in} \frac{Z_0}{R_{out} + Z_0} e^{-\mathcal{R}l/2Z_0}$$

where V_{in} is the open circuit output voltage swing of the driver, l is the length of the line, \mathcal{R} is the unit resistance of the line, Z_0 is the impedance of the line, and R_{out} is the resistance of the output device. To achieve the first incidence switching, we must have $V_{first} \geq V_{IH}$ or $l \leq \frac{2Z_0}{\mathcal{R}} \ln \frac{V_{in}Z_0}{V_{IH}(R_{out}+Z_0)}$. Whence the the first incidence switching is achieved, the propagation delay is mainly determined by the time-of-flight which can be calculated by the following equation [3]:

$$t_f = \frac{l\sqrt{\epsilon_r}}{c_0} \quad (3.1)$$

where l is the net length, ϵ_r is the dielectric constant of the insulator, and c_0 is the light speed in vacuum.

As there is a maximum time-of-flight delay (t_{max}) for each critical net to satisfy the clock frequency requirement, we have $\frac{l\sqrt{\epsilon_r}}{c_0} \leq t_{max}$ or $l \leq \frac{c_0 t_{max}}{\sqrt{\epsilon_r}}$.

By combining the time-of-flight delay constraint and the first incidence switching constraint, we obtain the *net-length constraints* which is shown as follows: $l_i \leq \min(\frac{2Z_0}{R} \ln \frac{V_{in}Z_0}{V_{IH}(R_{out}+Z_0)}, \frac{c_0 t_{max}}{\sqrt{\epsilon_r}})$, where l_i is the length of net i .

In our routing approach the net-length constraints are satisfied to meet the delay requirement in the MCM.

2. Noise constraints are converted into the path-separation and parallel-length constraints: The excessive electrical noise can cause inadvertent logic transition and can increase the delay for the noise to settle down (t_{settle}). Therefore, the noise must be controlled to ensure that the correct output is generated and the delay is minimized.

The noises generated by interconnections are crosstalk and reflection noises. The reflection noise occurs whenever the interconnection of a net branches, terminates, or changes direction. The level of reflection noise depends on how the line is terminated and there is no simple model for the reflection noise. However, as a general guideline, the number of vias and bends in the interconnection of a net should be minimized to reduce the reflection noise. Mutual inductance and capacitance between the parallel paths of different nets create unwanted electrical coupling known as *crosstalk noise*. Whenever a signal edge travels down a signal wire, both forward and backward crosstalk noise pulses are induced in the neighboring wires.

Crosstalk noise is determined by the capacitive coupling, K_C , and inductive coupling, K_L . The coupling between nets can be minimized by making sure that no paths of these two nets are in parallel for too long or too close to each other.

Capacitive coupling K_C and inductive coupling K_L between adjacent signal paths add at the near end of the quiet line and subtract at the far end. The maximum noise voltage at the near end can be approximated by [8]:

$$V_n \approx K_B \frac{2V_S}{vT_1} l \quad \text{if } l < \frac{vT_1}{2}$$

$$\approx K_B V_s \quad \text{if } l > \frac{v}{2}$$

where $K_B = (K_C + K_L)/4$ is the coupling coefficient, V_s is the voltage swing on the active line, $v = c/\sqrt{\epsilon_r}$ is the propagation velocity of electromagnetic waves in the dielectric, T_1 is 0%-100% rise time of the signal, and l is the length for which the paths are in parallel.

The maximum noise voltage at the far end is given as [8]:

$$V_f = K_F \frac{2 V_s l}{v T_1}$$

where $K_F = (K_C - K_L)/4$ is the coupling coefficient.

As can be seen from the equations for the noise voltage, the crosstalk noise depends on the length of two parallel paths l and the capacitive coupling K_C and inductive coupling K_L between adjacent signal paths. K_C and K_L depends on the the length of parallel paths and the distance between the two parallel paths. As a result, the distance between paths of two nets and the length of parallel paths of different nets have to be controlled to minimize the crosstalk noise.

We have to distinguish the case where the paths of nets are on the same layer from the case where the paths of nets are on the different layers due to the presence of dielectric material between layers. Therefore, the *homogeneous parallel-length constraints*, where the length of two parallel paths between nets i and j which are on the same layer must not exceed \mathcal{L}_{ij}^P , are introduced. On the other hand, if the paths of nets i and j are on the different layers, the length of two parallel paths between nets i and j must not exceed \mathcal{L}_{ij}^Z , which are called *inhomogeneous parallel-length constraints*. Both \mathcal{L}_{ij}^P and \mathcal{L}_{ij}^Z depend on the distance between the two parallel paths of net i and net j . The closer these two paths are, the smaller \mathcal{L}_{ij}^P or \mathcal{L}_{ij}^Z becomes.

In addition, if the paths of two nets are too close to each other, the excessive crosstalk noise will be generated. The *homogeneous path-separation constraints*

where the distance between the paths of net i and net j which are on the same layer must be greater than a certain value and *inhomogeneous path-separation constraints* where the distance between the paths of net i and net j which are on different layers must be greater than a different value have to be satisfied.

In our approach, both the parallel-length and the path-separation constraints are met to control the crosstalk noise.

3. Fabrication Constraints are converted into the layer-number, via-type, and via-number constraints: Another constraint in thick film MCMs is associated with fabrication process. In order to achieve high yield in manufacturing MCMs, the number of routing layers, the type of vias, i.e. stacked vias, staggered vias, or spiral vias, and the maximum number of stacked vias of each net should be specified. In our approach, the specifications of the number of routing layers, the type of vias, and the number of stacked vias for each net are satisfied.

In summary, the delay, crosstalk noise, and fabrication constraints are converted into the geometric constraints such as net-length, path-separation, parallel-length, layer-number, via-type, via-number constraints (refer to Figure 3). The geometric constraints are given as the input to our approach. Our approach generates the routing for the netlist with the minimum number of layers while satisfying all the constraints. Further discussion on the issue of constraints can be found in [3, 8, 23].

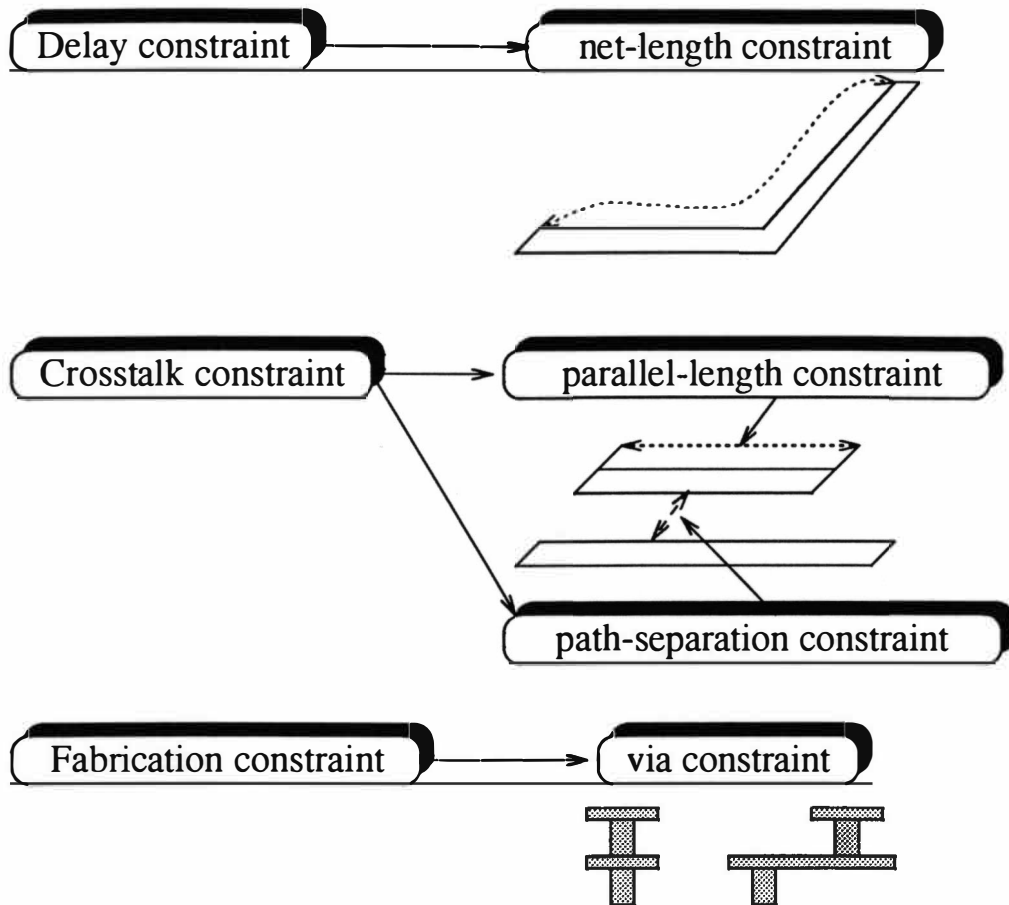


Figure 3. Performance Constraints are Converted into Geometric Constraints.

CHAPTER IV

OVERVIEW OF THE PROPOSED APPROACH

The routing for thick film MCMs is carried out in a three-dimensional routing space using a recursive formulation. Due to the complexity of routing in the entire three-dimensional space, the routing is completed in several different phases. In the following, the different phases of the proposed approach are described.

1. Tiling: The MCM substrate is partitioned into a set of tiles. Tiling takes care of splitting the substrate into smaller regions in a recursive manner such that the denser area of the tile is partitioned into more number of tiles when compared to the less denser ones.

2. Off-Tile Routing: The terminals which are not located on the edges of the tiles are routed onto the faces of the towers so that the characteristics of all the terminals are similar and no distinction need be made between them.

3. Routing Distribution:

(a) *XY-Plane Routing Distribution:* A Steiner tree for each net in terms of the tiles through which the net passes is determined. The objective of this phase is to uniformly distribute the amount of wiring over the XY plane. We have developed an algorithm called multi-net-hierarchical routing to build the Steiner trees for the nets based on hierarchical routing algorithm [4]. At the completion of this phase, the number of layers required for routing the nets can be estimated based on the level of routing congestion in each tile. In addition, the length of each net in the XY direction can also be estimated quite accurately as the length of each net in the XY direction may change only marginally during the tower routing phase. By finding the Steiner trees for critical nets first, the net-length constraint for these critical nets can be met since the length of each net in the

XY direction may change only marginally during the tower routing phase and the length of each net in Z dimension is usually a fraction of the total length.

(b) *Z-Dimension Routing Distribution*: The layer on which each net passes each tower face is determined. The objective of this phase is to uniformly distribute the congestion along the Z direction. At the completion of this phase, we would have already computed the total number of layers required for routing. If the constraints on the number of layers cannot be met, the routing or placement has to be carried out again. In addition, since the length of each net in the Z direction can be estimated, the total length of each net along the XY-dimension as well as the Z-dimension can be estimated accurately.

4. Terminal Assignment: The exact location of the terminal of each net on the face of each tower is determined. The objective of this phase is to maximize the set of planar nets on each layer in a tile while assigning the terminals. After terminal assignment, the length of those nets in the planar set is known. Notice that at the end of each phase we get a better estimate of the length of the nets in an incremental fashion finally leading to the exact length. In addition, the path-separation constraints are met by assigning each terminal separated from the other terminals by the required distance.

5. Tower Routing: The nets are routed within each tower. We use an approximation technique to find a maximum set of planar nets which can be routed directly and fast to reduce the running time of tower routing. The remaining nets are routed one at a time using three-dimensional Soukup's technique [20]. We specify the parallel-length constraints, path-separation constraints, via-type, and via-number constraints in the tower routing. The path-separation constraints are satisfied by using "cable routing". The parallel-length, via-type, and via-number constraints are satisfied by forcing the signal path of a net to change direction if any constraint is to be violated.

The overview of our approach is shown in Figure 4. As can be seen from the figure, the routing problem of the entire routing space is converted into the routing problems of several smaller towers which are independent from each other. For complex tower routing problems which are too large due to either the size of the tile or the large number of nets present in the tile, we apply our approach in a recursive fashion to break up the original problem into several smaller tower routing problems and solve them individually (see Figure 5). As a result, the amount of computing resources spent on a routing region (tower, sub-tower, sub-sub-tower) is directly proportional to its complexity. On the other hand, during the routing process, more and more information about the use of routing resources become available after each phase. This characteristics makes our approach very flexible and can be used not only for the routing of thick film MCMs but also for estimating the required routing resources to evaluate the placement quality for a placement tool. Furthermore, as each of the tower routing problem is independent of the other, we can assign the problem of routing a tower to a different processor and hence achieve a better time complexity if a parallel computing environment is used. The best utilization of routing space is possible due to the uniform distribution of routing and the three-dimensional perspective of our approach. Furthermore, the delay, crosstalk noise, and fabrication constraints are met in our approach.

For the sake of brevity, only the important phases of the proposed approach will be discussed.

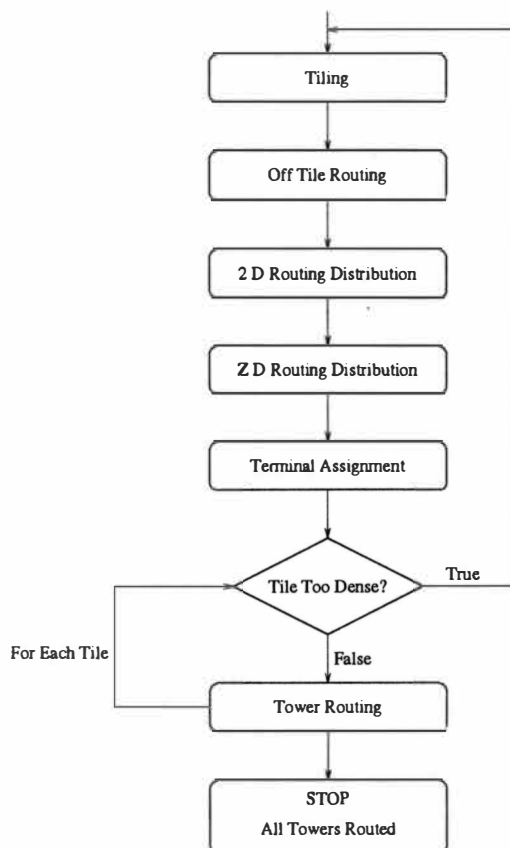


Figure 4. Overview of Our Approach.

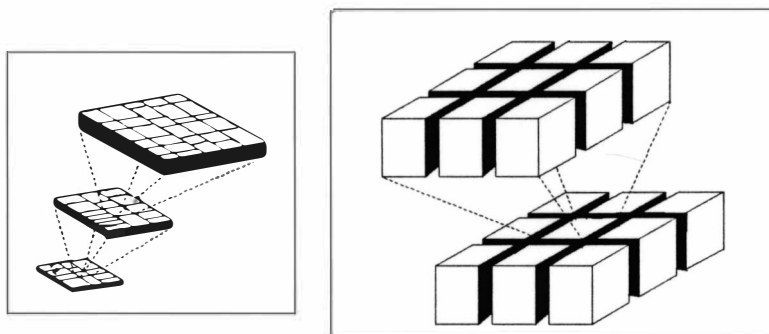


Figure 5. Routing Space is Recursively Partitioned.

CHAPTER V

TERMINAL ASSIGNMENT

In this chapter, we discuss the terminal assignment phase which finds the exact locations of the terminals of each net in the towers through which the net passes. The objective of terminal assignment phase is to maximize the number of planar nets in each tower while satisfying the path-separation constraints. In this chapter, we assume that all the nets are two-terminal nets. The proposed algorithms can be easily extended to handle the multi-terminal nets. We omit this extension for the sake of brevity.

Since the towers and the layers in these towers where the terminals of the nets are located have been determined during the routing distribution phase, we can only permute the terminals of the nets along a tile edge. The terminal assignment is carried out by bipartitioning the substrate recursively. At each level of bipartitioning, the set of tiles is partitioned into two sets of tiles which are of the same sizes or similar sizes and the locations terminals along the partition boundary

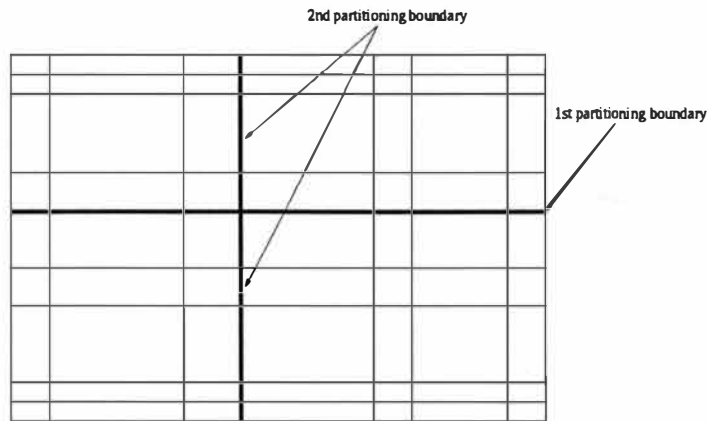


Figure 6. Substrate is Bipartition Hierarchically.

is determined (refer to Figure 6). We bipartition the substrate recursively and assign only the terminals along the partition boundary at each hierarchy level so that the global perspective of the net distributions can be considered during the terminal assignment. At the bottom level of bipartition, partitions corresponds to tiles and all the terminals have been assigned.

In the following discussion, we assume that the nets under consideration pass the same tile edge and the terminals of these nets on the tile edge can be permuted. In addition, the tile edge under consideration is along the partition boundary. The terminal locations are determined in two steps. During the first step, we find the ordering of the terminals along a tile edge so as to achieve the maximum number of planar nets. Later on, the terminals are assigned to exact locations according to the ordering of the terminals and the path-separation constraints.

Ordering Terminals

We order the terminals on a tile edge to minimize the number of crossings between the nets and, thereby, maximizing the number of planar nets. The *crossing* between two nets is defined as the intersection between the two line segments connecting the terminals of the two nets respectively. *Planar nets* are the nets without any crossing between them.

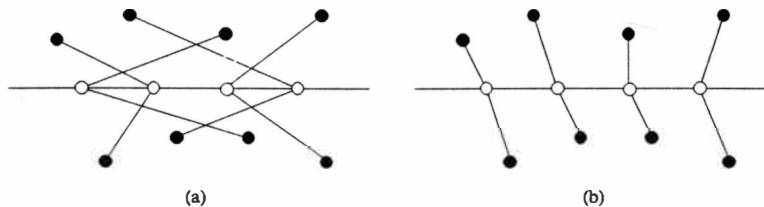


Figure 7. Terminal Permutation to Minimize the Number of Crossings.

An example of minimizing the number of crossing while ordering the terminals on a tile edge along the partitioning boundary is shown in Figure 7. Sometimes, it is desirable to uniformly distribute the crossings over the substrate. In order to uniformly distribute the crossings over the substrate, the number of crossings on both sides of the partitioning boundary should be balanced at each level of hierarchy. An example of balancing the number of crossing on both sides of a tile edge is illustrated in Figure 8.

In order to show how the terminals can be ordered so as to minimize the number of crossings or balance the number of crossings on both sides of a tile edge, we introduce a relation called *crossing relation* and a function called *crossing function*. Let the tile edge under consideration be \mathcal{E} . Let the terminals of the net n_1 and n_2 on \mathcal{E} be t_1 and t_2 . We assume that the tile edge is a horizontal line (The case of vertical tile edge can be similarly handled.). Let the tiles above and below \mathcal{E} be T_1 and T_2 respectively. The *crossing relation* $t_1 \prec t_2$ is defined as follows: $t_1 \prec t_2$ if there is no crossing between n_1 and n_2 in both T_1 and T_2 when t_1 is assigned to the left of t_2 . The *crossing function* $C(t_1, t_2)$ is defined as follows:

$C(t_1, t_2) = 1$ if the crossing between n_1 and n_2 is above \mathcal{E} when t_1 is assigned to the left of t_2 and $C(t_1, t_2) = -1$ if the crossing between n_1 and n_2 is below \mathcal{E} when t_1 is assigned to the left of t_2 and $C(t_1, t_2) = 0$ otherwise

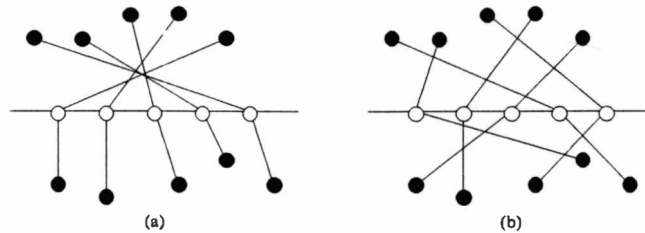


Figure 8. Terminal Permutation to Balance Crossing on Both Sides.

The crossing relation is used to define the ordering between the terminals of two nets to avoid the crossing whereas the crossing function is used to show where the crossing is in case that the crossing cannot be avoided. The crossing relation and the crossing function are determined by the terminals of the nets above \mathcal{E} , by the terminals of the nets below \mathcal{E} , or by all of them. In the following, we discuss how the crossing relation and crossing function are determined in each one of these cases.

1. If n_1 and n_2 pass T_1 and not all of them pass T_2 (Figure 9(a)(b)(c)(d)),

(a) If n_1 and n_2 pass two different edges e_1 and e_2 respectively in T_1 , then $t_1 \prec t_2$ if e_1 is to the left of e_2 or $t_2 \prec t_1$ if e_1 is to the right of e_2 . In addition, $C(t_1, t_2) = 0$. In the example shown in Figure 9(a), $t_1 \prec t_2$ and $C(t_1, t_2) = 0$.

(b) If n_1 and n_2 pass the same edge e in T_1 , the locations of the terminals of n_1 and n_2 on e are p_1 and p_2 respectively, and p_1 and p_2 are fixed, then $t_1 \prec t_2$ if p_1 is to the left of p_2 or $t_2 \prec t_1$ if p_1 is to the right of p_2 . In addition, $C(t_1, t_2) = 0$. In the example shown in Figure 9(b), $t_1 \prec t_2$ and $C(t_1, t_2) = 0$.

(c) If n_1 and n_2 pass the same edge e in T_1 , not all the locations of the terminals of n_1 and n_2 on e are fixed, and one of the two nets terminates at e (refer to Figure 9(c)), then the crossing relation between t_1 and t_2 is undefined. In addition, $C(t_1, t_2) = 0$.

(d) If n_1 and n_2 pass the same edge e in T_1 , not all the terminal locations of n_1 and n_2 on e are fixed, and none of the two nets terminates at e , then the next tile adjacent to e is to be considered, and the above procedures (a)(b)(c)(d) are recursively applied to this tile until the crossing relation and the crossing function of t_1 and t_2 can be determined. In the example shown in Figure 9(d), we cannot decide the crossing relation and crossing function between t_1 and t_2 in T_1 . Instead we consider the tile T and decide the crossing relation and crossing function between t_1 and t_2 in tile T . Since e_1 is to the left of e_2 , $t_1 \prec t_2$ and $C(t_1, t_2) = 0$.

2. If both n_1 and n_2 pass T_2 but not both of them pass T_1 , we apply the method described above to T_2 to define the crossing relation and crossing function between t_1 and t_2 .

3. If n_1 and n_2 pass both T_1 and T_2 , we apply the method described above to both T_1 and T_2 to define crossing relation between t_1 and t_2 . Let the crossing relations between t_1 and t_2 defined in T_1 and T_2 be \prec' and \prec'' respectively. We define the crossing relations and crossing function in the following way.

(a) If $t_1 \prec' t_2$ and $t_1 \prec'' t_2$ ($t_2 \prec' t_1$ and $t_2 \prec'' t_1$), then $t_1 \prec t_2$ ($t_2 \prec t_1$). In addition, $C(t_1, t_2) = 0$ (refer to Figure 9(e)).

(b) If $t_1 \prec' t_2$ and $t_2 \prec'' t_1$ ($t_2 \prec' t_1$ and $t_1 \prec'' t_2$), then no matter how the terminals are permuted on the edge \mathcal{E} , there is a crossing between the two nets. The crossing relation between t_1 and t_2 is undefined in this case. In addition,

$$C(t_1, t_2) = 1 \text{ if } t_2 \prec' t_1 \text{ and } t_1 \prec'' t_2.$$

$$C(t_1, t_2) = -1 \text{ if } t_1 \prec' t_2 \text{ and } t_2 \prec'' t_1.$$

For example, $C(t_1, t_2) = 1$ in Figure 9(f) while $C(t_1, t_2) = -1$ in Figure 9(g).

(c) If one of \prec' and \prec'' between t_1 and t_2 is undefined, without loss of generality, we assume that \prec' is undefined, then

$$t_1 \prec t_2 \text{ when } t_1 \prec' t_2$$

$$t_2 \prec t_1 \text{ when } t_2 \prec' t_1$$

In addition, $C(t_1, t_2) = 0$.

(d) If both of \prec' and \prec'' between t_1 and t_2 are undefined, then the crossing relation between t_1 and t_2 is undefined. In addition, $C(t_1, t_2) = 0$.

It can be easily seen that the crossing relation defined above is a partial ordering. As a result, we can topologically sort this partial ordering to obtain an ordering of terminals called *topological ordering*. Clearly the following theorem holds.

Theorem 1 *The number of crossings between nets is minimum if the terminals are assigned to locations according to the topological ordering.*

On the other hand, in order to equalize the number of crossings across the partition, we use a sequential approach. We initialize the list with only one terminal and add to the list with one terminal at a time until all the terminals have been added to the list. It can easily be seen that the list can be expanded in such a way that the difference between the number of crossings above the edge \mathcal{E} and the number of crossings below \mathcal{E} between the nets whose terminals are on the list is no greater than 1. If we call the ordering of the terminals so constructed as *sequential ordering*, then we have the following result:

Theorem 2 *The difference between the number of crossings above the edge \mathcal{E} and the number of crossings below \mathcal{E} between the nets is no greater than 1 if terminals are assigned to locations according to the sequential ordering.*

The topological ordering is used for ordering terminals if the number of planar nets is to be maximized whereas the sequential ordering is used if the crossings

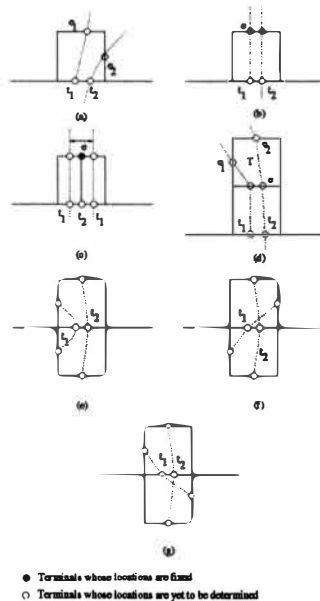


Figure 9. Terminal Ordering.

between the nets are to be distributed evenly over the substrate. Depending on the constraints of the problem, we may either use the first method to minimize the number of crossings or the second method to balance the number of crossings across the partition.

Finding Terminal Locations

After the ordering of the terminals or the relative positions among the terminals have been obtained, the terminals are assigned to an exact location on the tile edge. First the terminals will be assigned next to each other according to the ordering of the terminals. If a path-separation constraint between net n_i and net n_j is specified and the original terminal assignment cannot achieve the desired separation, either net n_i or net n_j will be permuted with some other terminal to satisfy the path-separation constraint. Note that this permutation of terminals may result in less number of planar nets as the original ordering of terminals has been changed. In addition, the path-separation constraint also effects the number of layers since an increase in the value of minimum distance between nets leads to a decrease in the number of nets that can be assigned to a tile edge, and therefore resulting in an increase in the number of layers.

CHAPTER VI

TOWER ROUTING

In this chapter, we discuss the details of routing within each tower. Since all the terminal locations are specified and are located on the faces of the tower, all the towers can be independently routed. The objective of the tower routing is to complete the required interconnections while satisfying path-separation, parallel-length, via-type and via-number constraints.

The tower routing is completed in two steps: planar routing and three-dimensional routing.

1. Planar Routing: In the first step, a set of planar nets in each layer is selected and routed. Planar routing is useful in reducing the number of bends, minimizing the net lengths and avoiding the usage of large number of vias. As a result, planar routing is helpful in minimizing the noise due to reflection and minimize delay.

2. Residual Routing: The remaining nets are routed by using a three-dimensional router based on Soukup's style algorithm [20] while satisfying the constraints.

Planar Routing

In this section, we first consider the problem of finding a maximum planar subset for routing nets on different layers of the tower. We prove that the problem of finding such a maximum planar subset is NP-Hard and present an approximation algorithm.

We now introduce the terminology which is used in our discussion. Let k be the total number of routing layers. Let \mathcal{T} be a set of terminals t_{lw}^D where $D \in \{EAST, WEST, NORTH, SOUTH\}$, $1 \leq l \leq k, 1 \leq w \leq W_D$. Note that

D represents the face of the tower and W_D represents the width of the respective tower face. The superscript D will be dropped if it is clear from the context. A terminal t_{lw}^D is said to be vacant, if t_{lw}^D has not been assigned to any net and the terminal $t_{lw}^D \in \mathcal{T}$.

A net is considered routable in a certain layer if both of its terminals lie on the same layer, or if pillars of vacant terminals exist for each terminal so that the net terminals can be brought to the desired layer. Let us state the definition of routability of a net more precisely. Consider a net $n_i = (t_{l_1 w_1}^{D_1}, t_{l_2 w_2}^{D_2})$. Let us assume that $1 \leq l_1 \leq l$ and $1 \leq l_2 \leq l$. The net n_i is considered routable in layer l either if $l = l_1 = l_2$, or if all the terminals in sets $\{t_{l_1 w_1}^{D_1}, t_{(l_1-1)w_1}^{D_1}, \dots, t_{lw_1}^{D_1}\}$ and $\{t_{l_2 w_2}^{D_2}, t_{(l_2-1)w_2}^{D_2}, \dots, t_{lw_2}^{D_2}\}$ are vacant. We can similarly define, a net to be routable for other cases, when $l \leq l_1, l_2$, or $l_2 \leq l \leq l_1$.

We consider 2 types of nets in our discussion. Nets that can be routed only on layer i are denoted as \mathcal{N}_i while nets that can be routed on either layer i or layer $i+1$ are denoted as $\mathcal{N}_{i,i+1}$. For example, \mathcal{N}_1 consists of a set of nets that can be routed only on layer one. Similarly sets $\mathcal{N}_2, \mathcal{N}_3, \dots, \mathcal{N}_k$ are defined. \mathcal{N}_{12} represent a set of nets that can be routed either on layer 1 or layer 2. Similarly sets $\mathcal{N}_{12}, \mathcal{N}_{23}, \dots, \mathcal{N}_{k-1,k}$ are defined (see Figure 10). If two nets that are routable on layers i and $i+1$ share a same pillar (see Figure 11), then a conflict occurs if the net with the terminal on a layer less than i (net 1 in Figure 11) is assigned to layer $i+1$ where the other net is assigned to layer i . Thus, if two nets share a same pillar, the net with the terminal on a layer less than i (net 1 in Figure 11) can only be assigned to \mathcal{N}_i while the other net can only be assigned to \mathcal{N}_{i+1} to avoid the possible conflicts.

Figure 12 gives a formal description of the algorithm Planar-Routing. Algorithm Planar-Routing finds two different solutions of planar subsets and selects the best one among the two. The first solution represented by \mathcal{S}_1 (see Figure 12) is generated by finding two planar subsets for each layer pair by using subroutine

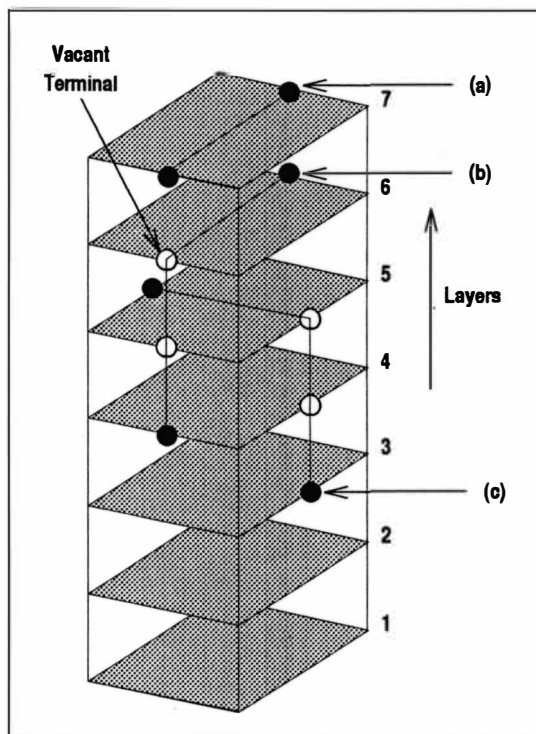


Figure 10. A Tower Showing Different Types of Nets.

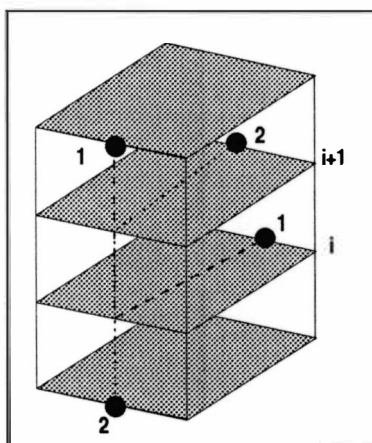


Figure 11. Potential Conflicts Among Nets.

2-RMPS. Finally a maximum planar subset (MPS) is chosen for the last layer and added to \mathcal{S}_1 (in case of number of layers is odd). The second solution is generated by choosing a maximum planar subset (MPS) for the first layer and then finding two planar subsets thereafter for each layer pair. The second solution is represented by \mathcal{S}_2 (see Figure 12). In case of even number of layers, a maximum planar subset for the last layer is chosen and is added to \mathcal{S}_2 . Algorithm Planar-Routing selects the maximum of \mathcal{S}_1 and \mathcal{S}_2 . Once a set of two planar subset of nets have been selected they are routed on the respective layers while satisfying the path-separation and parallel length constraints. In case the constraints cannot be satisfied for certain nets, then these nets are routed by the three dimensional router in the residual routing phase.

The subroutine 2-RMPS finds 2-restricted maximum planar subset, such that first set is routable on layer i and the second set is routable on layer $i + 1$. Subroutine 2-RMPS selects a maximum two planar subsets from three different strategies. The first strategy uses the bipartite subgraph of \mathcal{N}_{12} generated by the algorithm MBS [5] as the two planar subsets X_1 and Y_1 . The performance ratio of the algorithm MBS is at least 0.75 [5]. The second strategy finds a maximum planar subset of $\mathcal{N}_1 \cup \mathcal{N}_{12}$ and the maximum planar subset of \mathcal{N}_2 as the two planar subsets X_2 and Y_2 respectively. The subroutine $\text{MPS}(\mathcal{N}_i)$ finds the maximum planar subset for the given nets such that the set is routable on layer i . Subroutine MPS is based on the algorithm for finding a maximum independent set in circle graphs presented in [21]. The third strategy is similar to the second strategy. The algorithm 2-RMPS then returns the best result among the three strategies.

The time complexity of the algorithm 2-RMPS is dominated by the time complexity of MPS and the time complexity of MBS. Since the time complexity for both MPS and MBS is $O(m^2)$, the time complexity of the algorithm 2-RMPS

is $O(m^2)$ where m is the number of nets. Algorithm 2-RMPS is formally described in Figure 13.

The overall time complexity of the algorithm Planar-Routing is dominated by the complexity of subroutine 2-RMPS which is $O(m^2)$. Therefore, the time complexity of the algorithm Planar-Routing is $O(km^2)$.

Provably Good Algorithm for 2-RMPS: In the following, we prove that restricted maximum 2-planar subset problem is NP-hard, and develop an approximation algorithm for solving such a problem.

Let us start with some terminology. Given a set of nets \mathcal{N} , a set $\mathcal{N}' \subseteq \mathcal{N}$ is called a *planar subset* if the nets in \mathcal{N}' are pairwise independent. A *maximum planar subset* (1-MPS) is one with the maximum number of nets among all planar subsets. A *k-planar subset* can be defined as a set consisting of k disjoint planar subsets and a *maximum k-planar subset* (k -MPS) has the maximum number of vertices among all such k -planar subsets.

The problem of finding maximum k -planar subset in a switch box is equivalent to finding a maximum k -colorable subgraphs in a corresponding circle graph G [26]. Maximum k -colorable subgraph problem is known to be NP-hard for general graphs, since it includes as special cases both the 1-MPS and chromatic number problem [9, 26]. Planar subset problem in a switch box is polynomial time solvable [21], but for $k = 2$, the k -MPS is NP-complete [19]. In [5], a provably good algorithm was presented for k -MPS problem and the following theorem was proved

Theorem 3 *Given a set of nets, the algorithm finds a k planar subset such that $\rho \geq (1 - (1 - \frac{1}{k})^k)$ where ρ is the ratio of solution found with optimal solution of k -MPS problem.*

In the restricted maximum two planar subset problem, vertices are restricted to certain layers. We call such a problem as k -RMPS problem. Since we route on a layer pair each time, we restrict ourselves to description of 2-RMPS.

Algorithm Planar-Routing(\mathcal{N}, k, S)
Input: \mathcal{N} : Set of nets that pass through a tower k : Number of routing layers.
Output: \mathcal{S} : Set of planar nets
<pre> begin if k is odd then $t = 1$; else $t = 0$; $\mathcal{S}_1 = \phi$; for $j = 1$ to $\lfloor \frac{k}{2} \rfloor$ $S = 2\text{-RMPS}(\mathcal{N}_{2j-1} - \mathcal{S}_1, \mathcal{N}_{2j} - \mathcal{S}_1)$; $\mathcal{S}_1 = S \cup \mathcal{S}_1$; if ($t = 1$) then $\mathcal{S}_1 = \mathcal{S}_1 \cup \text{MPS}(\mathcal{N}_L - \mathcal{S}_1)$; $\mathcal{S}_2 = \text{MPS}(V_1)$; for $j = 1$ to $\lfloor \frac{k}{2} \rfloor - 1$ $S = 2\text{-RMPS}(\mathcal{N}_{2j} - \mathcal{S}_2, \mathcal{N}_{2j+1} - \mathcal{S}_2)$; $\mathcal{S}_2 = S \cup \mathcal{S}_2$; if ($t = 0$) then $\mathcal{S}_2 = \text{MPS}(\mathcal{N}_L - \mathcal{S}_2)$; $S = \text{SELECT_MAX}(\mathcal{S}_1, \mathcal{S}_2)$; end.</pre>

Figure 12. Algorithm Planar-Routing.

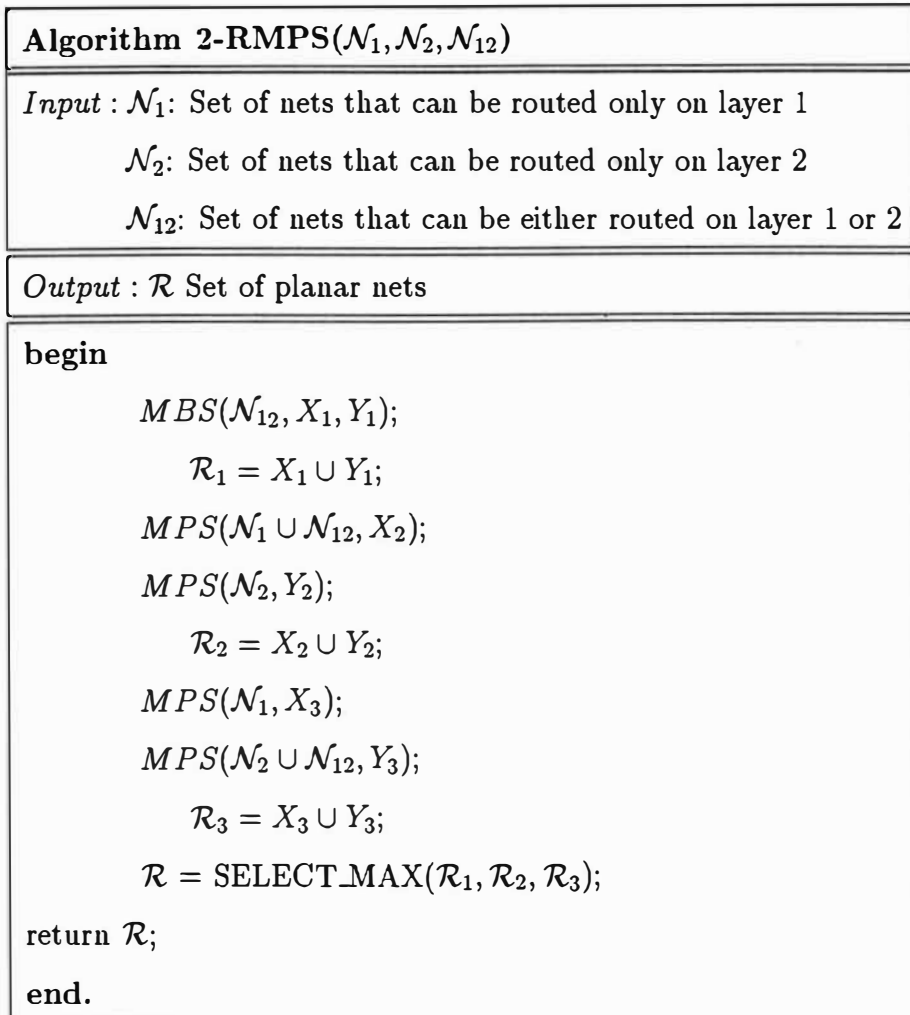


Figure 13. Algorithm 2-RMPS.

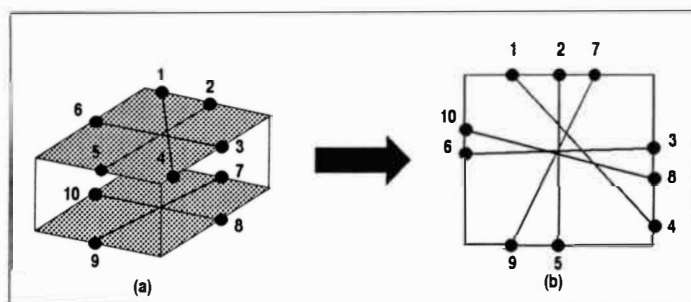


Figure 14. Transformation of Tower Routing Problem Into a Switch Box Problem.

Note that the problem of finding two planar subset of nets from a given two layers of a tower is equivalent to that of finding a two planar subset in a switch box. Figure 14 clearly describes this transformation. Hence algorithms for finding maximum planar subset in switch boxes can be extended to our problem of finding two planar subset. Let \mathcal{N}_1 , be the set of nets which can only be routed on layer one, \mathcal{N}_2 , be the set of nets which can only be routed on layer two, and \mathcal{N}_{12} , be the set of nets which can either be routed on layer one or layer two.

Instance: 2-Restricted Maximum Planar Subset Problem (2-RMPS): Given a switch box, and three sets $\mathcal{N}_1, \mathcal{N}_2, \mathcal{N}_{12}$.

Question: Does there exist planar subsets $N_1 \subseteq \mathcal{N}_1 \cup \mathcal{N}_{12}$ and $N_2 \subseteq \mathcal{N}_2 \cup \mathcal{N}_{12}$, such that $|N_1| + |N_2|$ is maximum among all such sets ?

Theorem 4 *2-RMPS is NP-Hard.*

Proof: By restricting $\mathcal{N}_1 = \mathcal{N}_2 = \phi$, 2-RMPS problem is equivalent to 2-MPS in a circle graph, which is NP-hard [19]. Thus, 2-RMPS problem is also NP-hard. \square

As 2-RMPS problem is NP-hard, we propose an approximation algorithm which guarantees at least 60% of the optimal solution. For a 2-restricted maximum planar subset problem in a graph G , we define the *performance ratio* of 2-RMPS to be $\rho = \frac{S}{S^*}$, where S is the size of the 2-restricted planar subsets obtained by the algorithm 2-RMPS and S^* is the size of the maximum 2-restricted maximum planar subsets for a given graph G .

Theorem 5 *Let ρ be the performance ratio of the algorithm 2-RMPS. For any given instance of the problem, the algorithm 2-RMPS produces a solution such that $\rho \geq 0.6$.*

Proof: Let the contributions of $\mathcal{N}_1, \mathcal{N}_2$, and \mathcal{N}_{12} in the optimal solution S^* be S_1^* , S_2^* , and S_{12}^* respectively, .i.e., $S^* = S_1^* \cup S_2^* \cup S_{12}^*$ where $S_1^* \subset \mathcal{N}_1, S_2^* \subset \mathcal{N}_2, S_{12}^* \subset \mathcal{N}_{12}$. Let $S = S_1 \cup S_2 \cup S_{12}$ represent the planar subset obtained as a result of

2-RMPS where $S_1 \subseteq \mathcal{N}_1$, $S_2 \subseteq \mathcal{N}_2$, and $S_{12} \subseteq \mathcal{N}_{12}$. We denote the cardinality of any set S_{12}^* as $|S_{12}^*|$. We will show that $|S| \geq 0.6|S^*|$.

Let α be defined as follows:

$$\alpha = \frac{|S_{12}^*|}{|S^*|} \quad (6.1)$$

and therefore

$$1 - \alpha = \frac{|S_1^* \cup S_2^*|}{|S^*|} \quad (6.2)$$

Let $R1 = X_1 \cup Y_1$ be the solution generated by the algorithm 2-RMPS (by MBS), $R2 = X_2 \cup Y_2$ be the solution generated by the second strategy from the algorithm 2-RMPS, and $R3 = X_3 \cup Y_3$ be the solution generated by the third strategy from the algorithm 2-RMPS (see Figure 13).

If algorithm 2-RMPS selects $R1$ when α is greater than $1 - \alpha$. In such a case $\rho \geq \frac{3}{4}\alpha$ [5]. On the other hand if the algorithm 2-RMPS selects $R2$ or $R3$, the performance ratio is calculated as follows: Let $S_{12}^* = S_{12}^{1*} \cup S_{12}^{2*}$ where $S_{12}^{1*} \subset \mathcal{N}'_1$ and $S_{12}^{2*} \subset \mathcal{N}'_2$. Then, we have either $|S_{12}^{1*}| \geq 0.5|S_{12}^*|$ or $|S_{12}^{2*}| \geq 0.5|S_{12}^*|$. Without loss of generality, we assume that $|S_{12}^{1*}| \geq 0.5|S_{12}^*|$ (the case when $|S_{12}^{2*}| \geq 0.5|S_{12}^*|$ can be similiarly proved). Therefore the performance ratio ρ ,

$$\rho \geq \frac{|S_1^* \cup S_2^*|}{|S^*|} + 0.5|S_{12}^*| \quad (6.3)$$

$$\rho \geq 1 - \alpha + \frac{\alpha}{2} = 1 - \frac{\alpha}{2} \quad (6.4)$$

By equating the performance ratio of MBS ($\frac{3}{4}\alpha$) and Equation (6.4) and solving for α , we get $\alpha = 0.8$. By substituting the value of α , we obtain the performance ratio for the algorithm 2-RMPS as follows:

$$\rho = \max\left\{1 - \frac{\alpha}{2}, \frac{3}{4}\alpha\right\} \geq 0.6.$$

Hence the performance of the algorithm 2-RMPS ≥ 0.6 . \square

Figure 15 represents the $\alpha - \rho$ graph for 2-RMPS. X-axis represents α while the Y-axis represents the performance ratio ρ . It can be clearly seen from Figure 15 that the performance ratio of algorithm 2-RMPS is at least 0.6. For any given input the solution of the 2-RMPS always lies inside the shaded region. Notice that the performance ratio at the intersection of the two lines is 0.6 which is the lower bound on the performance of 2-RMPS.

Satisfying Constraints

In this section we describe the method used to satisfy the path-separation, via-number and parallel-path-length constraints.

Noise due to crosstalk is minimized by satisfying the path-separation constraint. If the path-separation constraint is the same for all the net pairs i and j , then the path-separation constraint is satisfied by setting the grid separation equal to the path separation value. However, path-separation constraint is critical for nets whose signals change frequently such as clock nets, as they are more

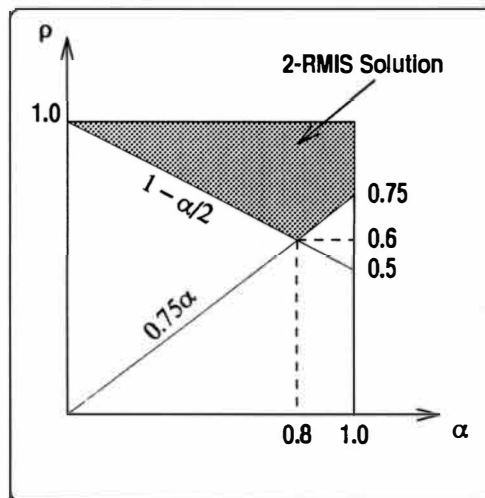


Figure 15. $\alpha - \rho$ Graph for 2-RMPS.

likely to induce crosstalk to their neighboring nets. As a result, the net-separation constraint varies from net to net and hence is not uniform. Our routing algorithm takes care of non-uniform net-separation constraints by using the “cable routing” technique. The route of a net in regular routing is a “line”. In contrast, the route of the net in “cable routing” is a “cable” consisting of a core “line” and several surrounding “lines” (See Figure 16(c)). Figure 16(a) and (b) show the cross section of a “cable” when path separation constraint is one and two respectively. Finally, the via-number and parallel-path-length constraints are satisfied by forcing the signal path of a net to change the direction in which it is routed.

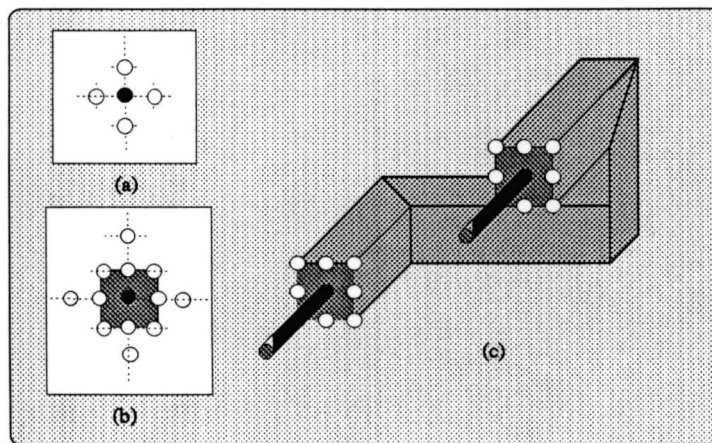


Figure 16. Cable Routing.

CHAPTER VII

EXPERIMENTAL RESULTS

The proposed approach is implemented in C on Sun SparcStation 1+ and tested on several industrial benchmarks such as MCC1 and MCC2 [12, 13], as well as several randomly system generated examples. In this chapter, we discuss the results obtained on MCC1 and a randomly generated example henceforth referred as to *SYS1*.

The design of MCC1 consists of 6 chips, 765 I/O pins and contains 799 signal nets, two power nets, one ground net and a grid size of about 600×600 . Figure 17 shows an initial interconnection pattern of MCC1.

As stated earlier, the first step of the routing algorithm is tiling which is a recursive approach of partitioning the substrate. Figure 18 shows the substrate

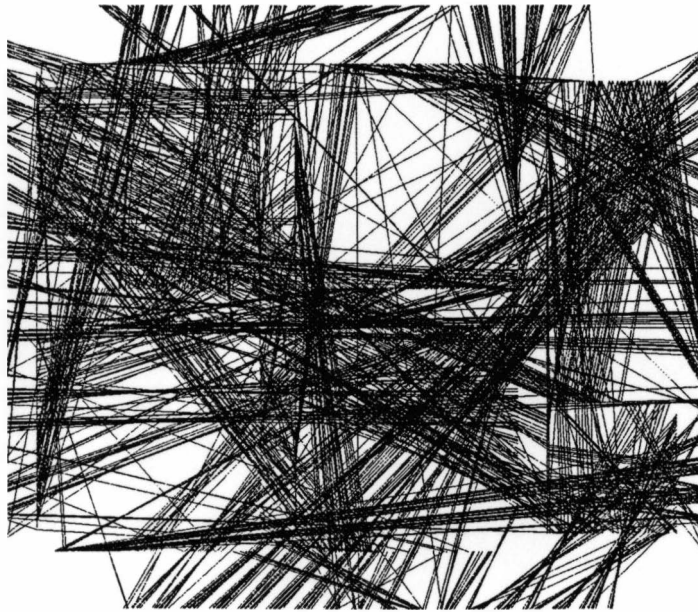


Figure 17. Interconnection Pattern of MCC1 Before Routing Distribution.

after being partitioned into a set of tiles. The tiles are referred with respect to rows and columns. For example, $\text{tile}[3][2]$ is the area intersecting the third row and second column (see Figure 18). $\text{Tile}[3][2]$ has a capacity of 187 nets along the X-direction and 109 along the Y-direction. Notice (see Figure 17) that the area covered by $\text{tile}[3][2]$ is one of the densest areas on the MCC1 substrate. In total, the substrate was partitioned into 63 tiles with different capacities along the X-direction and Y-direction. Based on the density of the tiles the proposed algorithm can recursively partition the tiles into subtiles.

The next step of the routing algorithm is to uniformly distribute the wiring in the XY-plane and the Z-dimension while estimating the number of layers to be used for routing. All the tile edges have to meet their capacities during this phase. $\text{Tile}[3][2]$ was allocated 116 nets along the X-direction and 85 along the Y-axis. At the completion of this step an estimate on the number of layers was obtained and was equal to be 10.

The next step is to assign terminals to the tile edges. Figure 19 shows a interconnection pattern after the terminal assignment step. As a result of the terminal assignment step, significant number of the nets become planar. Table 1

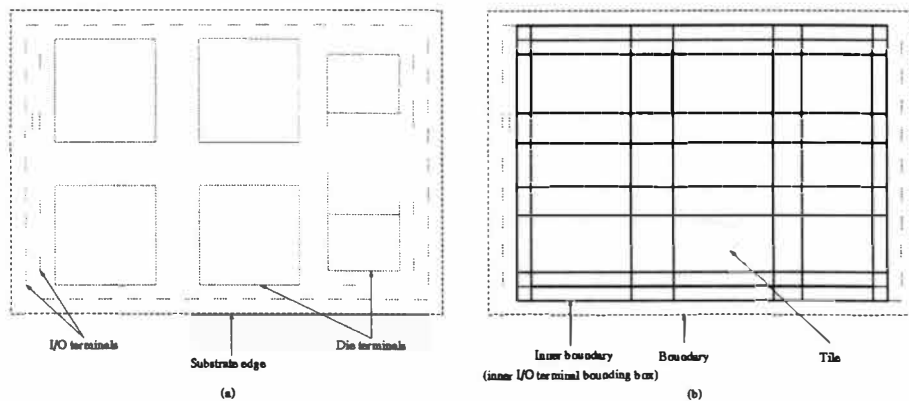


Figure 18. Tiling Pattern for MCC1.

shows the ratio of number of type I nets and type II nets to the total number of nets. Notice that the ratio of the number of type I nets to the total number of nets is over 42%. Also the type I nets and type II nets account for more than 65% of the total nets resulting in faster tower routing. The planar nets are selected from either type I or type II nets by using an approximation algorithm which has been described in a previous chapter. It can be clearly seen from Figure 19 that the nets have been uniformly distributed.

Finally, each tower is routed independently in three dimensions based on the algorithm presented in [20]. Figure 20 shows typical routing in two adjacent layers of two towers of MCC1 where net-separation is set equal to 2 for all critical nets. Notice that significant amount of nets are routed in a planar fashion. Also notice that the routing space has been utilized efficiently by a uniform distribution of nets and a good terminal assignment.

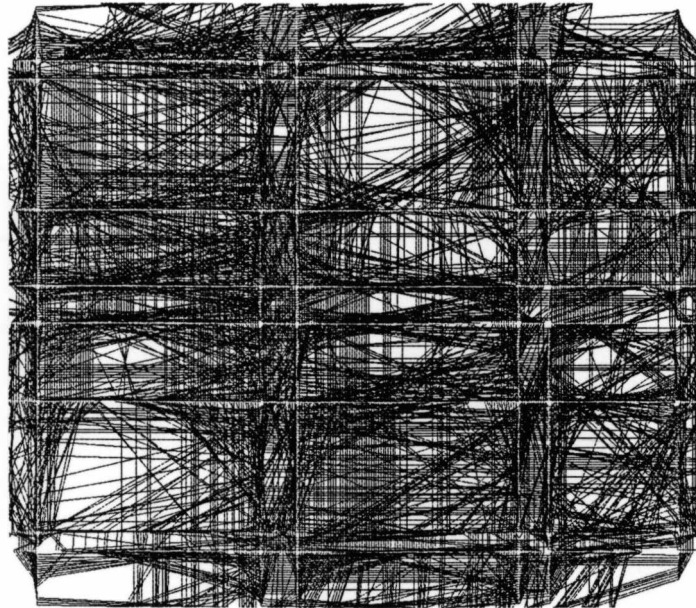


Figure 19. Interconnection Pattern of MCC1 After Terminal Assignment.

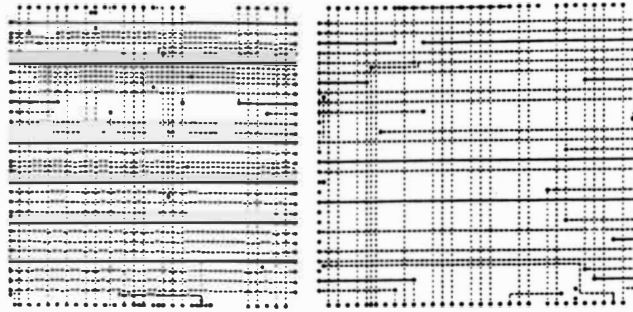


Figure 20. Signal Paths on Two Layer Pairs in MCC1.

Table 1

Percentage of the Planar Nets in MCC1

Type of nets	Avg. % in a tower	Max. % in a tower	Min % in a tower
Type I	42	66	0
Type II	24	100	0

Table 2

Effects of Different Path-Separation Values in MCC1

Path-Separation	Number of layers
2	8
3	10
4	12

Figure 21 shows an elevation routing profile of MCC1 describing the number of vias used per column for six layers of MCC1. This figure is useful in determining the ratio of the number of vias used to the total number of available vias. It can be seen from Figure 21 that the total number of vias used in the lower layers is much higher than that in the upper layers. Also, this figure illustrates the uniform distribution of the routing space and validity of our algorithm. The spikes seen in the graph are formed at the tower faces where the density is high due to the routing on the faces of the tower. MCC1 has a capacity of 245 vias/column (see Figure 21).

Figure 22 projects a top view (plan) of one of the towers in MCC1. This figure shows the number of nets per unit area which have been routed in the tower. Also, this figure facilitates in getting a visual idea of the working of our algorithm while identifying areas of high routing density called *hot spots*. It can be clearly seen from Figure 22 that the routing is uniform. In addition, it can also be seen that 65% of the area is half or less denser, 34% of the area uses from 0.6 to 0.8 of the total capacity while less than 1% of the area is completely used.

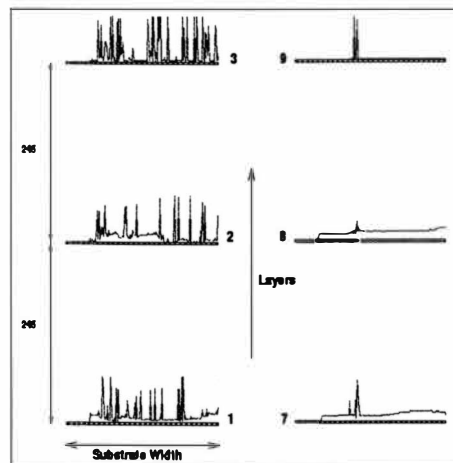


Figure 21. Elevation Routing Profile of MCC1.

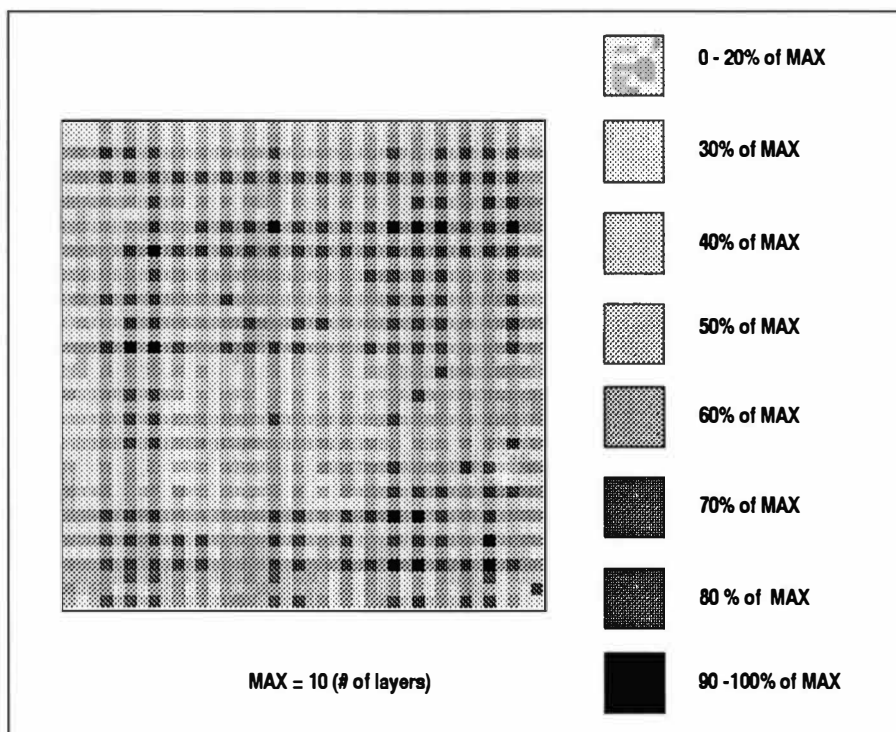


Figure 22. A PLAN Showing Total Net Distribution of a Tower in MCC1.

CHAPTER VIII

CONCLUSIONS

A new routing methodology for thick film MCMs has been developed. This methodology can satisfy the delay, noise, and fabrication constraints. In addition, the approach is amiable to parallel processing. Implementation results on benchmarks verify the validity of the proposed approach.

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